AzureWave Technologies, Inc.

AW-XH327-PUR

IEEE 802.11 a/b/g/n/ac/ax Wi-Fi

+ Bluetooth 5.2 Combo SIP Module

Datasheet

Rev.A

DF

(For Standard)

Features

WiFi

- 802.11a/b/g/n/ac/ax compliant, dual-band capable (2.4/5 GHz)
- 5GHz : 20/40/80-MHz channels, 1024-QAM, 2x2 MIMO providing up to 1.2 Gbps PHY data rate
- 2.4 GHz: 20/40-MHz channels, 1024-QAM, 2x2 MIMO providing up to 574 Mbps PHY date rate
- 802.11ax STA mode and Soft AP mode with 11ax scheduled access
- Supports 802.11d, h, k, r, v, w, ai
- Zero-wait dynamic frequency selection (DFS): Background channel availability check (CAC) scan for immediate switch to candidate DFS channel
- On-chip power amplifiers and low-noise amplifiers
- Supports 2 and 3-antenna configurations
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE
- Fast VSDB (Virtual Simultaneous Dual Band)
- Worldwide regulatory support: Global products supported with worldwide homologated design
- Integrated Arm® Cortex® R4 processor with tightly coupled memory for complete WLAN subsystem functionality. This architecture offloads the host processor completely from WLAN functionality.
- Transmission and reception of HE-SU and HE-ER-SU PPDU.
- Reception of HE-MU PPDU -OFDMA/MU-MIMO Frame.
- Transmission of HE-TB PPDU (Uplink MU OFDMA).

Bluetooth

- Bluetooth 5.2 (BDR + EDR + BLE).
- All Bluetooth 5.0/5.1/5.2 optional features supported including LE-Audio.
- Dedicated Bluetooth RF path for best WLAN-BT coexistence performance.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM/I2S for audio data.
- Supports multiple simultaneous Advanced Audio Distribution.
- Profiles (A2DP) for stereo sound.
- On-chip memory includes 512 KB SRAM and 2 MB ROM.

Revision History

Document NO: R2-1327-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2023/04/24	DCN029130	● Initial Version	Barry Tsai	N.C. Chen

Table of Contents

1. Introduction

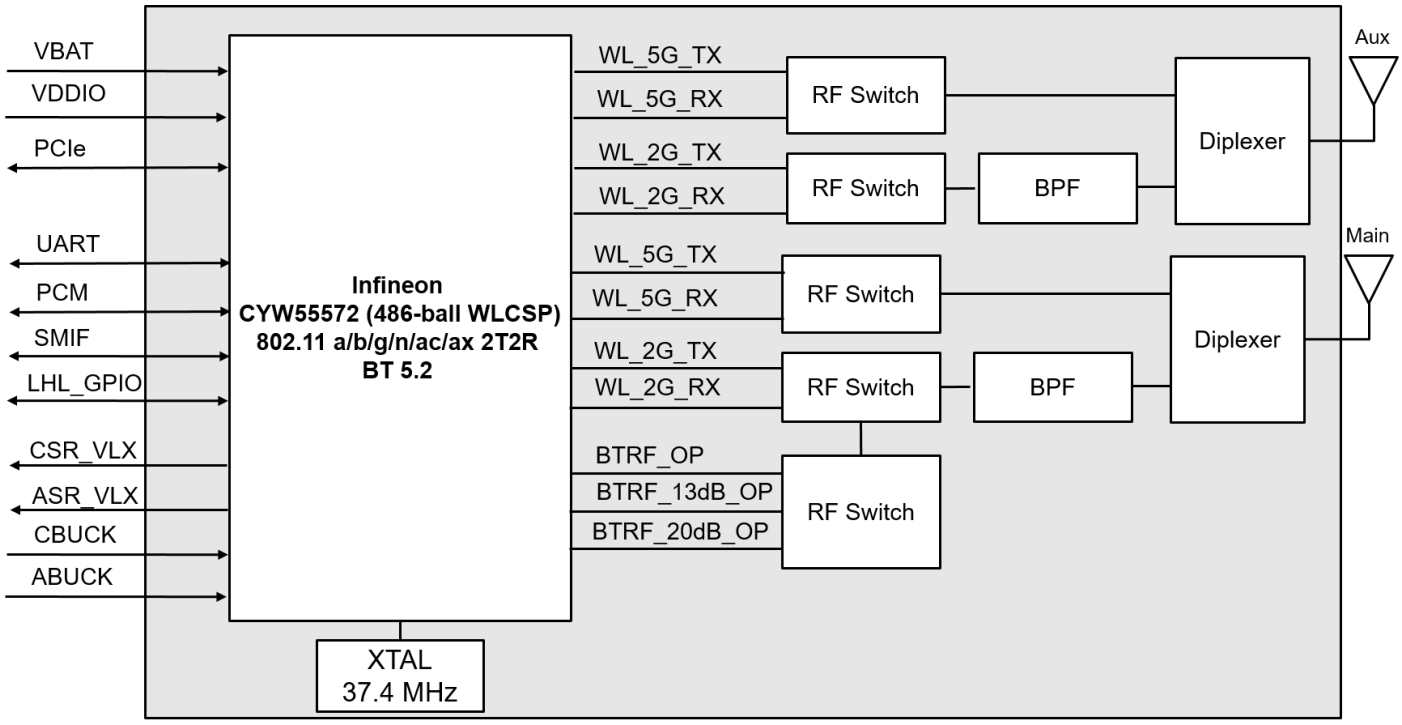
1.1 Product Overview

The AW-XH327-PUR device provides the highest level of integration for Commercial and Consumer IoT wireless systems with integrated dual-band 2x2 MIMO IEEE 802.11ax WLAN MAC/baseband/radio, Bluetooth 5.2 MAC/baseband/radio, and integrated Power Management Unit. WLAN and Bluetooth radios also include on-chip power amplifiers and low-noise amplifiers to further reduce the need for external components.

WLAN interfaces to host processor through a PCIe v3.0 Gen2 interface while Bluetooth host interface is provided through high-speed 4-wire UART interface. Additionally, the Bluetooth section supports PCM and I2S interfaces for audio applications.

AW-XH327-PUR is qualified to operate across Industrial (-40 °C to +85 °C) temperature range.

1.2 Block Diagram



AW-XH327-PUR Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi + Bluetooth 5.2 Combo SIP Module
Major Chipset	Infineon CYW55572 (486-ball WLCSP)
Host Interface	WiFi + BT ● PCIe + UART **Note**: Please refer to G10 pin of 2.3 Host configuration interface table for your interface choice
Dimension	10mm x 10mm x 1.26mm
Form factor	● Sip module,117 pins
Antenna	2T2R, external ANT1(Main)：WiFi/Bluetooth → TX/RX ANT2(Aux)：WiFi → TX/RX
Weight	TBD

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax 2T2R
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	WLAN: 2.4 / 5 GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9), 1024-QAM(MCS10~11)
Number of Channels	**2.4GHz** ■ USA, Canada and Taiwan – 1 ~ 11 ■ China, Most European Countries – 1 ~ 13 ■ Japan, 1 ~ 13

<table>
<tr><td></td><td>5GHz
■ USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165</td></tr>
<tr><td>Output Power[1]
(Board Level Limit)*</td><td>
2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)
@EVM<8%</td><td>18</td><td>19.5</td><td>21</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦-25 dB</td><td>16.5</td><td>18</td><td>19.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS11)
@EVM≦-35 dB</td><td>13.5</td><td>15</td><td>16.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)
@EVM<-25 dB</td><td>14.5</td><td>16.5</td><td>18.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>13.5</td><td>15.5</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)
@EVM≦-27 dB</td><td>13.5</td><td>15.5</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11ac (VHT20 MCS8)
@EVM≦-30 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ac (VHT40 MCS9)
@EVM≦-32 dB</td><td>10.5</td><td>12.5</td><td>14.5</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9)
@EVM≦-32 dB</td><td>9.5</td><td>11.5</td><td>13.5</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS11)
@EVM≦-35 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11ax (HE40 MCS11)
@EVM≦-35 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11ax (HE80 MCS11)
@EVM≦-35 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

[1] Unless otherwise stated, limit values apply for an ambient temperature of +25 °C.

Receiver Sensitivity**

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-89	-86	dBm
11g (54Mbps)		-77	-74	dBm
11n (HT20 MCS7)		-75	-72	dBm
11ax (HE20 MCS11)		-64	-61	dBm

5G(n/ac packets with LDPC)

	Min	Typ	Max	Unit
11a (54Mbps)		-74	-71	dBm
11n (HT20 MCS7)		-72	-69	dBm
11n (HT40 MCS7)		-69	-66	dBm
11ac (VHT20 MCS8)		-67	-64	dBm
11ac (VHT40 MCS9)		-63	-60	dBm
11ac (VHT80 MCS9)		-60	-57	dBm
11ax (HE20 MCS11)		-61	-58	dBm
11ax (HE40 MCS11)		-56	-53	dBm
11ax (HE80 MCS11)		-55	-52	dBm

Data Rate

802.11b: 1, 2, 5.5, 11Mbps
802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n: MCS0~7 HT20/HT40
802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11ac: MCS0~8 VHT20
802.11ac: MCS0~9 VHT40/VHT80
802.11ax: MCS10~11 HE20/HE40/HE80

Security

- **WPA, WAPI STA, WPA2 (Enterprise) and WPA3 (Enterprise) support for powerful encryption and authentication**
- **AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility**
- **Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)**

*** If you have any certification questions about output power please contact FAE directly**
**** Project is in engineering stage, RF performance is still being verified.**

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 5.2</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2400~2483.5MHz</td></tr>
<tr><td>Modulation</td><td>GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)</td></tr>
<tr><td>Output Power*</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>4</td><td>7</td><td>10</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td>4</td><td>7</td><td>10</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity**</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td></td><td>-90</td><td>-87</td><td>dBm</td></tr>
<tr><td>EDR</td><td></td><td>-86</td><td>-83</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td></td><td>-92</td><td>-89</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

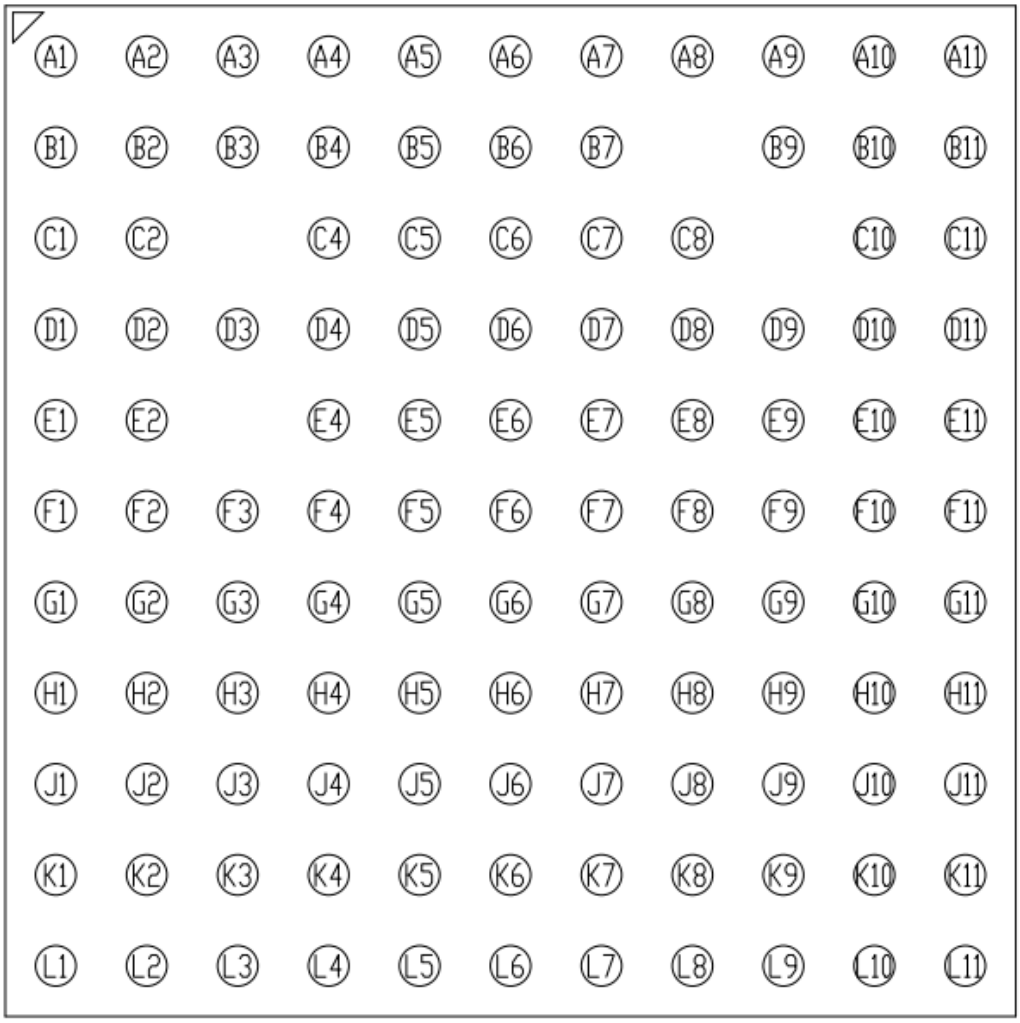
*** If you have any certification questions about output power please contact FAE directly**
**** Project is in engineering stage, RF performance is still being verified.**

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V
Operating Temperature	-40℃ to 85℃
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃ to 125℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

2. Pin Definition

2.1 Pin Map



AW-XH327-PUR Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
A1	GND	Ground.		GND
A2	PCIE_RDN	PCIE Receiver Differential Pair Negative Input		I
A3	PCIE_RDP	PCIE Receiver Differential Pair Positive Input		I
A4	PCIE_TDN	PCIE Transmitter Differential Pair Negative Output		O
A5	PCIE_TDP	PCIE Transmitter Differential Pair Positive Output		O
A6	PCIE_REFCLKN	PCIE Differential Pair Clock Source (100 MHz) Negative Input.		I
A7	PCIE_REFCLKP	PCIE Differential Pair Clock Source (100 MHz) Positive Input.		I
A8	GND	Ground.		GND
A9	CSR_VLX	CSR Power Stage Output to Inductor	0.9V	O
A10	ASR_VLX	ASR Power Stage Output to Inductor	1.12V	O
A11	GND	Ground.		GND
B1	GND	Ground.		GND
B2	GND	Ground.		GND
B3	GND	Ground.		GND
B4	GND	Ground.		GND
B5	GND	Ground.		GND
B6	GND	Ground.		GND
B7	GND	Ground.		GND
B9	CSR_VLX	CSR Power Stage Output to Inductor	0.9V	O
B10	ASR_VLX	ASR Power Stage Output to Inductor	1.12V	O
B11	GND	Ground.		GND
C1	WL_REG_ON	Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW55572 regulators. When this pin is high, the regulators are enabled and the	VDDIO	I

		WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.		
C2	BT_PCM_SYNC	PCM sync; can be master (output) or slave (input), or SLIMbus data.	VDDIO	I/O
C4	PCIE_CLKREQ_L	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.	3.3V	OD
C5	GND	Ground.		GND
C6	LHL_GPIO5	Miscellaneous General Purpose I/O	VDDIO	I/O
C7	BT_REG_ON	Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW55572 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.	VDDIO	I
C8	GND	Ground.		GND
C10	VBAT	3.3V power pin	3.3V	VCC
C11	VBAT	3.3V power pin	3.3V	VCC
D1	PCIE_PERST_L	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1	3.3V	I
D2	BT_PCM_IN	PCM data input.	VDDIO	I
D3	BT_PCM_OUT	PCM data output.	VDDIO	O
D4	BT_PCM_CLK	PCM clock; can be master (output) or slave (input).	VDDIO	I/O
D5	PCIE_PME_L	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3	3.3V	OD
D6	LHL_GPIO3	Miscellaneous General Purpose I/O	VDDIO	I/O
D7	LHL_GPIO2	Miscellaneous General Purpose I/O	VDDIO	I/O
D8	GND	Ground.		GND
D9	CBUCK_0P9	Internal Buck 0.9V voltage generation pin.	0.9V	I

D10	CBUCK_0P9	Internal Buck 0.9V voltage generation pin.	0.9V	I
D11	ABUCK_1P12	Internal Buck 1.12V voltage generation pin.	1.12V	I
E1	GND	Ground.		GND
E2	GPIO_0_WL_HOST_WAKE	WL Host Wake.	VDDIO	O
E4	BT_DEV_WAKE	Bluetooth DEVICE WAKE	VDDIO	I/O
E5	GND	Ground.		GND
E6	LHL_GPIO4	Miscellaneous General Purpose I/O	VDDIO	I/O
E7	GPIO_11_WL_UART_TX	Debug UART Serial Output.	VDDIO	O
E8	GND	Ground.		GND
E9	GPIO_10_WL_UART_RX	Debug UART Serial Input.	VDDIO	I
E10	GND	Ground.		GND
E11	ABUCK_1P12	Internal Buck 1.12V voltage generation pin.	1.12V	I
F1	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	VDDIO	O
F2	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	VDDIO	I
F3	BT_HOST_WAKE	Bluetooth HOST_WAKE.	VDDIO	I/O
F4	BT_CLK_REQ	A Bluetooth clock request.	VDDIO	I/O
F5	GND	Ground.		GND
F6	LHL_GPIO0	Miscellaneous General Purpose I/O	VDDIO	I/O
F7	LPO_IN	External Sleep Clock Input (32.768 kHz)		I
F8	GND	Ground.		GND
F9	GND	Ground.		GND
F10	GND	Ground.		GND
F11	VDDIO	1.8 V IO Supply for WLAN GPIOs	VDDIO	VCC
G1	BT_UART_TXD	UART Serial Output. Serial data output for the HCI UART interface.	VDDIO	O

G2	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	VDDIO	I
G3	GND	Ground.		GND
G4	GND	Ground.		GND
G5	GND	Ground.		GND
G6	GND	Ground.		GND
G7	GND	Ground.		GND
G8	GND	Ground.		GND
G9	GND	Ground.		GND
G10	GPIO_1	Strap option	VDDIO	I/O
G11	GND	Ground.		GND
H1	RESERVED	Please don't connect to this pin.		N/A
H2	RESERVED	Please don't connect to this pin.		N/A
H3	RESERVED	Please don't connect to this pin.		N/A
H4	RESERVED	Please don't connect to this pin.		N/A
H5	GND	Ground.		GND
H6	WL_DEV_WAKE	WL DEV_WAKE.	VDDIO	I/O
H7	GND	Ground.		GND
H8	GND	Ground.		GND
H9	RESERVED	Please don't connect to this pin.		N/A
H10	RESERVED	Please don't connect to this pin.		N/A
H11	RESERVED	Please don't connect to this pin.		N/A
J1	RESERVED	Please don't connect to this pin.		N/A
J2	RESERVED	Please don't connect to this pin.		N/A
J3	GND	Ground.		GND
J4	GND	Ground.		GND

J5	GND	Ground.		GND
J6	GND	Ground.		GND
J7	GND	Ground.		GND
J8	GND	Ground.		GND
J9	RESERVED	Please don't connect to this pin.		N/A
J10	RESERVED	Please don't connect to this pin.		N/A
J11	RESERVED	Please don't connect to this pin.		N/A
K1	GND	Ground.		GND
K2	GND	Ground.		GND
K3	GND	Ground.		GND
K4	GND	Ground.		GND
K5	GND	Ground.		GND
K6	BT_GPIO_11	BT General Purpose I/O	VDDIO	I/O
K7	GND	Ground.		GND
K8	GND	Ground.		GND
K9	GND	Ground.		GND
K10	GND	Ground.		GND
K11	GND	Ground.		GND
L1	GND	Ground.		GND
L2	RESERVED	Please don't connect to this pin.		N/A
L3	GND	Ground.		GND
L4	GND	Ground.		GND
L5	C0_ANT	WLAN/BT Main RF TX/RX path.		RF
L6	GND	GND	Ground.	
L7	GND	GND	Ground.	
L8	GND	GND	Ground.	

L9	GND	GND	Ground.	
L10	C1_ANT	WLAN Aux RF TX/RX path.		RF
L11	GND	GND	Ground.	

2.3 Host Configuration Interface Table

Pin No	Definition	Interface	Strap
G10	GPIO_1	PCIE	1

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	-0.5	-	6.0	V
VDDIO	DC supply voltage for digital I/O	-0.5	-	2.2	V
Tj	Maximum junction temperature	-	-	125	°C

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulator	3.135	3.3	3.465	V
VDDIO	DC supply voltage for digital I/O	1.71	1.8	1.89	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital I/O pins, VDDIO=1.8V					
V_{IH}	Input high voltage	0.65 × VDDIO	-	-	V
V_{IL}	Input low voltage	-	-	0.35 × VDDIO	V
V_{OH}	Output high voltage	VDDIO – 0.45	-	-	V
V_{OL}	Output Low Voltage	-	-	0.45	V

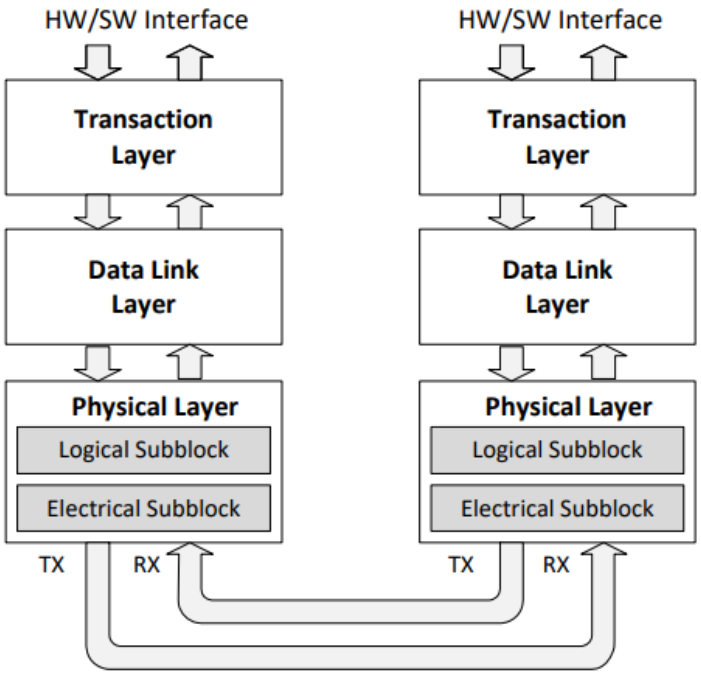
3.4 Host Interface

3.4.1 PCIe Interface

The PCI Express (PCIe) core in AW-XH327-PUR is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen2 speeds. This core contains all the necessary blocks, including logical and electrical functional sub blocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 20. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and AW-XH327-PUR device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

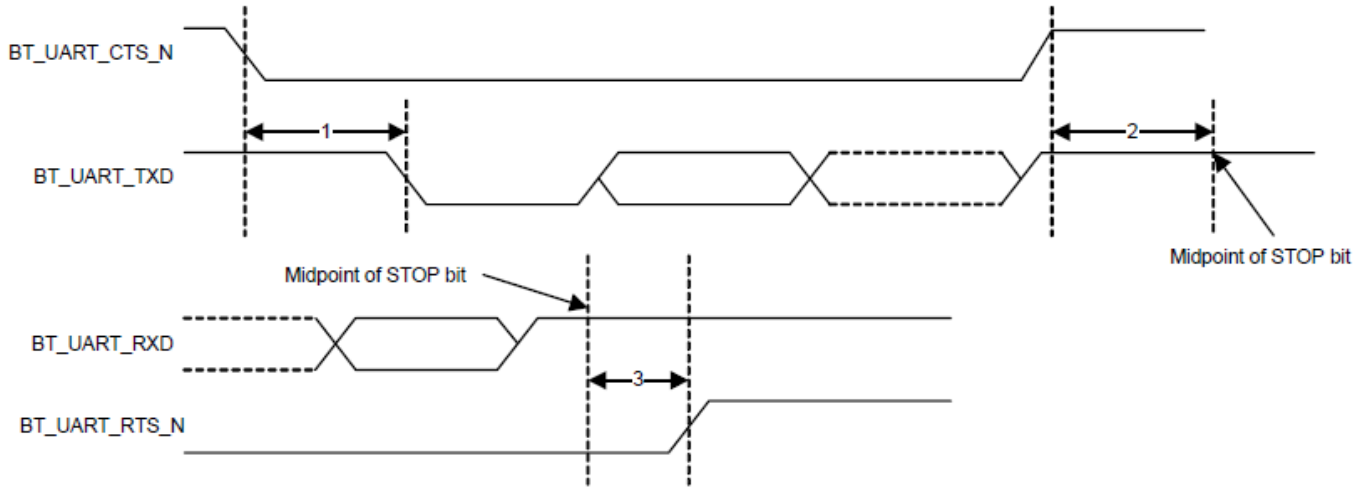


3.4.2 UART Interface

The AW-XH327-PUR UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The baud rate may be selected through a vendor-specific UART HCI command.
UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.0 UART HCI specification. The default baud rate is 115.2 Kbaud.
The AW-XH327-PUR UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.
Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-XH327-PUR UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

UART Interface Signals

PIN No.	Name	Description	Type
F1	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	O
F2	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	I
G1	BT_UART_TXD	UART Serial Output. Serial data output for the HCI UART interface.	O
G2	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	I



UART Timing

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

3.5 Power up Timing Sequence

AW-XH327-PUR has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals

■ **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-XH327-PUR regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

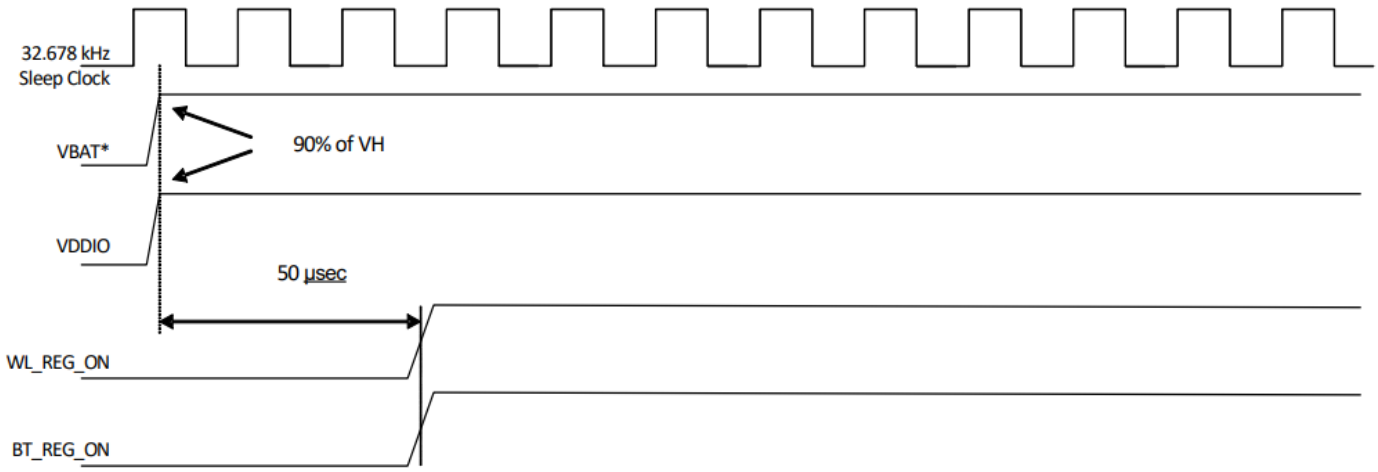
■ **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal AW-XH327-PUR regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note

■ AW-XH327-PUR has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating PCIe accesses.

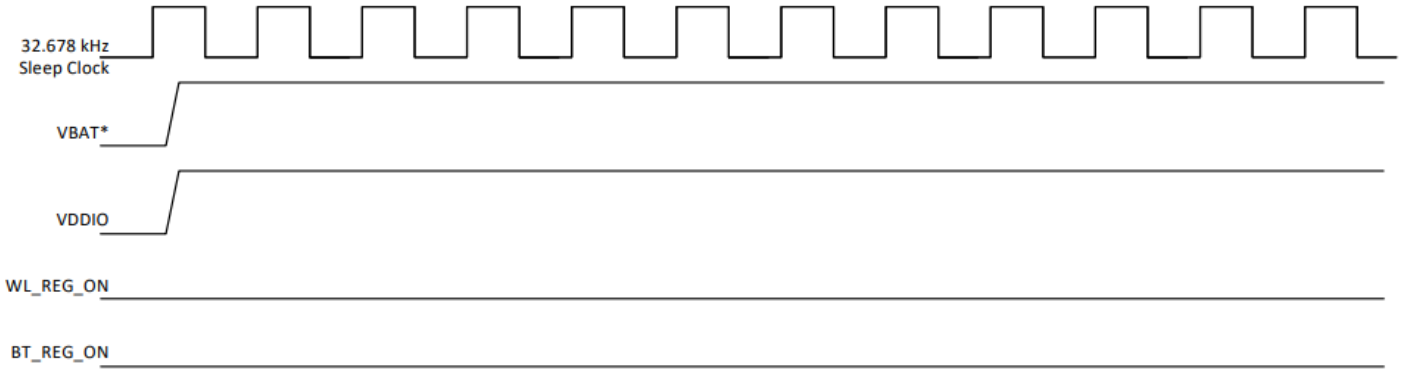
■ VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.

WLAN = ON, Bluetooth = ON



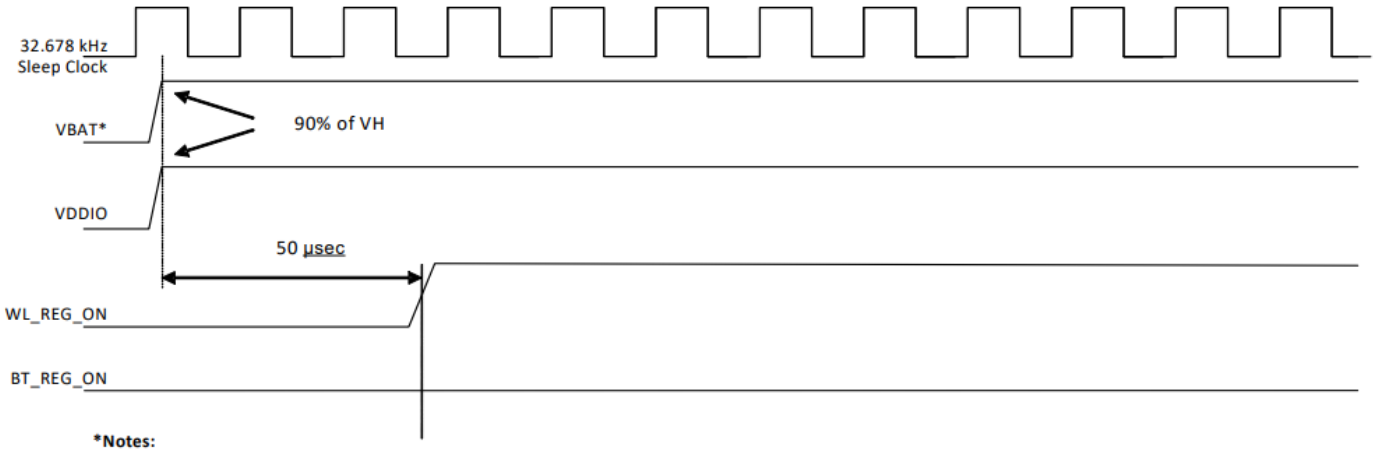
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF



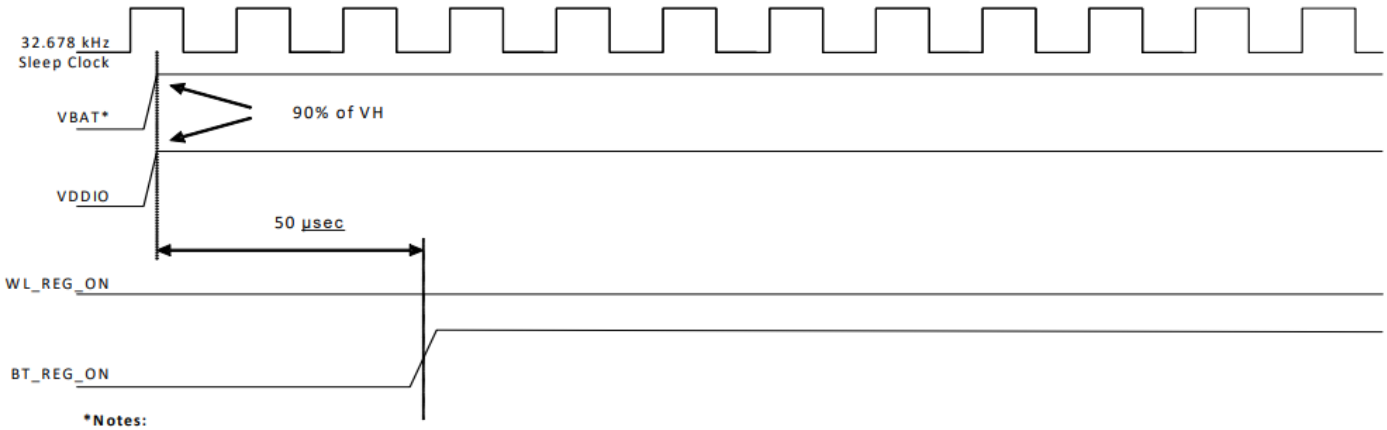
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF



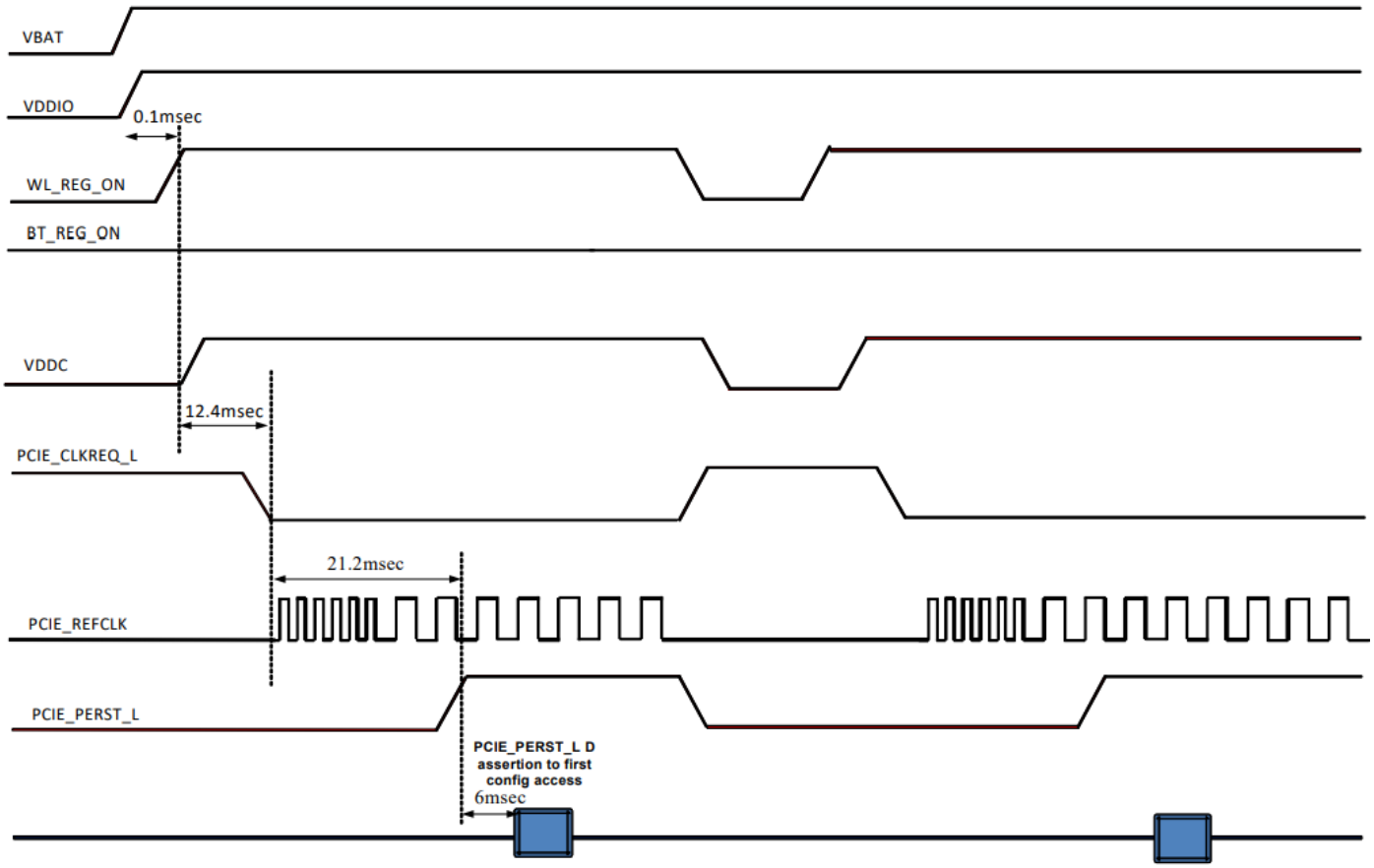
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = ON



***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN Power-Up Sequence for PCIe Host



There is variation of about +/-30% on above timing numbers

3.6 Power Consumption*

3.6.1 WLAN

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

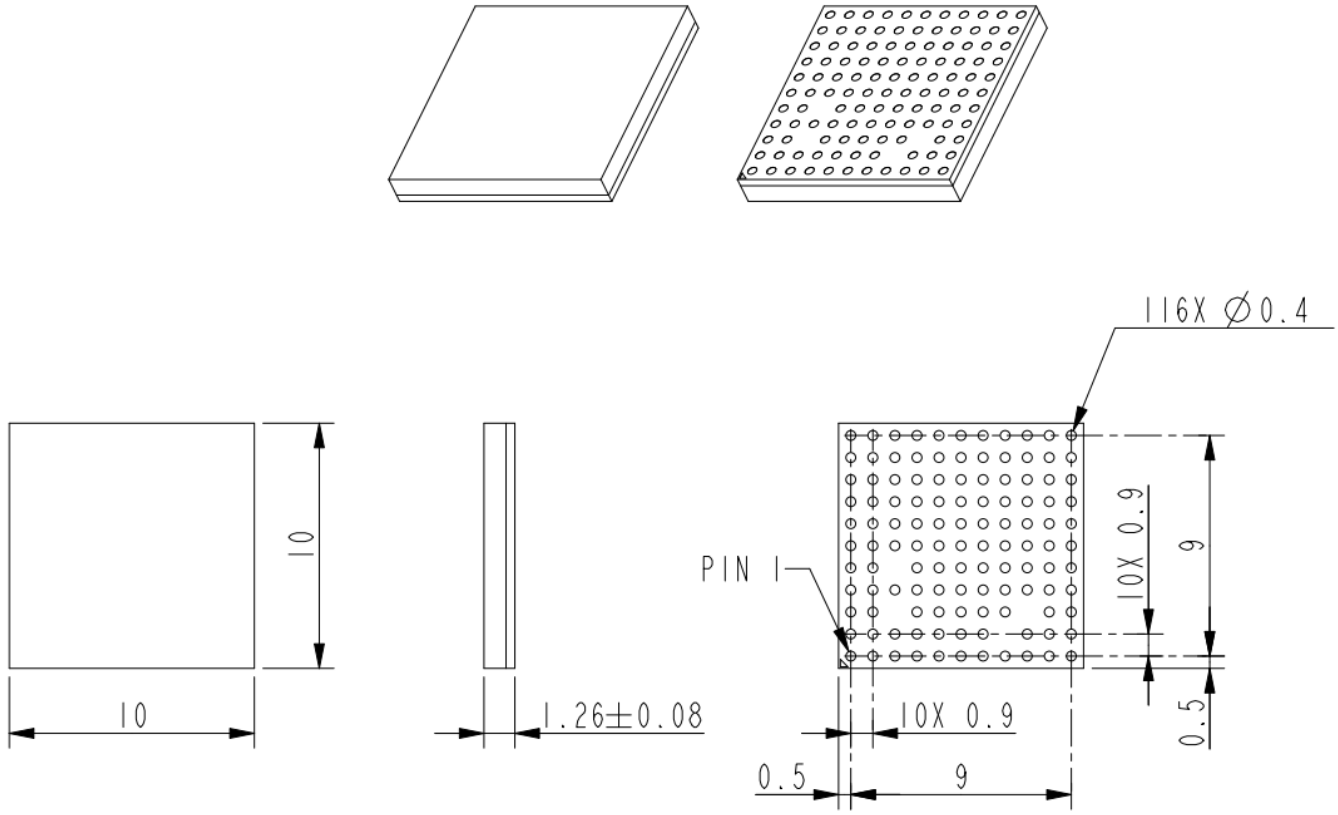
3.6.2 Bluetooth

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

4. Mechanical Information

4.1 Mechanical Drawing



5. Packaging Information

TBD