AW-XH316

IEEE 802.11 a/b/g/n/ac/ax Wi-Fi
+ Bluetooth 5.2 Combo SIP Module

Datasheet

Rev.A

DF

(For Standard)
Features

WiFi

- 802.11a/b/g/n/ac/ax compliant, dual-band capable (2.4/5 GHz).
- 5 GHz: 20/40/80-MHz channels, 1024-QAM, 2x2 MIMO providing up to 1.2 Gbps PHY data rate.
- 2.4 GHz: 20/40-MHz channels, 1024-QAM, 2x2 MIMO providing up to 574 Mbps PHY data rate.
- 802.11ax STA mode and Soft AP mode with 11ax scheduled access.
- Supports 802.11d, h, k, r, v, w, ai.
- Zero-wait dynamic frequency selection (DFS): Background channel availability check (CAC) scan for immediate switch to candidate DFS channel.
- On-chip power amplifiers and low-noise amplifiers.
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE.
- Fast VSDB (Virtual Simultaneous Dual Band)
- Security:
  - WPA, WAPI STA, WPA2 (Enterprise) and WPA3 (Enterprise) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
  - Worldwide regulatory support: Global products supported with worldwide homologated design
  - Integrated Arm® Cortex® R4 processor with tightly coupled memory for complete WLAN subsystem functionality. This architecture offloads the host processor completely from WLAN functionality.

Bluetooth

- Bluetooth 5.2 (BDR + EDR + BLE).
- All Bluetooth 5.0/5.1/5.2 optional features supported including LE-Audio.
- Dedicated Bluetooth RF path for best WLAN-BT coexistence performance.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM/I2S for audio data.
- Supports multiple simultaneous Advanced Audio Distribution.
- Profiles (A2DP) for stereo sound.
- On-chip memory includes 512 KB SRAM and 2 MB ROM.
## Revision History

**Document NO:** R2-1316-DST-01

<table>
<thead>
<tr>
<th>Version</th>
<th>Revision Date</th>
<th>DCN NO.</th>
<th>Description</th>
<th>Initials</th>
<th>Approved</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2021/04/16</td>
<td>DCN021583</td>
<td>Initial Version</td>
<td>JM.Pang</td>
<td>Chihhao Liao</td>
</tr>
</tbody>
</table>

The information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of AzureWave.
# Table of Contents

## Features

## Revision History

## Table of Contents

1. **Introduction** .................................................................................. 5
   - 1.1 Product Overview ........................................................................ 5
   - 1.2 Block Diagram ........................................................................... 5
   - 1.3 Specifications Table .................................................................... 6
     - 1.3.1 General ............................................................................... 6
     - 1.3.2 WLAN ............................................................................... 6
     - 1.3.3 Bluetooth ........................................................................... 8
     - 1.3.4 Operating Conditions ......................................................... 9

2. **Pin Definition** ........................................................................... 10
   - 2.1 Pin Map .................................................................................... 10
   - 2.2 Pin Table .................................................................................. 11

3. **Electrical Characteristics** .......................................................... 17
   - 3.1 Absolute Maximum Ratings ..................................................... 18
   - 3.2 Recommended Operating Conditions ....................................... 18
   - 3.3 Digital IO Pin DC Characteristics .......................................... 18
   - 3.4 Host Interface ........................................................................... 19
     - 3.4.1 SDIO Interface ................................................................... 19
     - 3.4.2 UART Interface ................................................................. 22
     - 3.4.3 PCIe Interface .................................................................... 24
   - 3.5 Power up Timing Sequence .................................................... 25
   - 3.6 Power Consumption ............................................................... 29
     - 3.6.1 WLAN .............................................................................. 29
     - 3.6.2 Bluetooth ........................................................................... 29

4. **Mechanical Information** .............................................................. 30
   - 4.1 Mechanical Drawing ................................................................. 30

5. **Packaging Information** ............................................................... 31
1. Introduction

1.1 Product Overview

The AW-XH316 module provides the highest level of integration for Commercial and Consumer systems, with integrated IEEE 802.11 a/b/g/n/ac/ax MAC/baseband/radio (dual-core 2×2 MIMO), Bluetooth 5.2+ Isochronous. It provides a small form-factor solution with minimal external components to drive down cost and allows for platform design flexibility in size, form, and function.

1.2 Block Diagram

![AW-XH316 Block Diagram](image)
# 1.3 Specifications Table

## 1.3.1 General

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Product Description</strong></td>
<td>IEEE 802.11 a/b/g/n/ac/ax Wi-Fi + Bluetooth 5.2 Combo SIP Module</td>
</tr>
<tr>
<td><strong>Major Chipset</strong></td>
<td>Infineon CYW55572 (486-ball WLCSP)</td>
</tr>
<tr>
<td><strong>Host Interface</strong></td>
<td>WiFi + BT</td>
</tr>
<tr>
<td></td>
<td>● SDIO + UART</td>
</tr>
<tr>
<td></td>
<td>● PCIe + UART</td>
</tr>
<tr>
<td><strong>Note:</strong></td>
<td>Please refer to G10 pin of 2.3 Host configuration interface table for your</td>
</tr>
<tr>
<td></td>
<td>interface choice</td>
</tr>
<tr>
<td><strong>Dimension</strong></td>
<td>12mm x 13mm x 1.21mm</td>
</tr>
<tr>
<td><strong>Form factor</strong></td>
<td>● Sip module, 142 pins</td>
</tr>
<tr>
<td><strong>Antenna</strong></td>
<td>2T2R, external</td>
</tr>
<tr>
<td></td>
<td>ANT1(Main) : WiFi/Bluetooth TX/RX</td>
</tr>
<tr>
<td></td>
<td>ANT2(Aux) : WiFi TX/RX</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td>TBD</td>
</tr>
</tbody>
</table>

## 1.3.2 WLAN

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>WLAN Standard</strong></td>
<td>IEEE 802.11 a/b/g/n/ac/ax 2T2R</td>
</tr>
<tr>
<td><strong>WLAN VID/PID</strong></td>
<td>N/A</td>
</tr>
<tr>
<td><strong>WLAN SVID/SPID</strong></td>
<td>N/A</td>
</tr>
<tr>
<td><strong>Frequency Range</strong></td>
<td>WLAN: 2.4 GHz / 5GHz Band</td>
</tr>
<tr>
<td><strong>Modulation</strong></td>
<td>DSSS</td>
</tr>
<tr>
<td></td>
<td>DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps)</td>
</tr>
<tr>
<td></td>
<td>OFDM</td>
</tr>
<tr>
<td></td>
<td>BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1<del>2), 16-QAM(36/24Mbps/MCS3</del>4),</td>
</tr>
<tr>
<td></td>
<td>64-QAM(72.2/54/48Mbps/MCS5<del>7), 256-QAM(MCS8</del>9), 1024-QAM(MCS10~11)</td>
</tr>
<tr>
<td><strong>Number of Channels</strong></td>
<td>802.11b: USA, Canada and Taiwan – 1 ~ 11</td>
</tr>
</tbody>
</table>
### Output Power

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2.4G</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11b (11Mbps) @EVM&lt;35%</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11g (54Mbps) @EVM≤-27 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11n (HT20 MCS7) @EVM≤-28 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11n (HT40 MCS7) @EVM≤-28 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>5G</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11a (54Mbps) @EVM≤-25 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11n (HT20 MCS7) @EVM≤-27 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11n (HT40 MCS7) @EVM≤-27 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11ac (VHT20 MCS8) @EVM≤-30 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11ac (VHT40 MCS9) @EVM≤-32 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11ac (VHT80 MCS9) @EVM≤-32 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11ax (HE80 MCS11) @EVM≤-35 dB</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
</tbody>
</table>

### Receiver Sensitivity

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2.4G</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11b (11Mbps)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11g (54Mbps)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11n (HT20 MCS7)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
</tbody>
</table>
### 5G(n/ac packets with LDPC)

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>11a (54Mbps)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11n (HT20 MCS7)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11n (HT40 MCS7)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11ac (VHT20 MCS8)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11ac (VHT40 MCS9)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11ac (VHT80 MCS9)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>11ax (HE80 MCS11)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>dBm</td>
</tr>
</tbody>
</table>

### Data Rate

<table>
<thead>
<tr>
<th>802.11b: 1, 2, 5.5, 11Mbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps</td>
</tr>
<tr>
<td>802.11n: MCS0~7 HT20/HT40</td>
</tr>
<tr>
<td>802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps</td>
</tr>
<tr>
<td>802.11ac: MCS0~8 VHT20</td>
</tr>
<tr>
<td>802.11ac: MCS0~9 VHT40/VHT80</td>
</tr>
<tr>
<td>802.11ax: MCS10~11 HE20/HE40/HE80</td>
</tr>
</tbody>
</table>

### Security

- WEP
- WPA/WPA2/WPA3 Enterprise with 192-bit encryption
- WMM, WMM-PS (U-APSD), WMM-SA
- AES (hardware accelerator),
- TKIP (hardware accelerator)
- CKIP (software support)

* If you have any certification questions about output power please contact FAE directly

### 1.3.3 Bluetooth Features

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bluetooth Standard</td>
<td>Bluetooth 5.2</td>
</tr>
<tr>
<td>Bluetooth VID/PID</td>
<td>N/A</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>2400~2483.5MHz</td>
</tr>
<tr>
<td>Modulation</td>
<td>GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)</td>
</tr>
<tr>
<td>Output Power</td>
<td>Min</td>
</tr>
<tr>
<td>BDR</td>
<td>TBD</td>
</tr>
<tr>
<td>EDR</td>
<td>TBD</td>
</tr>
<tr>
<td>Low Energy (2MHz)</td>
<td>TBD</td>
</tr>
<tr>
<td>Receiver Sensitivity</td>
<td>Min</td>
</tr>
<tr>
<td>BDR</td>
<td>TBD</td>
</tr>
<tr>
<td>EDR</td>
<td>TBD</td>
</tr>
</tbody>
</table>
### 1.3.4 Operating Conditions

<table>
<thead>
<tr>
<th>Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Operating Conditions</strong></td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>3.3V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>Operating Humidity</td>
<td>less than 85% R.H.</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-40°C to 125°C</td>
</tr>
<tr>
<td>Storage Humidity</td>
<td>less than 60% R.H.</td>
</tr>
<tr>
<td><strong>ESD Protection</strong></td>
<td></td>
</tr>
<tr>
<td>Human Body Model</td>
<td>TBD</td>
</tr>
<tr>
<td>Changed Device Model</td>
<td>TBD</td>
</tr>
</tbody>
</table>
2. Pin Definition

2.1 Pin Map

AW-XH316 Pin Map (Top View)
### 2.2 Pin Table

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Definition</th>
<th>Basic Description</th>
<th>Voltage</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>A2</td>
<td>PCIE_RDN</td>
<td>PCIE Receiver Differential Pair Negative Input</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>PCIE_RDP</td>
<td>PCIE Receiver Differential Pair Positive Input</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>A4</td>
<td>PCIE_TDN</td>
<td>PCIE Transmitter Differential Pair Negative Output</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>A5</td>
<td>PCIE_TDP</td>
<td>PCIE Transmitter Differential Pair Positive Output</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>A6</td>
<td>PCIE_REFCLKN</td>
<td>PCIE Differential Pair Clock Source (100 MHz) Negative Input</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>A7</td>
<td>PCIE_REFCLKP</td>
<td>PCIE Differential Pair Clock Source (100 MHz) Positive Input</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>A8</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>A9</td>
<td>CSR_VLX</td>
<td>CSR Power Stage Output to Inductor</td>
<td>0.9V</td>
<td>O</td>
</tr>
<tr>
<td>A10</td>
<td>ASR_VLX</td>
<td>ASR Power Stage Output to Inductor</td>
<td>1.12V</td>
<td>O</td>
</tr>
<tr>
<td>A11</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>B1</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>B2</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>B3</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>B4</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>B5</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>B6</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>B7</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>B9</td>
<td>CSR_VLX</td>
<td>CSR Power Stage Output to Inductor</td>
<td>0.9V</td>
<td>O</td>
</tr>
<tr>
<td>B10</td>
<td>ASR_VLX</td>
<td>ASR Power Stage Output to Inductor</td>
<td>1.12V</td>
<td>O</td>
</tr>
<tr>
<td>B11</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td>GND</td>
</tr>
<tr>
<td>C1</td>
<td>WL_REG_ON</td>
<td>Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW55572 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.</td>
<td>VDDIO</td>
<td>I</td>
</tr>
<tr>
<td>Pin</td>
<td>Description</td>
<td>Voltage</td>
<td>Level</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>-----------------------------------------------------------------------------</td>
<td>---------</td>
<td>--------</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>BT_PCM_IN PCM data input.</td>
<td>VDDIO</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>BT_PCM_SYNC PCM sync; can be master (output) or slave (input), or SLIMbus data.</td>
<td>VDDIO</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>C4</td>
<td>PCIE_CLKREQ_L PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.</td>
<td>VDDIO</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>C5</td>
<td>GND Ground.</td>
<td>GND</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>C6</td>
<td>GND Ground.</td>
<td>GND</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>C7</td>
<td>BT_REG_ON Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW55572 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.</td>
<td>VDDIO</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>C8</td>
<td>GND Ground.</td>
<td>GND</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>C9</td>
<td>GND Ground.</td>
<td>GND</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>C10</td>
<td>VBAT 3.3V power pin</td>
<td>3.3V</td>
<td>VCC</td>
<td></td>
</tr>
<tr>
<td>C11</td>
<td>VBAT 3.3V power pin</td>
<td>3.3V</td>
<td>VCC</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>PCIE_PERST_L PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1</td>
<td>VDDIO</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>GND Ground.</td>
<td>GND</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>GND Ground.</td>
<td>GND</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>BT_PCM_OUT PCM data output.</td>
<td>VDDIO</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td>BT_PCM_CLK PCM clock; can be master (output) or slave (input).</td>
<td>VDDIO</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>PCIE_PME_L PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3</td>
<td>VDDIO</td>
<td>OD</td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>LHL_GPIO3 Miscellaneous General Purpose I/O</td>
<td>VDDIO</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>D8</td>
<td>GND Ground.</td>
<td>GND</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>D9</td>
<td>CBUCK_0P9 Internal Buck 0.9V voltage generation pin.</td>
<td>1.12V</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>D10</td>
<td>CBUCK_0P9 Internal Buck 0.9V voltage generation pin.</td>
<td>1.12V</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>D11</td>
<td>ABUCK_1P12</td>
<td>Internal Buck 1.12V voltage generation pin.</td>
<td>1.12V</td>
<td>I</td>
</tr>
<tr>
<td>-----</td>
<td>-----------</td>
<td>---------------------------------------------</td>
<td>------</td>
<td>---</td>
</tr>
<tr>
<td>E1</td>
<td>GPIO_0_WL_HOST_WAKE</td>
<td>WL Host Wake.</td>
<td>VDDIO</td>
<td>O</td>
</tr>
<tr>
<td>E2</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E3</td>
<td>BT_HOST_WAKE</td>
<td>Bluetooth HOST_WAKE.</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>E4</td>
<td>BT_CLK_REQ</td>
<td>A Bluetooth clock request.</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>E5</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E6</td>
<td>LHL_GPIO4</td>
<td>Miscellaneous General Purpose I/O</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>E7</td>
<td>LPO_IN</td>
<td>External Sleep Clock Input (32.768 kHz)</td>
<td></td>
<td>I</td>
</tr>
<tr>
<td>E8</td>
<td>GPIO_11_WL_UART_T_TX</td>
<td>Debug UART Serial Output.</td>
<td>VDDIO</td>
<td>O</td>
</tr>
<tr>
<td>E9</td>
<td>GPIO_10_WL_UART_T_RX</td>
<td>Debug UART Serial Input.</td>
<td>VDDIO</td>
<td>I</td>
</tr>
<tr>
<td>E10</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E11</td>
<td>ABUCK_1P12</td>
<td>Internal Buck 1.12V voltage generation pin.</td>
<td>1.12V</td>
<td>I</td>
</tr>
<tr>
<td>F1</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F2</td>
<td>BT_DEV_WAKE</td>
<td>Bluetooth DEVICE WAKE</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>F3</td>
<td>BT_UART_TXD</td>
<td>UART Serial Output. Serial data output for the HCI UART interface.</td>
<td>VDDIO</td>
<td>O</td>
</tr>
<tr>
<td>F4</td>
<td>BT_UART_RXD</td>
<td>UART serial input. Serial data input for the HCI UART interface.</td>
<td>VDDIO</td>
<td>I</td>
</tr>
<tr>
<td>F5</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F6</td>
<td>LHL_GPIO2</td>
<td>Miscellaneous General Purpose I/O</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>F7</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F8</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F9</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F10</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F11</td>
<td>VDDIO</td>
<td>1.8 V IO Supply for WLAN GPIOs</td>
<td>VDDIO</td>
<td>VCC</td>
</tr>
<tr>
<td>G1</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>G2</td>
<td>BT_UART_RTS_N</td>
<td>UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.</td>
<td>VDDIO</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td></td>
</tr>
<tr>
<td>G3</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>G4</td>
<td>LHL_GPIO5</td>
<td>Miscellaneous General Purpose I/O</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>G5</td>
<td>BT_UART_CTS_N</td>
<td>UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.</td>
<td>VDDIO</td>
<td>I</td>
</tr>
<tr>
<td>G6</td>
<td>LHL_GPIO0</td>
<td>Miscellaneous General Purpose I/O</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>G7</td>
<td>WL_DEV_WAKE</td>
<td>WL_DEV_WAKE.</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>G8</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>G9</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>G10</td>
<td>GPIO_1</td>
<td>Strap option</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>G11</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>H1</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>H2</td>
<td>SDIO_CMD</td>
<td>SDIO Command Line</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>H3</td>
<td>SDIO_CLK</td>
<td>SDIO Clock Input</td>
<td>VDDIO</td>
<td>I</td>
</tr>
<tr>
<td>H4</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>H5</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>H6</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>H7</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>H8</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>H9</td>
<td>SMIF_SPHB_DQ3</td>
<td>SMIF Data Line 3</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>H10</td>
<td>SMIF_SPHB_DQ1</td>
<td>SMIF Data Line 1</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>H11</td>
<td>SMIF_SPHB_DQ2</td>
<td>SMIF Data Line 0</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>J1</td>
<td>SDIO_DATA_0</td>
<td>SDIO Data Line 0</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>J2</td>
<td>SDIO_DATA_3</td>
<td>SDIO Data Line 3</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>J3</td>
<td>SDIO_DATA_2</td>
<td>SDIO Data Line 2</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>J4</td>
<td>SDIO_DATA_1</td>
<td>SDIO Data Line 1</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>J5</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>----------</td>
<td>-------------------------------------------------------</td>
<td>---</td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>J8</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>J9</td>
<td>SMIF_SPHB_CS0_N</td>
<td>SMIF Chip Select0 Active-low Output</td>
<td>VDDIO</td>
<td>O</td>
</tr>
<tr>
<td>J10</td>
<td>SMIF_SPHB_CK</td>
<td>SMIF Clock Output</td>
<td>VDDIO</td>
<td>O</td>
</tr>
<tr>
<td>J11</td>
<td>SMIF_SPHB_DQ0</td>
<td>SMIF Data Line 0</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>K1</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K2</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K3</td>
<td>BT_GPIO_11</td>
<td>BT General Purpose I/O</td>
<td>VDDIO</td>
<td>I/O</td>
</tr>
<tr>
<td>K4</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K5</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K6</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K7</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K8</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K9</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K10</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>K11</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>NC</td>
<td>Floating Pin, No connect to anything.</td>
<td>Floating</td>
<td></td>
</tr>
<tr>
<td>L2</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>L3</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>L4</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>L5</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>L6</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>L7</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>L8</td>
<td>GND</td>
<td>Ground.</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L9</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L10</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L11</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M3</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M4</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M5</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M6</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M7</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M8</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M9</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M10</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M11</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N1</td>
<td>C0_ANT</td>
<td>WLAN/BT Main RF TX/RX path.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N2</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N3</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N4</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N5</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N6</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N7</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N8</td>
<td>C1_ANT</td>
<td>WLAN/BT Aux RF TX/RX path.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N9</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N10</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N11</td>
<td>GND</td>
<td>Ground.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 2.3 Host Configuration Interface Table

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Definition</th>
<th>Interface</th>
<th>Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>G10</td>
<td>GPIO_1</td>
<td>PCIE</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDIO</td>
<td>0</td>
</tr>
</tbody>
</table>
# Electrical Characteristics

## 3.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBAT</td>
<td>DC supply for the VBAT and PA driver supply</td>
<td>-0.5</td>
<td>-</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>VDDIO</td>
<td>DC supply voltage for digital I/O</td>
<td>-0.5</td>
<td>-</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>Tj</td>
<td>Maximum junction temperature</td>
<td>-</td>
<td>-</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

## 3.2 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBAT</td>
<td>Power supply for Internal Regulator</td>
<td>3.0</td>
<td>3.3</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td>VDDIO</td>
<td>DC supply voltage for digital I/O</td>
<td>1.71</td>
<td>1.8</td>
<td>1.89</td>
<td>V</td>
</tr>
</tbody>
</table>

## 3.3 Digital IO Pin DC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital I/O pins, VDDIO=1.8V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>Input high voltage</td>
<td>0.65 × VDDIO</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input low voltage</td>
<td>-</td>
<td>-</td>
<td>0.35 × VDDIO</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output high voltage</td>
<td>VDDIO – 0.45</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>-</td>
<td>-</td>
<td>0.45</td>
<td>V</td>
</tr>
</tbody>
</table>
3.4 Host Interface

3.4.1 SDIO Interface

SDIO Bus Timing (Default Mode)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDIO CLK (All values are referred to minimum VIH and maximum VIL)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency – Data Transfer mode</td>
<td>$f_{PP}$</td>
<td>0</td>
<td>–</td>
<td>25</td>
<td>MHz</td>
</tr>
<tr>
<td>Frequency – Identification mode</td>
<td>$f_{OD}$</td>
<td>0</td>
<td>–</td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>Clock low time</td>
<td>$t_{WL}$</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Clock high time</td>
<td>$t_{WH}$</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Clock rise time</td>
<td>$t_{TLH}$</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Clock low time</td>
<td>$t_{THL}$</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Inputs: CMD, DAT (referenced to CLK)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input setup time</td>
<td>$t_{ISU}$</td>
<td>5</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Input hold time</td>
<td>$t_{IH}$</td>
<td>5</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Outputs: CMD, DAT (referenced to CLK)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Output delay time – Data Transfer mode
\[ t_{\text{ODLY}} \quad 0 \quad - \quad 14 \quad \text{ns} \]
Output delay time – Identification mode
\[ t_{\text{ODLY}} \quad 0 \quad - \quad 50 \quad \text{ns} \]

SDIO Bus Timing (High-Speed Mode)

SDIO Bus Timing Parameters (High-Speed Mode)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDIO CLK (all values are referred to minimum VIH and maximum VIL(^\text{b}))</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency – Data Transfer Mode</td>
<td>( f_{\text{PP}} )</td>
<td>0</td>
<td>-</td>
<td>50</td>
<td>MHz</td>
</tr>
<tr>
<td>Frequency – Identification Mode</td>
<td>( f_{\text{OD}} )</td>
<td>0</td>
<td>-</td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>Clock low time</td>
<td>( t_{\text{WL}} )</td>
<td>7</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Clock high time</td>
<td>( t_{\text{WH}} )</td>
<td>7</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Clock rise time</td>
<td>( t_{\text{TLH}} )</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>ns</td>
</tr>
<tr>
<td>Clock low time</td>
<td>( t_{\text{THL}} )</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>ns</td>
</tr>
</tbody>
</table>

Inputs: CMD, DAT (referenced to CLK)

| Input setup Time       | \( t_{\text{ISU}} \) | 6 | - | - | ns |
| Input hold Time        | \( t_{\text{IH}} \) | 2 | - | - | ns |

Outputs: CMD, DAT (referenced to CLK)
<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Value</th>
<th>Notes</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output delay time – Data Transfer Mode</td>
<td>$t_{ODLY}$</td>
<td>–</td>
<td>–</td>
<td>14</td>
</tr>
<tr>
<td>Output hold time</td>
<td>$t_{OH}$</td>
<td>2.5</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Total system capacitance (each line)</td>
<td>$CL$</td>
<td>–</td>
<td>–</td>
<td>40</td>
</tr>
</tbody>
</table>
3.4.2 UART Interface

The AW-XH316 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.0 UART HCI specification. The default baud rate is 115.2 Kbaud.

The AW-XH316 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-XH316 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

UART Interface Signals

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3</td>
<td>BT_UART_TXD</td>
<td>Bluetooth UART Serial Output. Serial data output for the HCI UART Interface</td>
<td>O</td>
</tr>
<tr>
<td>F4</td>
<td>BT_UART_RXD</td>
<td>Bluetooth UART Series Input. Serial data input for the HCI UART Interface</td>
<td>I</td>
</tr>
<tr>
<td>G2</td>
<td>BT_UART_RTS_N</td>
<td>Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface.</td>
<td>O</td>
</tr>
<tr>
<td>G5</td>
<td>BT_UART_CTS_N</td>
<td>Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td>Reference Characteristics</td>
<td>Minimum</td>
<td>Typical</td>
</tr>
<tr>
<td>---</td>
<td>------------------------------------------------------------------------------------------</td>
<td>---------</td>
<td>---------</td>
</tr>
<tr>
<td>1</td>
<td>Delay time, BT_UART_CTS_N low to BT_UART_TXD valid</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>2</td>
<td>Setup time, BT_UART_CTS_N high before midpoint of stop bit</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>3</td>
<td>Delay time, midpoint of stop bit to BT_UART_RTS_N high</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
3.4.3 PCIe Interface

The PCI Express (PCIe) core in AW-XH316 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen2 speeds. This core contains all the necessary blocks, including logical and electrical functional sub blocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 20. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and AW-XH316 device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.
3.5 Power up Timing Sequence

AW-XH316 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals

■ **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-XH316 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

■ **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal AW-XH316 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note

■ AW-XH316 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating PCIe accesses.

■ VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
WLAN = ON, Bluetooth = ON

WLAN = OFF, Bluetooth = OFF
**WLAN = ON, Bluetooth = OFF**

**WLAN = OFF, Bluetooth = ON**
WLAN Boot-Up Sequence for SDIO Host

WLAN Power-Up Sequence for PCIe Host
3.6 Power Consumption

3.6.1 WLAN
TBD
* The power consumption is based on Azurewave test environment, these data for reference only.

3.6.2 Bluetooth
TBD
* The power consumption is based on Azurewave test environment, these data for reference only.
4. Mechanical Information

4.1 Mechanical Drawing

TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.01mm
5. Packaging Information

TBD