AW-CU544

IEEE 802.11 b/g/n MAC/baseband/radio and Bluetooth 5.2 IoT Module

Layout Guide

Rev. A

(For Standard)
## Revision History

<table>
<thead>
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<th>Version</th>
<th>Revision Date</th>
<th>Description</th>
<th>Initials</th>
<th>Approved</th>
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<td>A</td>
<td>2022/11/06</td>
<td>• Initial Version</td>
<td>Steven Jian</td>
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Table of Contents

Revision History .................................................................................................................................................. 2
Table of Contents ............................................................................................................................................... 3
List of Figures .................................................................................................................................................. 3
1. Layout guide ................................................................................................................................................ 4
   1.1 Power & Digital Signal ............................................................................................................................ 4
   1.2 Antenna .................................................................................................................................................. 4
   1.3 Recommended PCB Footprint .................................................................................................................. 7

List of Figures

Figure 1............................................................................................................................................................ 5
Figure 2............................................................................................................................................................ 5
Figure 3............................................................................................................................................................ 6
Figure 4............................................................................................................................................................ 7
1. Layout guide

1.1 Power & Digital Signal

- **Pin E1 and F1** are the main power line for CYW43438. Keep its impedance as low as possible. Recommended trace width > 20mils. **DO NOT use Coin Cells for this rail. They are designed for low power device (<10mA), whereas the CYW43438 can consume up to 300mA average current.**
- Make sure every power traces have good return path (ground path).
- **High speed digital** traces shall have **equal electrical length within their respective group.** Keep them **away from noise sensitive blocks (e.g. antenna, CapSense and power traces).**
- Good return path and well shielded signal can reduce crosstalk, EMI emission and improve signal integrity.
- Traces for CapSense function should be short and narrow (recommend use Port 8 for its low self-capacitance traces inside the module).
- Use mutual-capacitance sensing method so that the sensitivity is not degraded because of high self-capacitance of the trace (refer to AN85951 - PSoC® 4 and PSoC® 6 MCU CapSense® Design Guide)

1.2 Antenna

- **P + Q > 20mm**
- **R = 7.65mm**
- Keep out distance (XYZ direction) “S” of the print antenna is > 10mm for non-conductive materials (e.g. plastic case) & 20mm for conductive materials (e.g. cables & connectors)
- Do not extend main board PCB outline to the antenna area.
- Above is the general guideline. Contact us if it does not fit your design.
1.3 Recommended PCB Footprint

Figure 4

- Recommended PCB Layout Footprint (Unit in mm Dia=0.75mm Solder Mask Defined)