AzureWave Technologies, Inc.

AW-CM256SM

IEEE 802.11a/b/g/n/ac Wi-Fi with Bluetooth

Combo Stamp LGA Module

Datasheet

Rev. D

0BH

(For Standard)

Features

WLAN

- High speed wireless connection up to 433.3Mbps transmit/receive PHY rate using 80MHz bandwidth
- 1 antennas to support 1(Transmit) × 1(Receive) technology and Bluetooth
- WCS (Wireless Coexistence System)
- Low power consumption and high performance
- Enhanced wireless security
- Fully speed operation with Piconet and Scatternet support
- 12mm(L) x 12mm(W) x1.7mm(H)　LGA package
- Dual - band 2.4 GHz and 5GHz 802.11 a/b/g/n/ac
- **External Crystal**

Bluetooth

- 1 antennas to support 1(Transmit) × 1(Receive) technology and Bluetooth
- Fully qualified Bluetooth BT4.2
- Compliant Bluetooth BT5.3
- Enhanced Data Rate(EDR) compliant for both 2Mbps and 3Mbps supported
- High speed UART and PCM for Bluetooth

Revision History

Document NO: R2-2256SM-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/07/14	DCN017658	● Initial release	Licheng Wang	Chihhao Liao
B	2021/03/23	DCN021165	● Change document format	Licheng Wang	Chihhao Liao
C	2021/04/21	DCN021634	● Update IC description.	Licheng Wang	Chihhao Liao
D	2022/04/07	DCN025882	● Update BT specification table.	Licheng Wang	Chihhao Liao

Table of Contents

1. Introduction

1.1 Product Overview

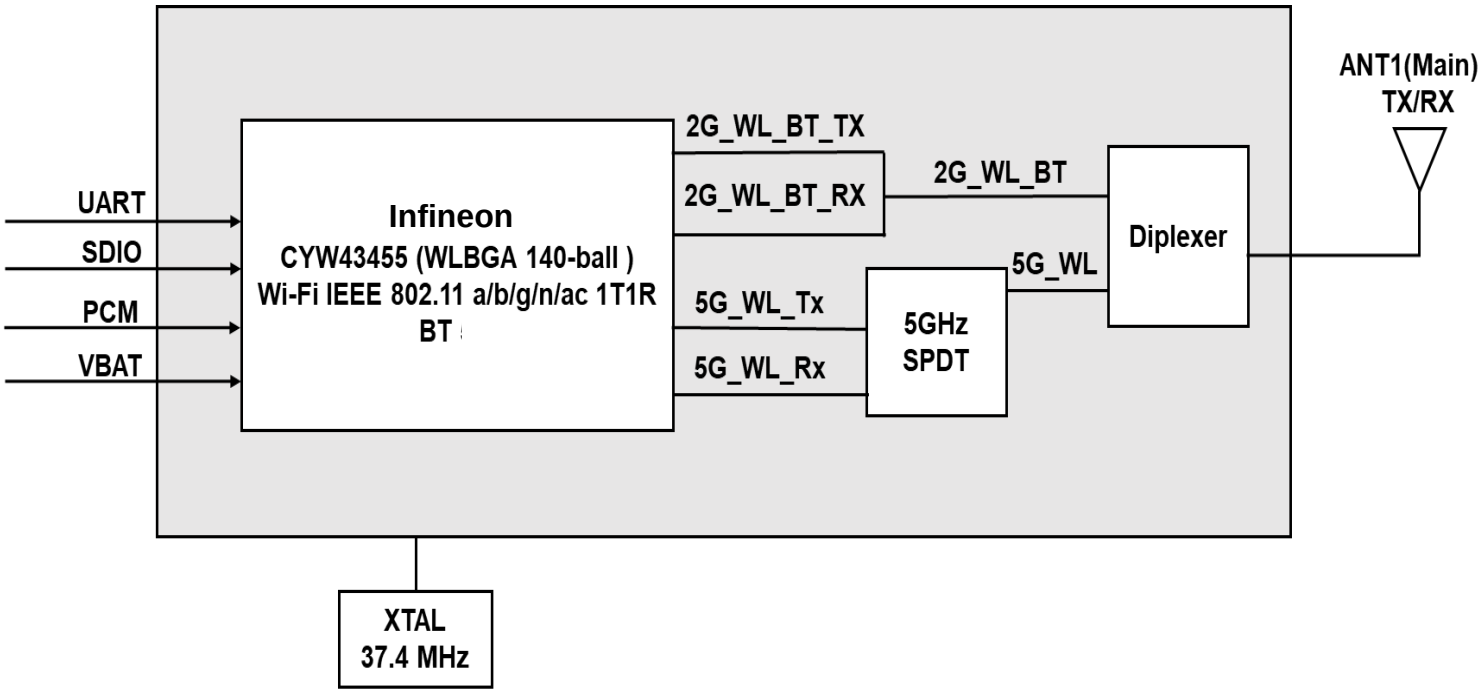
AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.11 a/b/g/n/ac WIFI with Bluetooth 5.0 combo SDIO and UART Stamp LGA Module --- **AW-CM256SM.** The AW-CM256SM IEEE 802.11 a/b/g/n/ac WIFI with Bluetooth 5.0 combo module is a highly integrated wireless local area network (WLAN) solution to let users enjoy the digital content through the latest wireless technology without using the extra cables and cords. It combines with Bluetooth 5.0 and provides a complete 2.4GHz Bluetooth system which is fully compliant to Bluetooth 5.0 and v2.1 that supports EDR of 2Mbps and 3Mbps for data and audio communications. It enables a high performance, cost effective, low power, compact solution that easily fits onto the SDIO and UART combo stamp LGA module.

Compliant with the IEEE 802.11a/b/g/n/ac standard, AW-CM256SM uses Direct Sequence Spread Spectrum (DSSS), Orthogonal Frequency Division Multiplexing (OFDM), BPSK, QPSK, CCK and QAM baseband modulation technologies.

Compare to 802.11n technology, 802.11ac standard makes big improvement on speed and range.

AW-CM256SM module adopts Infineon solution. The module design is based on the Infineon CYW43455 single chip.

1.2 Block Diagram



AW- CM256SM Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11a/b/g/n/ac Wi-Fi with Bluetooth 5.0 Combo Stamp LGA Module
Major Chipset	CYW43455 (WLBGA 140-ball)
Host Interface	Wi-Fi+BT SDIO+UART
Dimension	12 mm X 12 mm x 1.7 mm
Form factor	Stamp LGA Module 44 pin
Antenna	1T1R for WiFi/BT ANT1(Main)：WiFi/Bluetooth → TX/RX
Weight	0.45g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac 1T1R
WLAN VID/PID	1A3B / 2256
WLAN SVID/SPID	NA
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	802.11a/g/n/ac: OFDM 802.11b: CCK(11, 5.5Mbps), DQPSK(2Mbps), BPSK(1Mbps)
Number of Channels	**2.4GHz** ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13 **5GHz** USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

Output Power (Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<35%	16.5	18	19.5	dBm
11g (54Mbps) @EVM≦-27 dB	14.5	16	17.5	dBm
11n (HT20 MCS7) @EVM≦-28 dB	13.5	15	16.5	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM≦-27 dB	13.5	15	16.5	dBm
11n (HT20 MCS7) @EVM≦-28 dB	13.5	15	16.5	dBm
11n (HT40 MCS7) @EVM≦-28 dB	11.5	13	14.5	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	12.5	14	15.5	dBm
11ac (VHT40 MCS9) @EVM≦-32 dB	11.5	13	14.5	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	10.5	12	13.5	dBm

Receiver Sensitivity

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-87	-84	dBm
11g (54Mbps)		-76	-73	dBm
11n (HT20 MCS7)		-74	-71	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		-73	-70	dBm
11n (HT20 MCS7)		-71	-68	dBm
11n (HT40 MCS7)		-68	-65	dBm
11ac (VHT20 MCS8)		-66	-63	dBm
11ac (VHT40 MCS9)		-63	-60	dBm
11ac (VHT80 MCS9)		-59	-56	dBm

Data Rate

- 802.11b: 1, 2, 5.5, 11Mbps
- 802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- 802.11n: up to 86.7Mbps-single
- 802.11ac:up to 86.7Mbps (20MHz channel)
- 802.11ac:up to 200Mbps (40MHz channel)
- 802.11ac:up to 433Mbps (80MHz channel)

Security	■ WPA and WPA2(Personal) support for powerful encryption and authentication. ■ AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility. ■ Reference WLAN subsystem provides Cisco Compatible Extensions(CCX, CCX2.0, CCX3.0 and CCX4.0). ■ Reference WLAN subsystem provides Wi-Fi Protected Setup(WPS).

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 5.3 (Core Specification)</td></tr>
<tr><td>Bluetooth VID/PID</td><td>NA</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK
Payload 2M: 4-DQPSK
Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>(Conductive)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>GFSK</td><td></td><td>10</td><td>12</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>BT5.0+Enhanced Data Rate (EDR)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>GFSK</td><td></td><td>-86</td><td>-70</td><td>dBm</td></tr>
<tr><td>4-DQPSK</td><td></td><td>-86</td><td>-70</td><td>dBm</td></tr>
<tr><td>8DPSK</td><td></td><td>-80</td><td>-70</td><td>dBm</td></tr>
</table></td></tr>
</table>

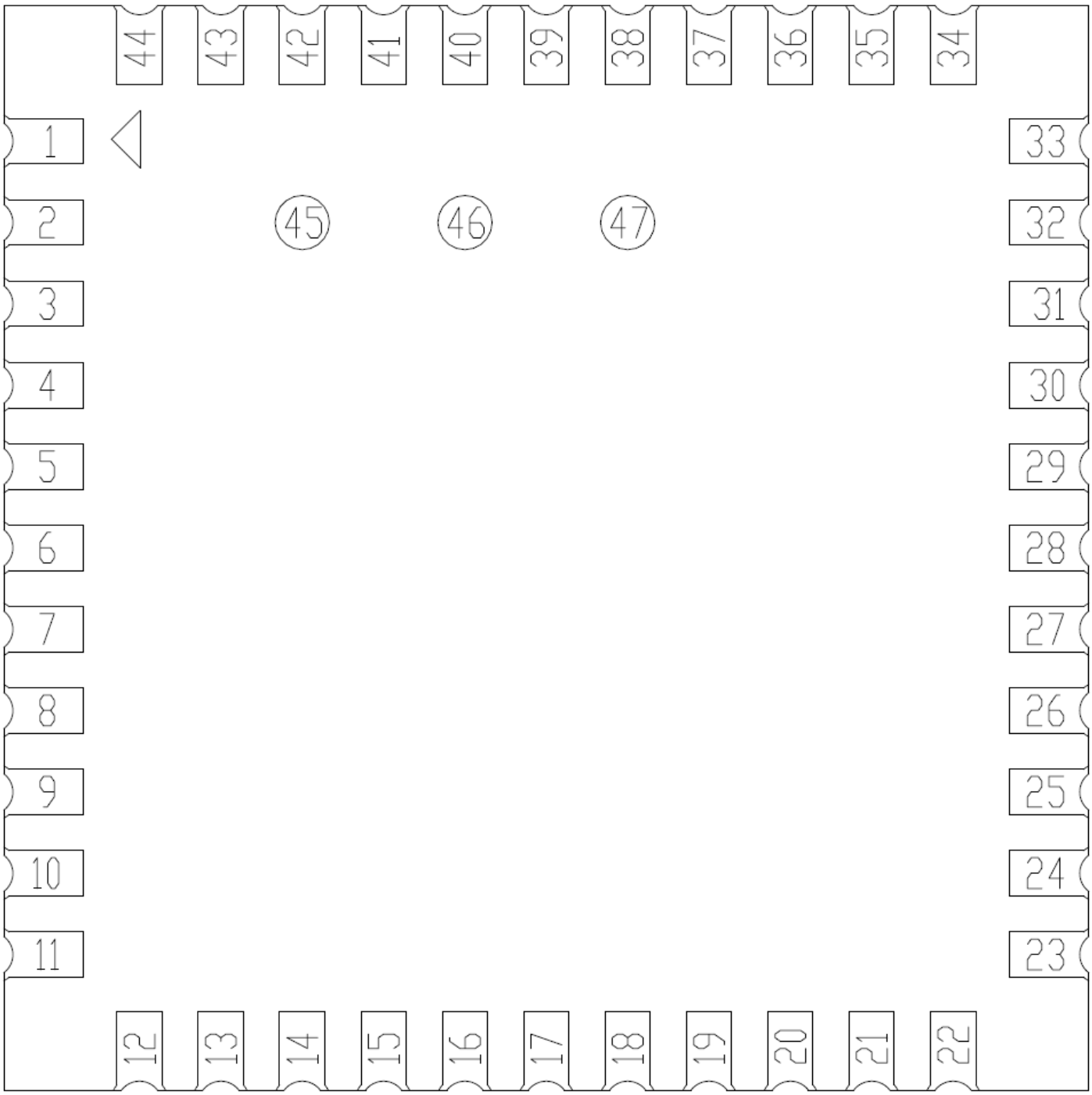
1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT: 3.2 ~ 4.8V ; typical: 3.6V VIO : 1.71 ~ 3.63V
Operating Temperature	-30℃ to +85℃[1]
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃ to +105℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	1KV per JEDEC EID/JESD22-A114
Changed Device Model	250V per JEDEC EIA/JESD22-C101

[1] Functionality is guaranteed across this ambient temperature range. Optimal RF performance specified in the data sheet, however, is guaranteed only for -20 °C to 75 °C.

2. Pin Definition

2.1 Pin Map



AW-CM256SM Top View Pin Map

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
3	GND	Ground.		GND
4	NC	Floating Pin, No connect to anything.		Floating
5	NC	Floating Pin, No connect to anything.		Floating
6	BT_WAKE	BT Device Wake		I
7	BT_HOSTWAKE	BT Host Wake		O
8	NC	Floating Pin, No connect to anything.		Floating
9	VBAT	3.3V power pin	3.3V	VCC
10	XTAL_IN	Crystal Input(37.4MHz)		I
11	XTAL_OUT	Crystal Output(37.4MHz)		O
12	WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.		I
13	WL_SDIO_HOST WAKE	WL Host Wake		O
14	SDIO_DATA2	SDIO Data Line 2		I/O
15	SDIO_DATA3	SDIO Data Line 3		I/O
16	SDIO_CMD	SDIO Command Input		I/O
17	SDIO_CLK	SDIO Clock Input		I
18	SDIO_DATA0	SDIO Data Line 0		I/O
19	SDIO_DATA1	SDIO Data Line 1		I/O
20	GND	Ground.		GND
21	VIN_LDO_OUT	Internal Buck voltage generation pin	1.35V(typ)	VCC

22	VDDIO	1.8V-3.3V VDDIO supply for WLAN and BT	VIO	VCC
23	VIN_LDO	Internal Buck voltage generation pin	1.35V(typ)	VCC
24	SUSCLK_IN	External 32K or RTC clock		I
25	BT_PCM_OUT	PCM data Out		O
26	BT_PCM_CLK	PCM Clock		I/O
27	BT_PCM_IN	PCM data Input		I
28	BT_PCM_SYNC	PCM Synchronization control		I/O
29	GPIO_7	SDIO mode selection pin 1.8V:pull up, connect to 1.8V 3.3V:pull down, connect to GND with using a 10K resistor or less		I
30	GPIO_4	GPIO configuration pin		I/O
31	GND	Ground.		GND
32	NC	Floating Pin, No connect to anything.		Floating
33	GND	Ground.		GND
34	BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.		I
35	NC	Floating Pin, No connect to anything.		Floating
36	GND	Ground.		GND
37	GPIO_6	GPIO configuration pin		I/O
38	GPIO_3	GPIO configuration pin		I/O
39	GPIO_5	GPIO configuration pin		I/O
40	GPIO_2	GPIO configuration pin		I/O
41	BT_UART_RTS_N	High-Speed UART RTS		O
42	BT_UART_TXD	High-Speed UART Data Out		O
43	BT_UART_RXD	High-Speed UART Data In		I

44	BT_UART_CTS_N	High-Speed UART CTS		I
45	NC	Floating Pin, No connect to anything.		Floating
46	NC	Floating Pin, No connect to anything.		Floating
47	NC	Floating Pin, No connect to anything.		Floating

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	-0.5	-	+6.0	V
VDDIO	DC supply voltage for digital I/O	-0.5	-	+3.9	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for the internal regulators and FEM	3.2	3.6	4.8	V
VDDIO	DC supply voltage for digital I/O	1.71	-	+3.63	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO=1.8V					
VIH	Input high voltage (VDDIO)	1.17	-	-	V
VIL	Input low voltage (VDDIO)	-	-	0.63	V
VOH	Output High Voltage @ 2mA	1.35	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V
VDDIO=3.3V					
VIH	Input high voltage (V_{DDIO})	2.0	-	-	V
VIL	Input low voltage (V_{DDIO})	-	-	0.8	V
VOH	Output High Voltage @ 2mA	2.9	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.4	V

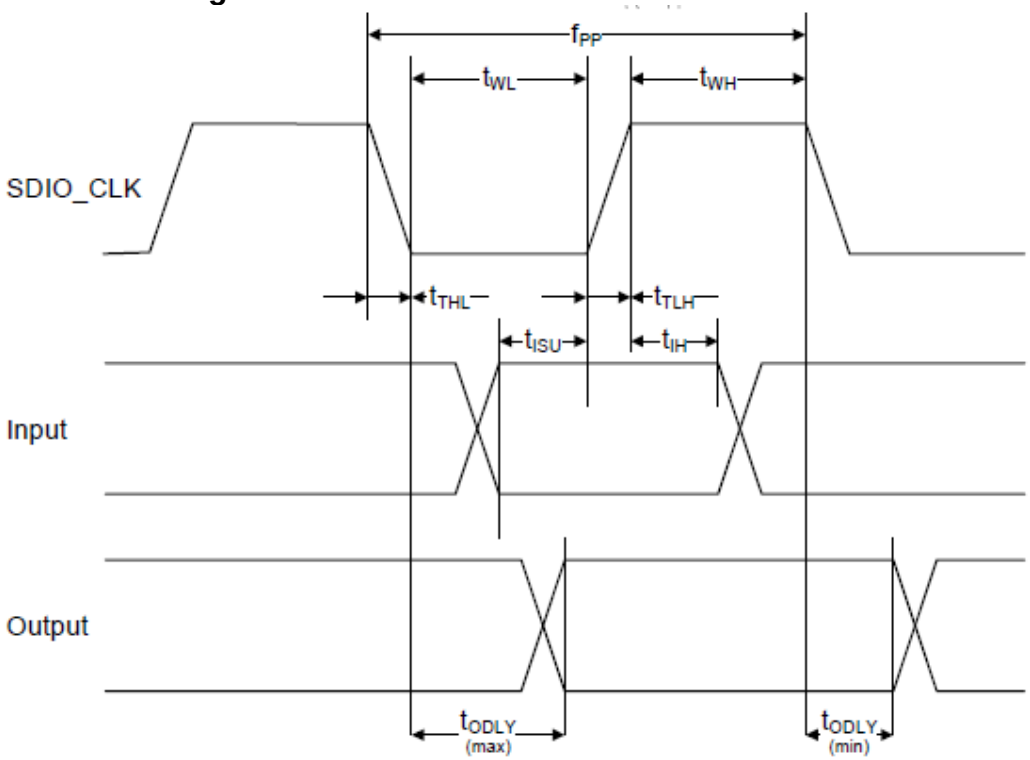
3.4 Host Interface

3.4.1 SDIO Interface

AW-CM256SM support for SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25MHz, including 1- and 4-bit modes (3.3V signaling).
- HS: High speed up to 50 MHz (3.3V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).
- SDR50: SDR up to 100 MHz (1.8V signaling).
- SDR104: SDR up to 208MHz (1.8V signaling).
- DDR50: DDR up to 50 MHz (1.8V signaling).

SDIO Default Mode Timing



SDIO Timing Data(Default Mode)

Symbol	Parameter	Condition	Min	Max	Units
f_{pp}	CLK Frequency	Normal	0	25	MHz
		High Speed	0	50	
t_{WH}	CLK High Time	Normal	10	-	ns
		High Speed	7	-	
t_{WL}	CLK Low Time	Normal	10	-	
		High Speed	7	-	
tTLH	CLK rise Time	Normal	-	10	
		High Speed	-	3	
tTHL	CLK fall Time	Normal	-	10	
		High Speed	-	3	
t_{ISU}	Input Setup Time	Normal	5	-	
		High Speed	6	-	
t_{IH}	Input Hold Time	Normal	5	-	
		High Speed	2	-	
t_{ODLY}	Output Delay Time	Normal	-	14	
		High Speed	-	14	

3.4.2 UART Interface

The AW-CM256SM shares a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

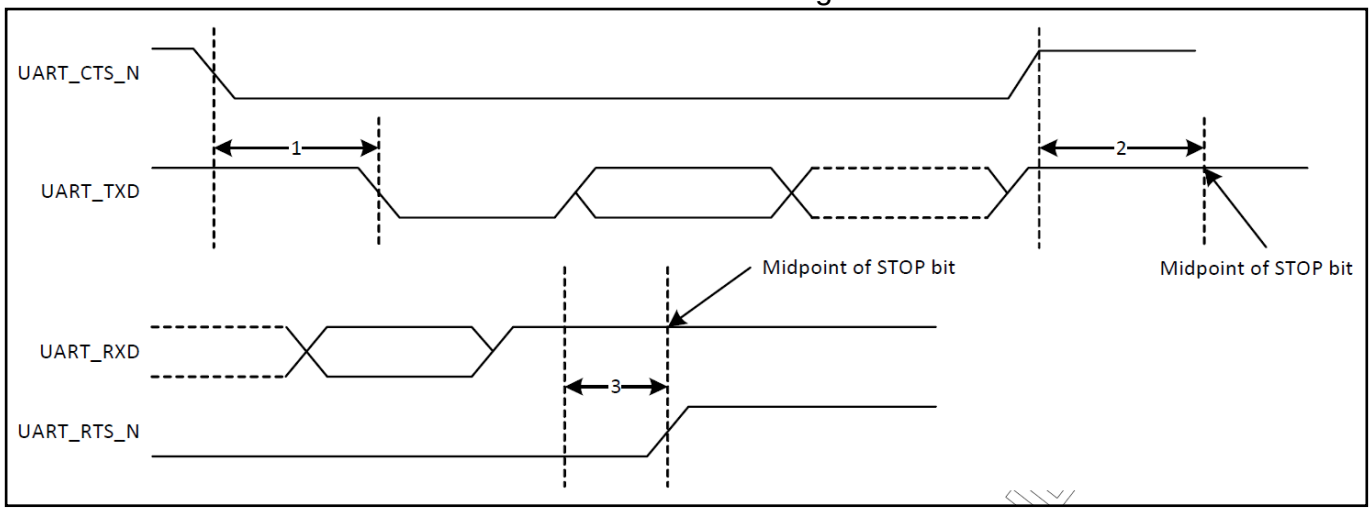
UART has a 1040-byte receive FIFO and a 1040-byte transmits FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud. The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals. Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-CM256SM UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

UART Interface Signals

PIN No.	Name	Description	Type
42	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	O
43	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	I
41	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	O
44	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	I

UART Timing

UART Timing



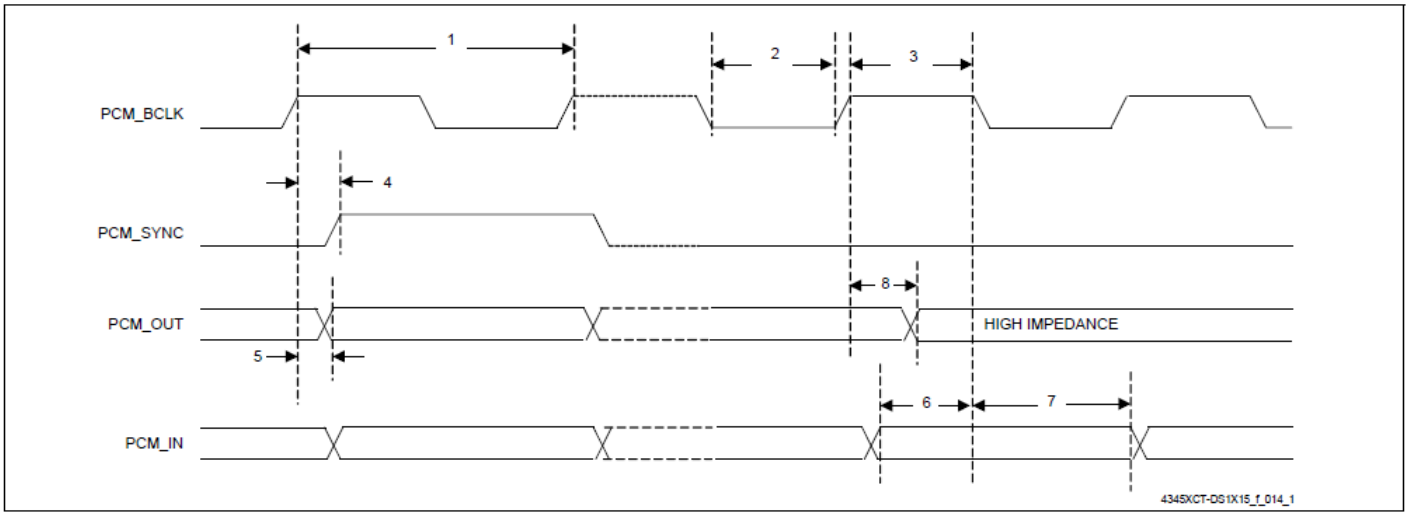
UART Timing Specifications

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

3.4.3 PCM Interface Timing

3.4.3.1 Short Frame Sync, Master Mode

PCM Timing Diagram (Short Frame Sync, Master Mode)

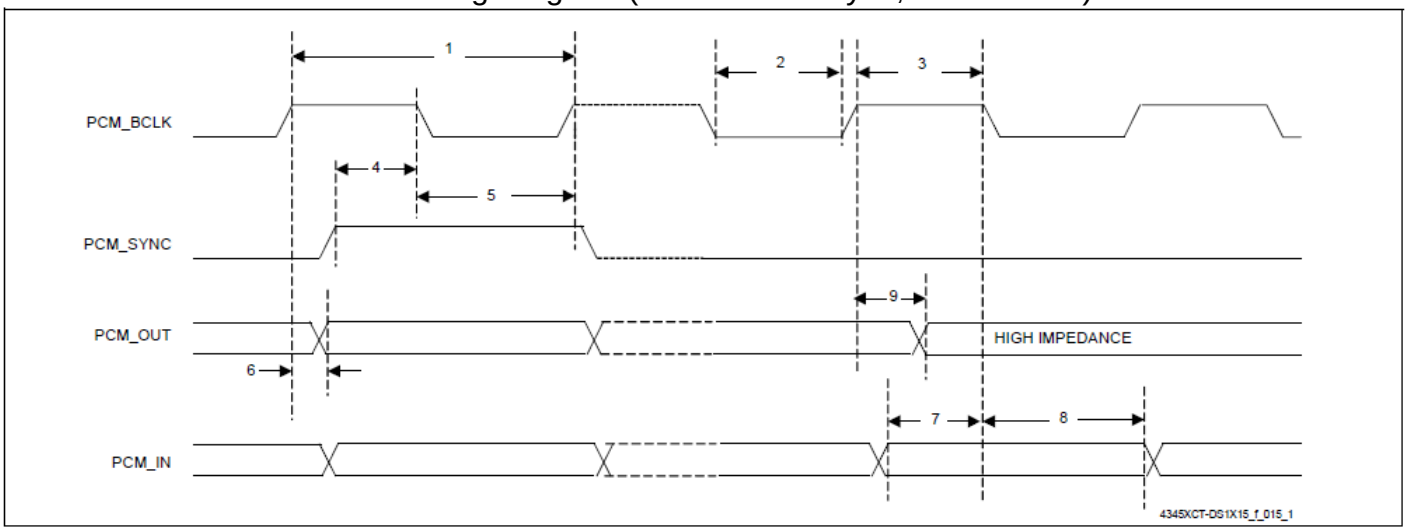


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

3.4.3.2 Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

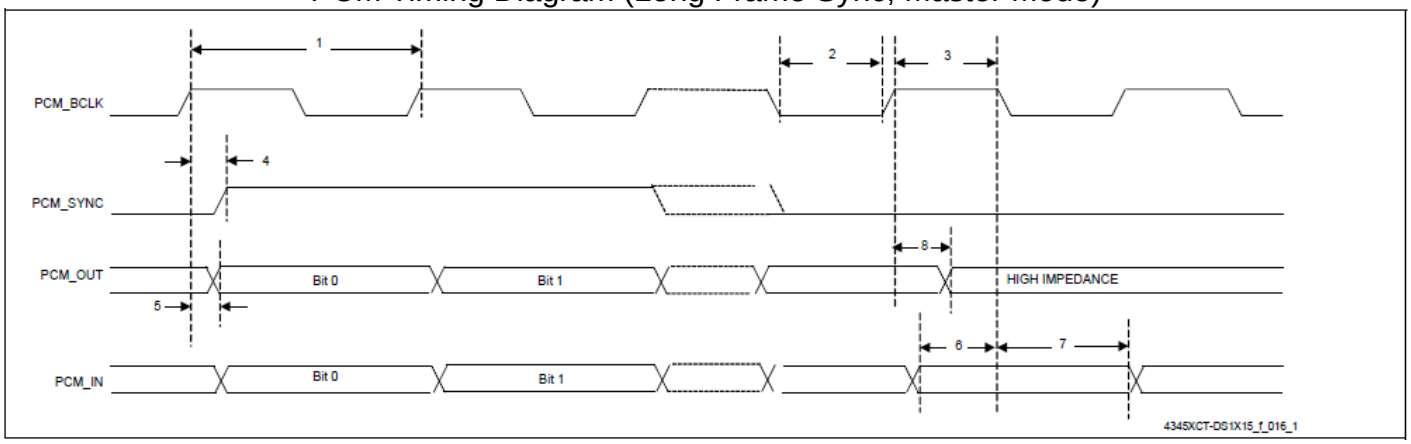


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

3.4.3.3 Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)



PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
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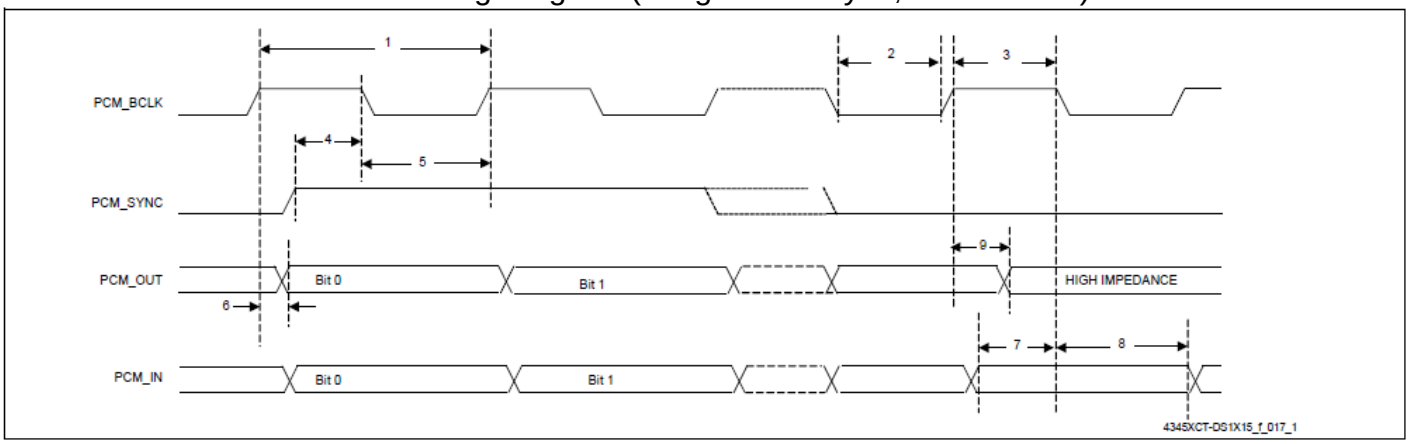
3.4.3.4 Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
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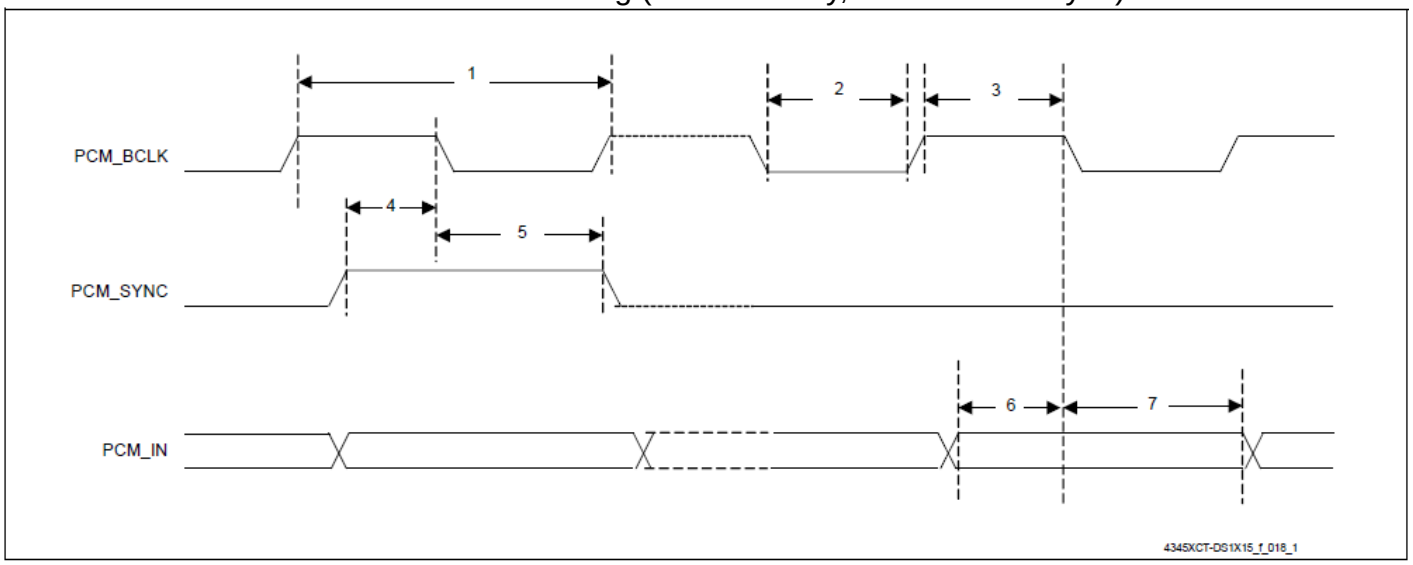
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

3.4.3.5 Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

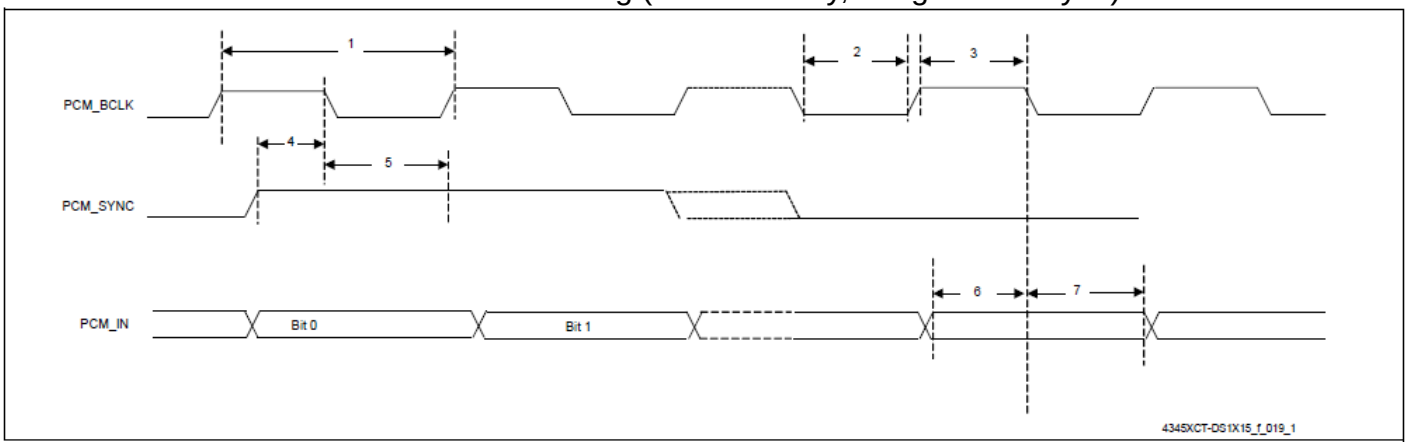


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

3.4.3.6 Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

3.5 Power up Timing Sequence

The AW-CM256SM has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Note:

- The WL_REG_ON and BT_REG_ON signals are ORed in the AW-CM256SM. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the AW-CM256SM regulators.
- The AW-CM256SM has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

Description of Control Signals

The AW-CM256SM has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption.

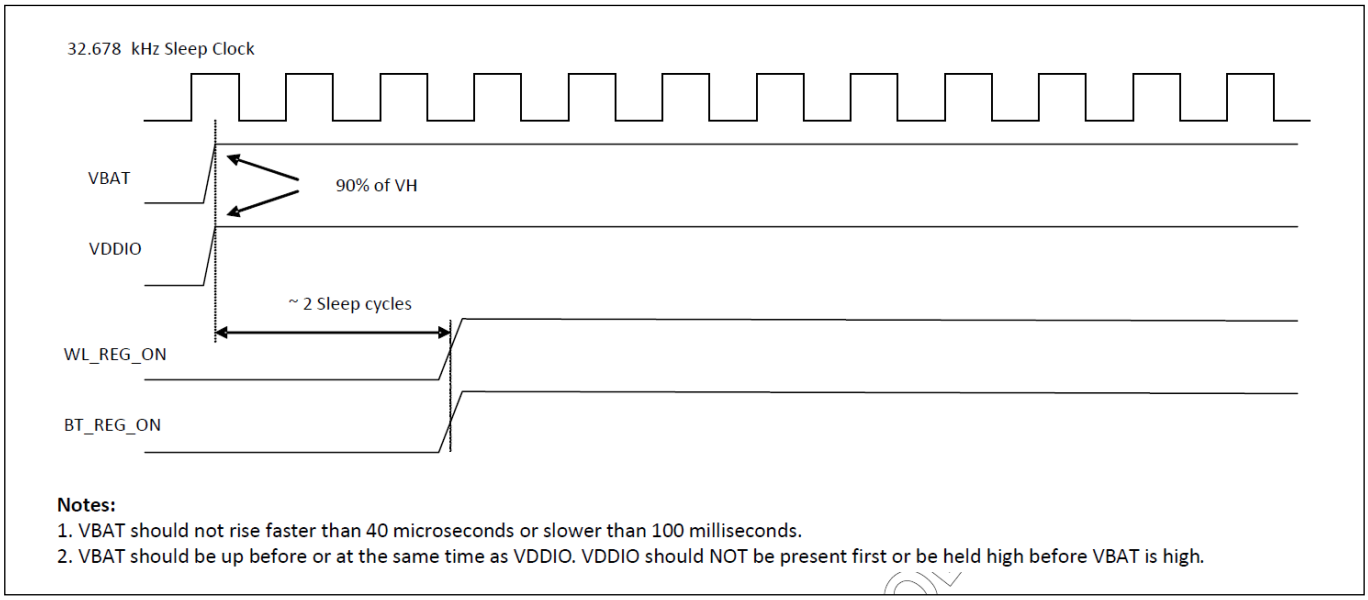
Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also ORgated with the BT_REG_ON input to control the internal AW-NMNF regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal AW-CM256SM regulators. If both BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

Note: For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 msec time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

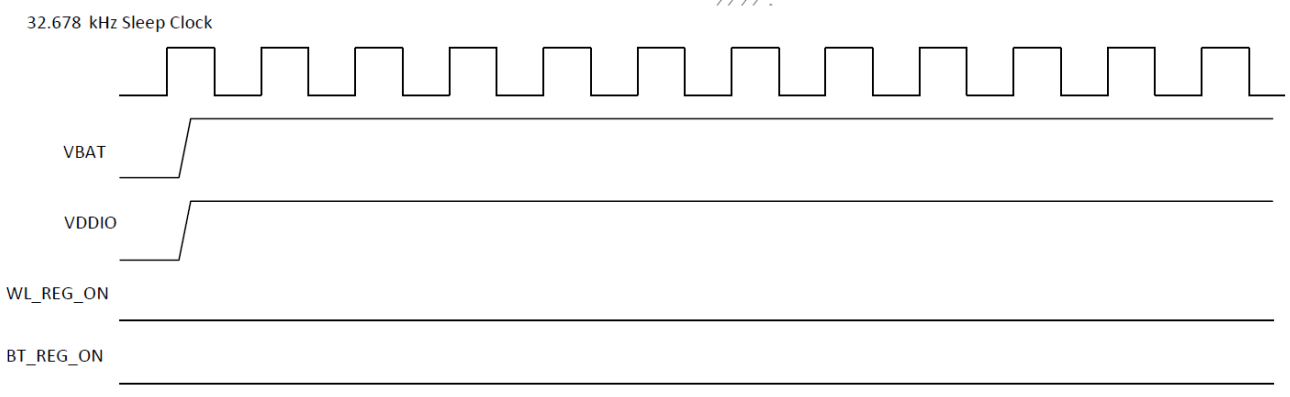
Control Signal Timing Diagrams

WLAN = ON, Bluetooth = ON



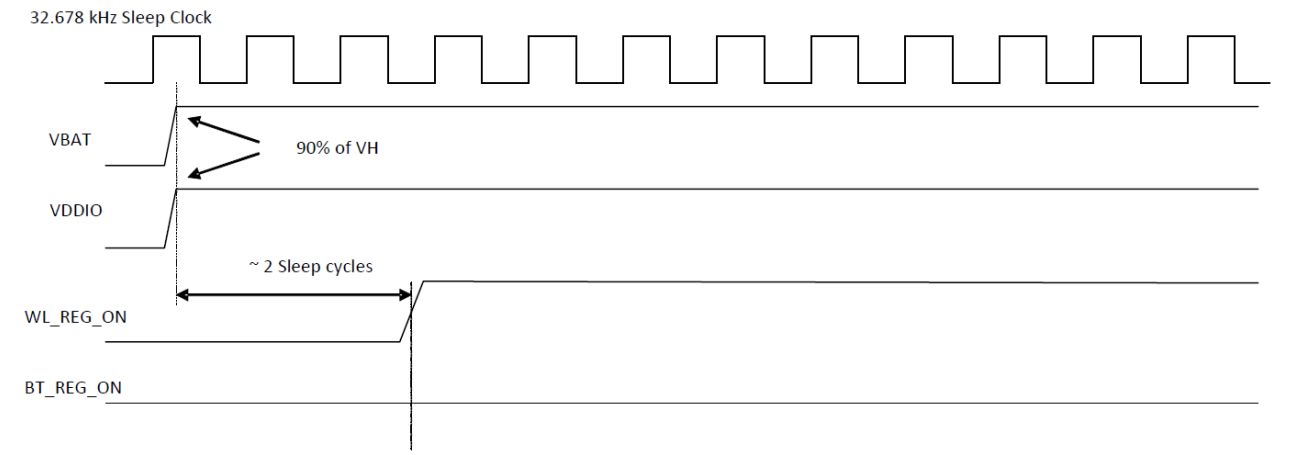
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF



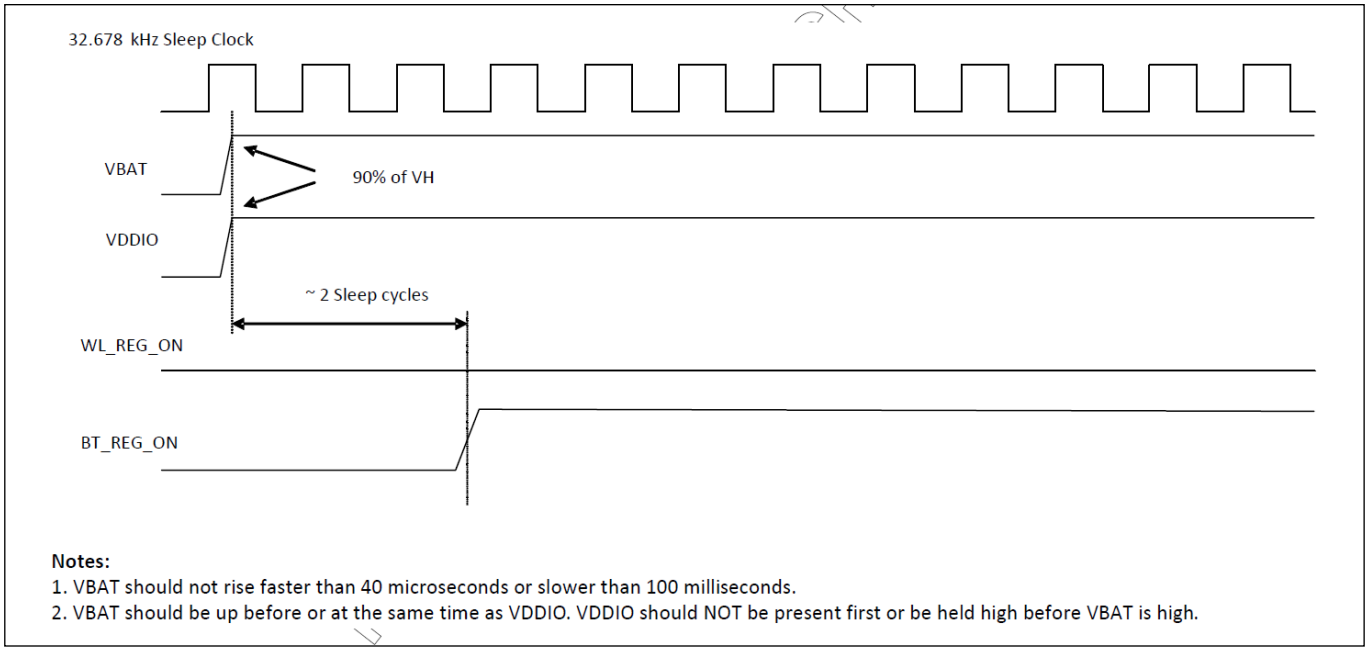
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = ON



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

3.6 Power Consumption*

3.6.1 WLAN

Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit (VBAT_IN=3.6 V)	Receive (VBAT_IN=3.6 V)
				Avg.	Avg.
2.4	11b@1Mbps	20	18	339.5 mA	50.4mA
	11g@54Mbps	20	16	165.8mA	53.0 mA
	11n@MCS7	20	15	247.7mA	53.2mA
	11n@MCS7	40	14	212.6mA	63.2mA
5	11a@54Mbps	20	15	280.1mA	69.1mA
	11n@MCS7	20	15	234.3mA	69.2mA
	11n@MCS7	40	13	204.3mA	78.4mA
	11ac@MCS9 NSS1	80	12	201.2mA	103.9mA

* The power consumption is based on Azurewave test environment, these data for reference only.

3.6.2 Bluetooth

No.	Mode	Packet Type	VBAT_IN=3.3 V
			Avg.
1	Transmit	DH5	31.7mA
2	Receive	3-DH5	23.1mA

* The power consumption is based on Azurewave test environment, these data for reference only.

3.7 Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

The AW-CM256SM uses a secondary low frequency clock for low-power-mode timing. Either the internal low- precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake-up earlier to avoid missing beacons. Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in below.

External 32.768 kHz Sleep Clock Specifications

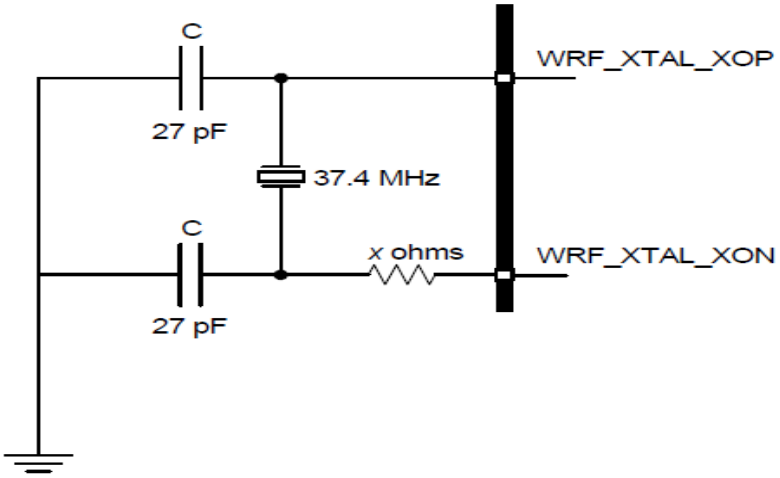
Parameter	*LPO Clock*	*Units*
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[a]	>100k <5	Ω pF
Clock jitter (during initial start-up)	<10,000	ppm

a. When power is applied or switched off.

Crystal Interface and Clock Generation

The AW-CM256SM can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in below. Consult the reference schematics for the latest configuration.

Recommended Oscillator Configuration



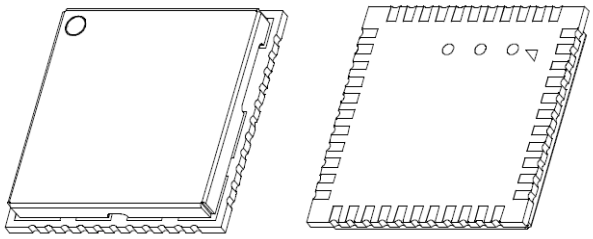
A fractional-N synthesizer in the AW-CM256SM generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references. The recommended default frequency reference is a **37.4 MHz crystal**. The signal characteristics for the crystal interface are listed in below

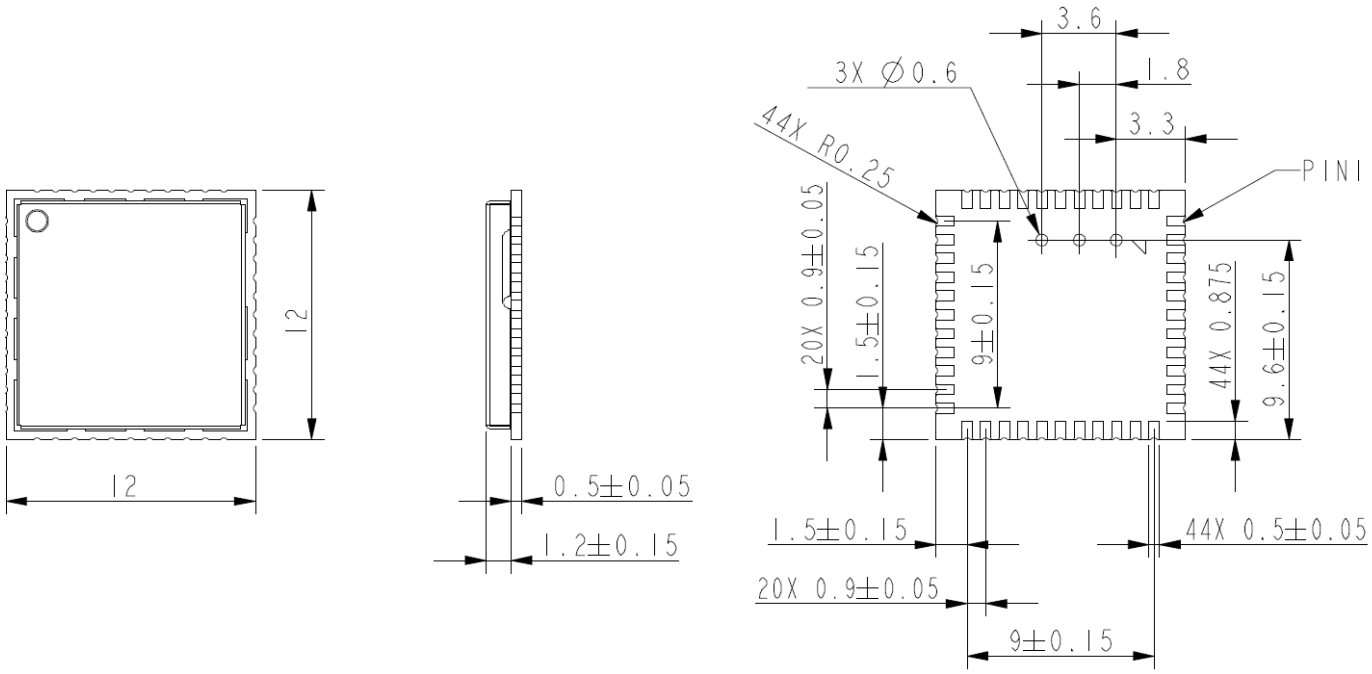
Crystal Oscillator and External Clock—Requirements and Performance (Cont.)

		Crystal[a]			External Frequency Reference[b c]			
Parameter	**Conditions/Notes**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
WRF_XTAL_XOP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_XOP input voltage (see Figure 6 on page 30)	IEEE 802.11a/b/g operation only	–	–	–	400	–	1200	mV_{p-p}
WRF_XTAL_XOP input voltage (see Figure 6 on page 30)	IEEE 802.11n/ac AC-coupled analog input	–	–	–	1	–	–	V_{p-p}
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[g] (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase Noise[g] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–144	dBc/Hz
Phase Noise[g] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase Noise[g] (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–149	dBc/Hz
Phase Noise[g] (IEEE 802.11ac, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–148	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–155	dBc/Hz

4. Mechanical Information

4.1 Mechanical Drawing





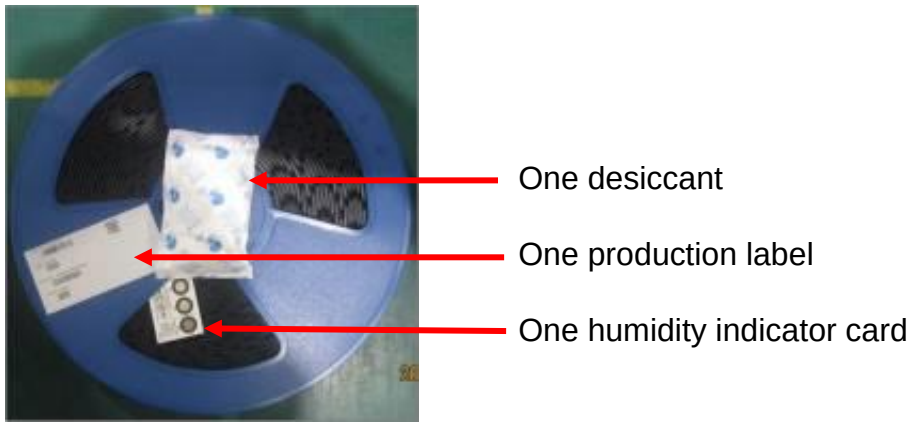
5. Packaging Information

1. One reel can pack 1,500pcs 12x12 stamp LGA modules

   (整軸產品數量為 1500pcs)

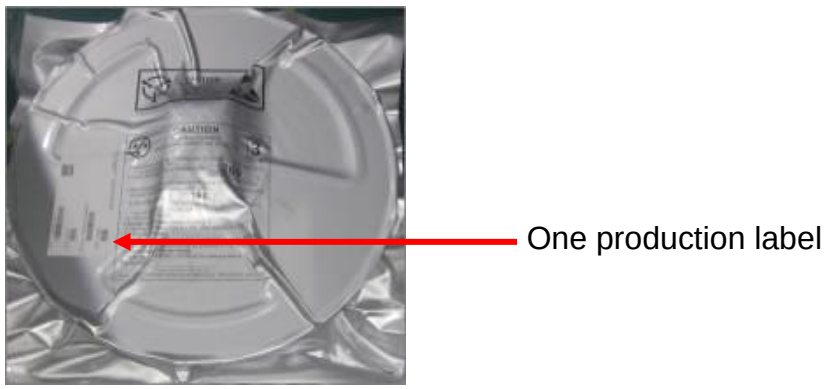
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel

   (卷軸貼上一張生產標籤，並放上一包防潮包及濕度指示卡)

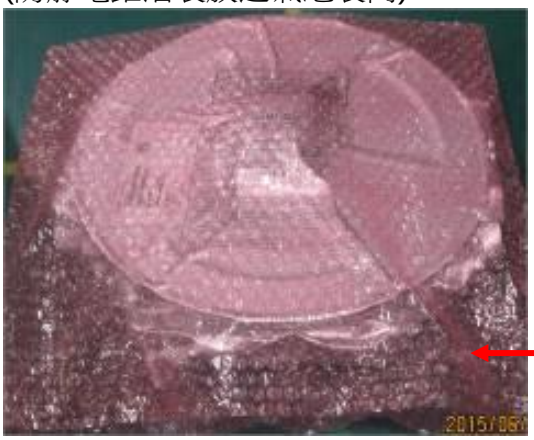


3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag

   (卷軸放進防靜電鋁箔袋，再貼上一張生產標籤)



4. A bag is put into the anti-static pink bubble wrap
   (防靜電鋁箔袋放進氣泡袋內)



One anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box
   (氣泡袋放進內箱中，再貼上一張生產標籤)

One production label

6. **5 inner boxes** could be put into one carton
   (五個內箱可以放進一個外箱)

7. Sealing the carton by AzureWave tape

   (使用海華 Logo 膠帶將外箱進行工字型封箱)

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton

   (外箱上貼附出貨標籤和箱號標籤；如不滿箱，需貼附尾數標籤)

Example of carton label (出貨標籤的範例)	AzureWave P/N: 2-2161H-B2 Customer: 由業務提供 Customer P/N: 由業務提供 Customer PO: 由業務提供 Description: AW-CB161H QTY: 1200 pcs C/N: N.W.: G.W. RoHS COMPLIANT
Example of box label (箱號標籤)	
Example of production label (生產標籤)	P/N: D/C: 1309 PCK NO.: PCKNO0069097 QTY: 294 BAG SEAL DATE: _____
Example of balance label (尾數標籤)