

AW-CU427

IEEE 802.11 b/g/n MAC/baseband/radio and Bluetooth 4.2 IoT Module

Datasheet

Version 02

Revision History

<i>Revision</i>	<i>Date</i>	<i>Description</i>	<i>Initials</i>	<i>Approved</i>
Version 0.1	2019/03/25	Initial Version	Steven Jian	Chihhao Liao
Version 0.2	2019/04/25	Update Dimension	Steven Jian	Chihhao Liao

Table of Contents

Revision History	2
1. Introduction.....	4
1.1 Product Overview	4
1.2 Features.....	5
1.2.1 WLAN.....	5
1.2.2 Bluetooth	5
1.2.3 MCU	5
1.3 Block Diagram.....	7
1.4 Specifications Table	8
1.4.1 General	8
1.4.2 WLAN.....	8
1.4.3 Bluetooth	10
1.4.4 Operating Conditions.....	10
2. Pin Definition	11
2.1 Pin Map.....	11
2.2 Pin Table.....	12
3. Electrical Characteristics	17
3.1 Absolute Maximum Ratings.....	17
3.2 Recommended Operating Conditions.....	17
3.3 GPIO DC Characteristics*	17
3.4 Bluetooth PCM Interface Timing.....	18
3.5 Power Consumption*	20
3.5.1 WLAN.....	20
3.5.2 Bluetooth	21
4. Mechanical Information	21
4.1 Mechanical Drawing.....	21
5. Packaging Information	24

1. Introduction

1.1 Product Overview

PRODUCT OVERVIEW AND FUNCTIONAL DESCRIPTION

AzureWave presents AW-CU427 Wi-Fi & Bluetooth with Microcontroller solution which provides a highly cost-effective, flexible and easy to-use hardware/software platform to build a new generation of connected, smart devices. These smart-connected devices enable device to deliver a broad-range of services to consumers including energy-management, demand-response, home automation and remote access. This allows a user to manage comfort and convenience, also run diagnostics and receive alerts and notifications, in addition to managing and controlling the device. Developers can leverage the rich connectivity features of these new smart devices to create a new generation of innovative new applications and services

The AW-CU427 offers the lowest RBOM. In addition, it integrates a power amplifier (PA) that meets the output power requirements of most handheld systems, a low-noise amplifier (LNA) for best-in-class receiver sensitivity, and an internal transmit/receive (iTR) RF switch, further reducing the overall solution cost and printed circuit board area. The AW-CU427 implements the world's most advanced Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative WLAN and Bluetooth coexistence.

1.2 Features

- Integrates Cypress solutions of CYW43438 & PSoC 62 (CY8C6247BZI-D54)
- Lead-free + Halogen Free Design
- 36.0mm(L) x 18mm(W) x 2.45 mm(H)
- On board PCB antenna (can opt for external antenna with ipex MHF connector)

1.2.1 WLAN

- Support single band 802.11 b/g/n
- SDIO v2.0, including DS and HS modes
- Security: WEP, WPA/WPA2 (personal), AES (HW), TKIP (HW), CKIP (SW), WMM/WMM-PS/WMM-SA

1.2.2 Bluetooth

- Bluetooth SmartAudio® technology improves voice and music quality to headsets
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Maximum UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.2 packet types
- Fully supports Bluetooth Core Specification version 4.2 + (Enhanced Data Rate) EDR features:
 - Adaptive Frequency Hopping (AFH)
 - Quality of Service (QoS)
 - Extended Synchronous Connections (eSCO) — Voice Connections
 - Fast Connect (interlaced page and inquiry scans)
 - Secure Simple Pairing (SSP)
 - Sniff Subrating (SSR)
 - Encryption Pause Resume (EPR)
 - Extended Inquiry Response (EIR)
 - Link Supervision Timeout (LST)

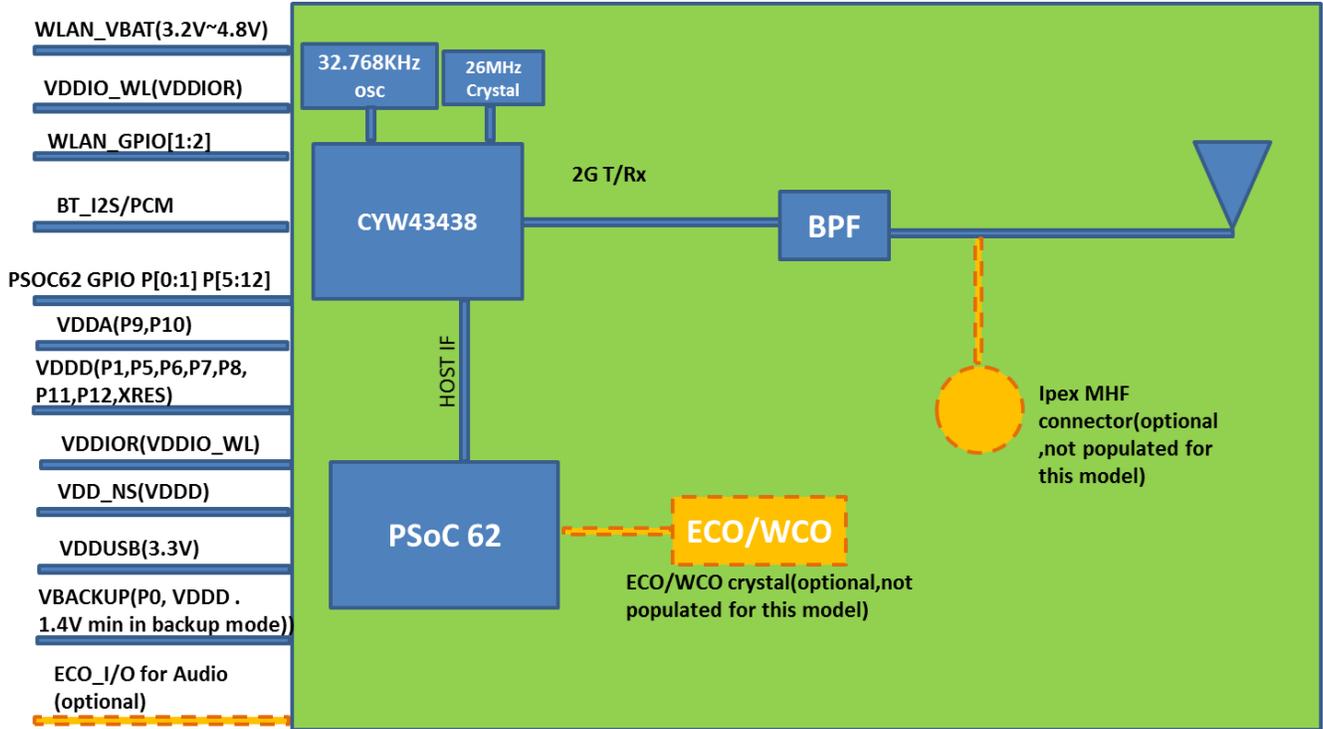
1.2.3 MCU

- 150-MHz Arm Cortex-M4F CPU with single-cycle multiply (Floating Point and Memory Protection Unit)
- 100-MHz Cortex M0+ CPU

- **1 MB Application Flash with 32-KB EEPROM area and 32-KB Supervisory Flash**
- **288 KB integrated SRAM**
- **OTP E-Fuse memory for validation and security**
- **Backup domain with 64 bytes of memory and Real-time Clock(RTC)**
- **8 MHz Internal Main Oscillator (IMO) with 2% accuracy**
- **USB Full-Speed Dual-role Host and Device interface**
- **I2S Interface; up to 192 ksps Word Clock**
- **Two PDM channels for stereo digital microphones**
- **Execute-In-Place (XIP) from external Quad SPI Flash**
- **Supports 1, 2, 4, and Dual-Quad interfaces**
- **12-bit 1 Msps SAR ADC with differential and single-ended modes**
- **Cypress CapSense Sigma Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing**
- **Mutual Capacitance sensing (Cypress CSX) with dynamic usage of both Self and Mutual sensing**
- **Automatic hardware tuning (SmartSense™)**
- **Hardware acceleration for Symmetric and Asymmetric cryptographic methods (AES, 3DES, RSA, and ECC) and Hash functions (SHA-512, SHA-256)**

1.3 Block Diagram

A simplified block diagram of the AW-CU427 module is depicted in the figure below.



**Support different HW configurations. Please contact Azurewave for the details.*

1.4 Specifications Table

1.4.1 General

Features	Description
Product Description	IEEE 802.11 b/g/n Wireless LAN and Bluetooth IoT Module
Major Chipset	Cypress CYW43438, PSoC 62 (CY8C6247BZI-D54)
Host Interface	SPI/UART/SDIO/USB/I2C/I2S
Dimension	36.0mm(L) x 18mm(W) x 2.8mm(H)
Package	LGA Module
Antenna	Internal PCB antenna
Weight	TBD

1.4.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
WLAN VID/PID	n/a
WLAN SVID/SPID	n/a
Frequency Range	WLAN: 2.4 GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps), QPSK(18/12Mbps), DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps), 16-QAM(36/24Mbps), 64-QAM (72.2/54/48Mbps)
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 Japan – 1 ~ 13 802.11g: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13 802.11n: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13

	2.4G				
Output Power (Board Level Limit)*		Min	Typ	Max	Unit
	11b (11Mbps) @EVM<35%	16	18	20	dBm
	11g (54Mbps) @EVM ≤ -25 dB	13	15	17	dBm
	11n (HT20 MCS7) @EVM ≤ -27 dB	12	14	16	dBm
	2.4G				
Receiver Sensitivity		Min	Typ	Max	Unit
	11b (1Mbps)		-97	-93	dBm
	11g (6Mbps)		-91	-87	dBm
	11b (11Mbps)		-88	-84	dBm
	11g (54Mbps)		-75	-70	dBm
	11n (HT20 MCS0)		-90	-86	dBm
	11n (HT20 MCS7)		-71	-67	dBm
Data Rate	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: MCS0~7 HT20				
Security	<ul style="list-style-type: none"> ◆ WPA™- and WPA2™- (Personal) support for powerful encryption and authentication ◆ AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility ◆ Cisco® Compatible Extension- (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX5.0) certified ◆ Wi-Fi Protected Setup (WPS) ◆ WEP ◆ WMM / WMM-SA ◆ CKIP(Software) 				

* If you have any certification questions about output power please contact FAE directly.

1.4.3 Bluetooth

Features	Description																				
Bluetooth Standard	Bluetooth 2.1+Enhanced Data Rate (EDR) / BT4.2																				
Bluetooth VID/PID	n/a																				
Frequency Range	2400~2483.5MHz																				
Modulation	GFSK (1Mbps), $\pi/4$ DQPSK (2Mbps) and 8DPSK (3Mbps)																				
Output Power	Basic Rate : 10dBm +/- 3dBm (Max Settings) BLE:8.5dBm+/-3dBm																				
Receiver Sensitivity	<table border="1"> <thead> <tr> <th></th> <th>Min</th> <th>Typ</th> <th>Max</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td>DH5</td> <td></td> <td>-92</td> <td>-82</td> <td>dBm</td> </tr> <tr> <td>2DH5</td> <td></td> <td>-94</td> <td>-84</td> <td>dBm</td> </tr> <tr> <td>3DH5</td> <td></td> <td>-88</td> <td>-78</td> <td>dBm</td> </tr> </tbody> </table>		Min	Typ	Max	Unit	DH5		-92	-82	dBm	2DH5		-94	-84	dBm	3DH5		-88	-78	dBm
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3DH5		-88	-78	dBm																	

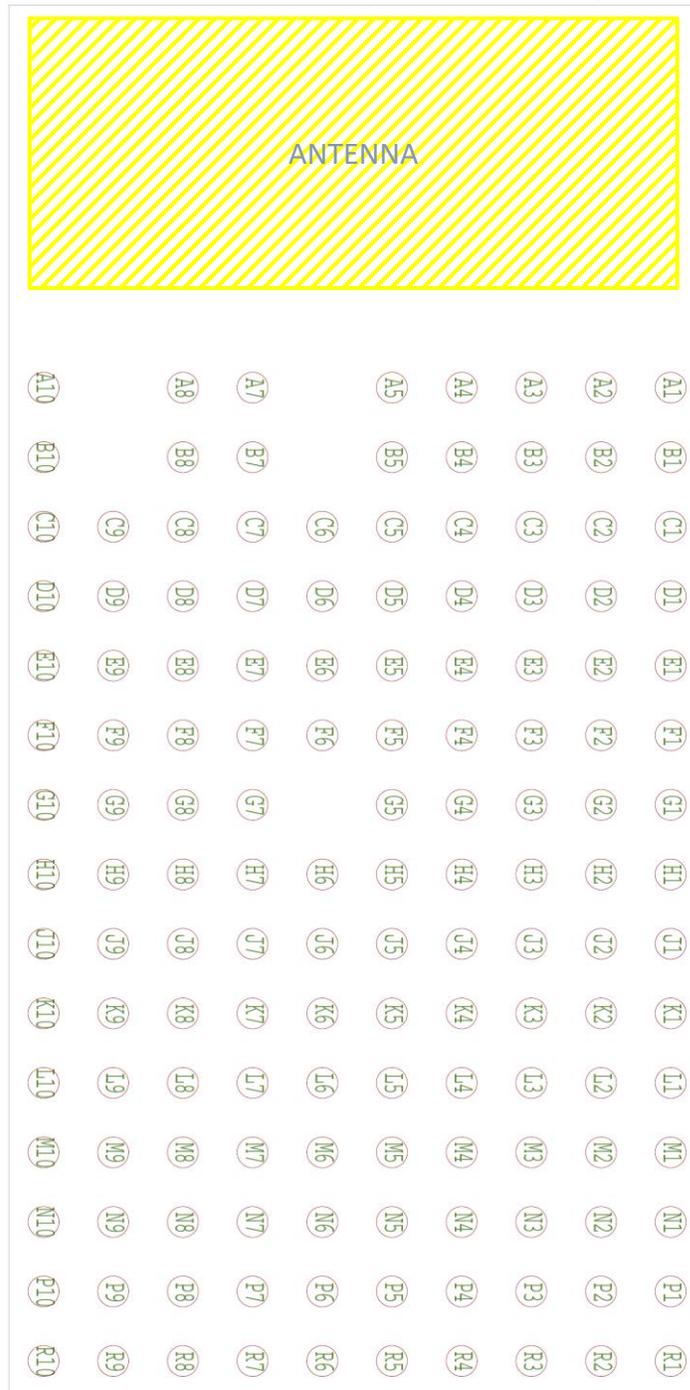
1.4.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	power supply WIFI/BT VBAT:3.2V~4.8V (3.6V Typical) VDD for MCU(except for USB):1.7V~3.6V
Operating Temperature	-30~70°C (Functionality is guaranteed.)
Operating Humidity	<85%
Storage Temperature	-40~85°C
Storage Humidity	<60 %
ESD Protection	
Human Body Model	>1kV
Charged Device Model	>300V

2. Pin Definition

2.1 Pin Map

AW-CU427 Top View Pin Map



2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
G3	BT_PCM_CLK/I2S_CLK	PCM or I2S clock; can be master (output) or slave (input)	VDDIO_WL	I/O
D3	BT_PCM_IN/I2S_DI	PCM or I2S data input sensing	VDDIO_WL	I
E3	BT_PCM_OUT/I2S_DO	PCM or I2S data output	VDDIO_WL	O
F3	BT_PCM_SYNC/I2S_WS	PCM SYNC or I2S_WS; can be master (output) or slave (input)	VDDIO_WL	I/O
D5	BT_REG_ON	Reserved for debug use only	VDDIO_WL	I
B1	BT_UART_CTS	Reserved for debug use only	VDDIO_WL	I
D2	BT_UART_RTS	Reserved for debug use only	VDDIO_WL	O
C2	BT_UART_RXD	Reserved for debug use only	VDDIO_WL	I
B2	BT_UART_TXD	Reserved for debug use only	VDDIO_WL	O
N5	ECO_IN_MODULE	Reserved.		Floating
N4	ECO_OUT_MODULE	Reserved.		Floating
A1	GND_A1	Ground.		GND
A10	GND_A10	Ground.		GND
A2	GND_A2	Ground.		GND
A3	GND_A3	Ground.		GND
A4	GND_A4	Ground.		GND
A5	GND_A5	Ground.		GND
A7	GND_A7	Ground.		GND
A8	GND_A8	Ground.		GND
B10	GND_B10	Ground.		GND
B3	GND_B3	Ground.		GND
B7	GND_B7	Ground.		GND
B8	GND_B8	Ground.		GND
C10	GND_C10	Ground.		GND
C3	GND_C3	Ground.		GND
C6	GND_C6	Ground.		GND
C7	GND_C7	Ground.		GND
C8	GND_C8	Ground.		GND
C9	GND_C9	Ground.		GND
D1	GND_D1	Ground.		GND
D7	GND_D7	Ground.		GND
D8	GND_D8	Ground.		GND

D9	GND_D9	Ground.		GND
E2	GND_E2	Ground.		GND
E5	GND_E5	Ground.		GND
F2	GND_F2	Ground.		GND
F6	GND_F6	Ground.		GND
F9	GND_F9	Ground.		GND
G1	GND_G1	Ground.		GND
G2	GND_G2	Ground.		GND
G7	GND_G7	Ground.		GND
H10	GND_H10	Ground.		GND
H3	GND_H3	Ground.		GND
H8	GND_H8	Ground.		GND
J8	GND_J8	Ground.		GND
J9	GND_J9	Ground.		GND
K2	GND_K2	Ground.		GND
K4	GND_K4	Ground.		GND
K5	GND_K5	Ground.		GND
K8	GND_K8	Ground.		GND
L1	GND_L1	Ground.		GND
L5	GND_L5	Ground.		GND
L7	GND_L7	Ground.		GND
N3	GND_N3	Ground.		GND
P3	GND_P3	Ground.		GND
P6	GND_P6	Ground.		GND
P8	GND_P8	Ground.		GND
R9	GND_R9	Ground.		GND
K6	P0_2	PSoC 62 P0.2	VBACKUP	I/O
J7	P0_3	PSoC 62 P0.3	VBACKUP	I/O
K7	P0_4	PSoC 62 P0.4	VBACKUP	I/O
J6	P0_5	PSoC 62 P0.5	VBACKUP	I/O
M2	P1_0	PSoC 62 P1.0	VDDD	I/O
M3	P1_1	PSoC 62 P1.1	VDDD	I/O
K3	P1_2	PSoC 62 P1.2	VDDD	I/O
L3	P1_3	PSoC 62 P1.3	VDDD	I/O
L2	P1_4	PSoC 62 P1.4	VDDD	I/O
J3	P1_5	PSoC 62 P1.5	VDDD	I/O

R7	P10_0	PSoC 62 P10.0	VDDA	I/O
R6	P10_1	PSoC 62 P10.1	VDDA	I/O
P7	P10_2	PSoC 62 P10.2	VDDA	I/O
L6	P10_3	PSoC 62 P10.3	VDDA	I/O
N7	P10_4	PSoC 62 P10.4	VDDA	I/O
M7	P10_5	PSoC 62 P10.5	VDDA	I/O
M6	P10_6	PSoC 62 P10.6	VDDA	I/O
R4	P11_0	PSoC 62 P11.0	VDDD	I/O
L4	P11_1	PSoC 62 P11.1	VDDD	I/O
R5	P11_2	PSoC 62 P11.2	VDDD	I/O
N6	P11_3	PSoC 62 P11.3	VDDD	I/O
M4	P11_4	PSoC 62 P11.4	VDDD	I/O
P4	P11_5	PSoC 62 P11.5	VDDD	I/O
P5	P11_6	PSoC 62 P11.6	VDDD	I/O
M5	P11_7	PSoC 62 P11.7	VDDD	I/O
R2	P12_0	PSoC 62 P12.0	VDDD	I/O
R1	P12_1	PSoC 62 P12.1	VDDD	I/O
N1	P12_2	PSoC 62 P12.2	VDDD	I/O
P1	P12_3	PSoC 62 P12.3	VDDD	I/O
P2	P12_4	PSoC 62 P12.4	VDDD	I/O
N2	P12_5	PSoC 62 P12.5	VDDD	I/O
C4	P5_0	PSoC 62 P5.0	VDDD	I/O
F4	P5_1	PSoC 62 P5.1	VDDD	I/O
E4	P5_2	PSoC 62 P5.2	VDDD	I/O
F5	P5_3	PSoC 62 P5.3	VDDD	I/O
D4	P5_4	PSoC 62 P5.4	VDDD	I/O
B5	P5_5	PSoC 62 P5.5	VDDD	I/O
B4	P5_6	PSoC 62 P5.6	VDDD	I/O
C5	P5_7	PSoC 62 P5.7	VDDD	I/O
F7	P6_0	PSoC 62 P6.0	VDDD	I/O
E7	P6_1	PSoC 62 P6.1	VDDD	I/O
E8	P6_2	PSoC 62 P6.2	VDDD	I/O
G8	P6_3	PSoC 62 P6.3	VDDD	I/O
F8	P6_4	PSoC 62 P6.4	VDDD	I/O
E9	P6_5	PSoC 62 P6.5	VDDD	I/O
E10	P6_6	PSoC 62 P6.6	VDDD	I/O

D10	P6_7	PSoC 62 P6.7	VDDD	I/O
F10	P7_0	PSoC 62 P7.0	VDDD	I/O
H9	P7_3	PSoC 62 P7.3	VDDD	I/O
G9	P7_4	PSoC 62 P7.4	VDDD	I/O
G10	P7_5	PSoC 62 P7.5	VDDD	I/O
J10	P8_0	PSoC 62 P8.0	VDDD	I/O
K9	P8_1	PSoC 62 P8.1	VDDD	I/O
L8	P8_2	PSoC 62 P8.2	VDDD	I/O
K10	P8_3	PSoC 62 P8.3	VDDD	I/O
L9	P8_4	PSoC 62 P8.4	VDDD	I/O
M8	P8_5	PSoC 62 P8.5	VDDD	I/O
L10	P8_6	PSoC 62 P8.6	VDDD	I/O
M9	P8_7	PSoC 62 P8.7	VDDD	I/O
P9	P9_0	PSoC 62 P9.0	VDDA	I/O
N9	P9_1	PSoC 62 P9.1	VDDA	I/O
M10	P9_2	PSoC 62 P9.2	VDDA	I/O
N8	P9_3	PSoC 62 P9.3	VDDA	I/O
P10	P9_4	PSoC 62 P9.4	VDDA	I/O
N10	P9_5	PSoC 62 P9.5	VDDA	I/O
R10	P9_6	PSoC 62 P9.6	VDDA	I/O
H4	SDIO_CLK_TP	Floating Pin, No connect to anything.		Floating
G5	SDIO_CMD_TP	Floating Pin, No connect to anything.		Floating
H5	SDIO_DATA0_TP	Floating Pin, No connect to anything.		Floating
G4	SDIO_DATA1_TP	Floating Pin, No connect to anything.		Floating
H7	SDIO_DATA2_TP	Floating Pin, No connect to anything.		Floating
H6	SDIO_DATA3_TP	Floating Pin, No connect to anything.		Floating
J4	USBDM	PSoC 62 USB D-	3.3V	I/O
J5	USBDP	PSoC 62 USB D+	3.3V	I/O
M1	VBACKUP	VBACKUP is the supply to the backup domain. The backup domain includes the 32-kHz WCO, RTC, and backup registers. It can generate a wake-up interrupt to the chip via the RTC timers or an external input. It can also generate an output to wakeup external circuitry. It is connected to VDDD when not used as a separate battery backup domain. VBACKUP provides the supply for Port 0. Min. is 1.4 V in Backup Mode		PWR
K1	VDD_NS	Power Supply for PSoC 62 Buck regulator	VDDD	PWR

H2	VDD_USB	Power Supply for PSoC 62 USB	3.3V	PWR
R8	VDDA	Power Supply for PSoC 62 P9,P10 (analog peripherals)	1.7~3.6V	PWR
R3	VDDD	Power Supply for PSoC 62 P1,P5,P6,P7,P8,P11,P12,XRES	1.7~3.6V	PWR
H1	VDDIO_WL	Power Supply for CYW43438 Digital I/O. Connect it to VDDIOR.	VDDIOR	PWR
J1	VDDIOR	Power Supply for PSoC 62 P2,P3,P4. Connect it to VDDIO_WL	1.7~3.6V	PWR
D6	WL_GPIO1	Reserved for debug use only	VDDIO_WL	I/O
E6	WL_GPIO2	Reserved for debug use only	VDDIO_WL	I/O
C1	WL_REG_ON	Reserved for debug use only	VDDIO_WL	I
F1	WLAN_VBAT	Main Power Supply for CYW43438	3.2~4.8V	PWR
E1	WLAN_VBAT	Main Power Supply for CYW43438	3.2~4.8V	PWR
J2	XRES_L	External reset I/O pin	VDDD	I

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
WLAN_VBAT	Power supply for CYW43438 PMU	-0.5	6	V
VDDD,VDDIOR,VDD_NS,VDDA,VDD_USB,VBACKUP	Power Supply for PSoC 62	-0.5	4	V
VDDIO_WL	Power supply for CYW43438 digital I/O	-0.5	3.9	V
USB_VDD_3V3	CYW4907 USB Power Supply	-0.5	3.9	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
WLAN_VBAT	Power supply for CYW43438 PMU	3.2	3.6	4.8	V
VDDD,VDDIOR,VDD_NS,VDDA	Power Supply for PSoC 62	1.7		3.6	V
VDDIO_WL	IO Voltage for WLAN(Does not support 1.8V unless BT is disabled)	1.7		3.6	V
VDD_USB	Power Supply for PSoC 62 USB	3.15	3.3	3.6	V
VBACKUP	Power supply to the PSoC 62 backup domain	1.4		3.6	V

3.3 GPIO DC Characteristics*

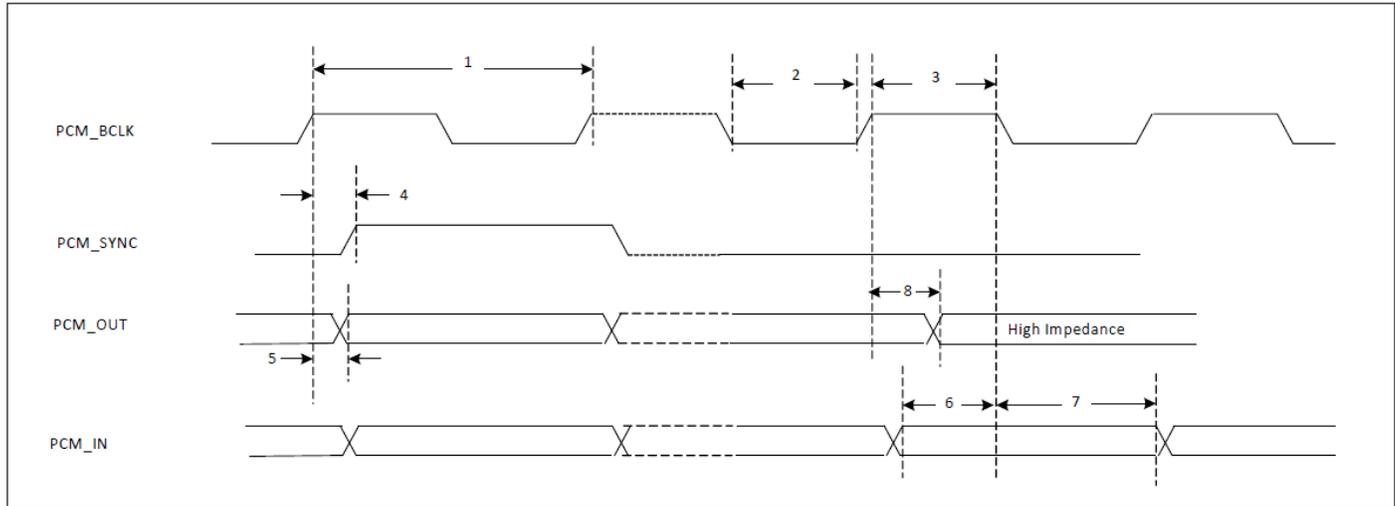
Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{IH}	Input high voltage	CMOS Input	0.7*VDD			V
V _{IL}	Input low voltage	CMOS Input			0.3*VDD	V
V _{IH}	Input high voltage	LVTTL input, VDD < 2.7 V	0.7*VDD			V
V _{IL}	Input low voltage	LVTTL input, VDD < 2.7 V			0.3*VDD	V

V _{IH}	Input high voltage	LVTTL input, VDD >= 2.7 V	2			V
V _{IL}	Input low voltage	LVTTL input, VDD >= 2.7 V			0.8	V
V _{OH}	Output High Voltage	IOH = 8 mA	VDD-0.5			V
V _{OL}	Output Low Voltage	IOL = 8 mA			0.4	V

*please find the details @ <https://www.cypress.com/documentation/datasheets/psoc-6-mcu-psoc-62-datasheet-programmable-system-chip-psoc>

3.4 Bluetooth PCM Interface Timing

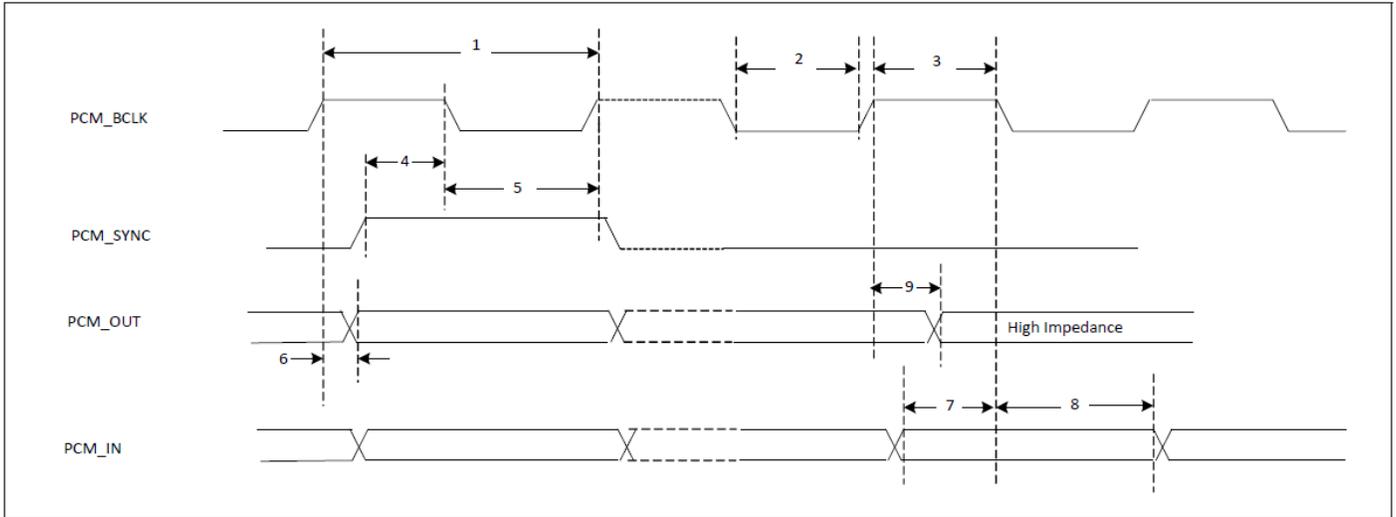
PCM Timing Diagram (Short Frame Sync, Master Mode)



PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

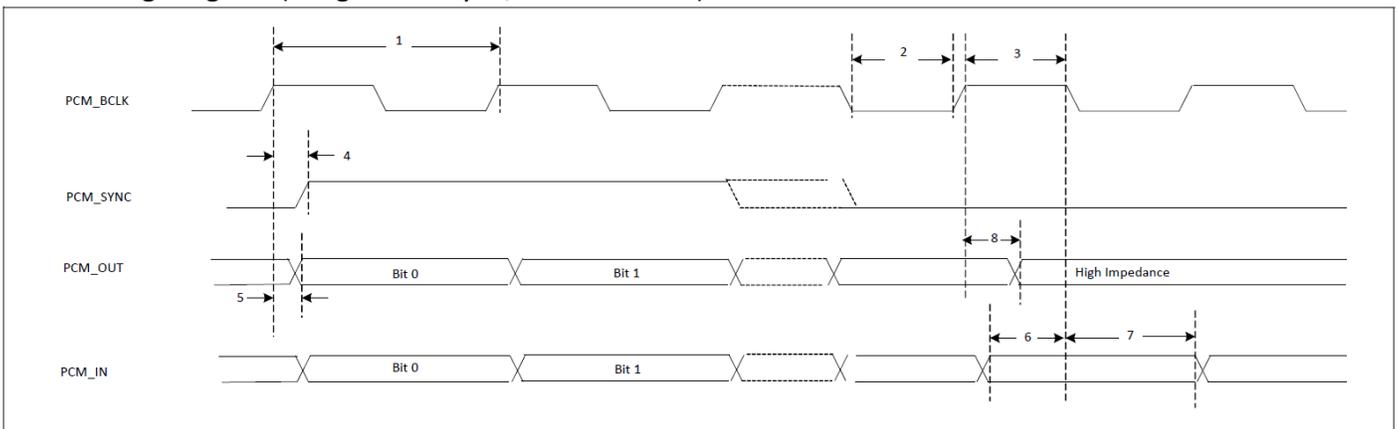
PCM Timing Diagram (Short Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

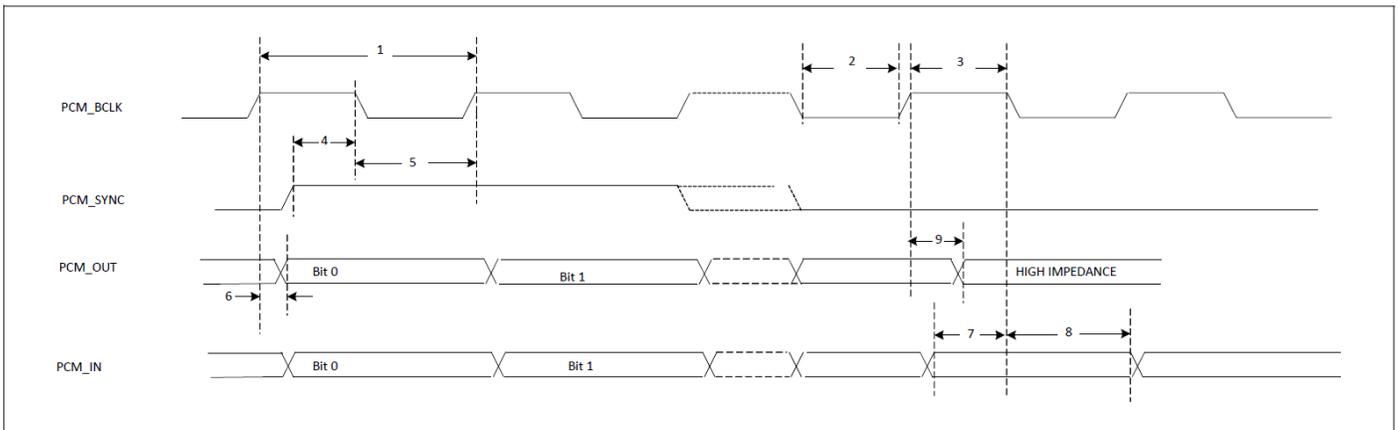
PCM Timing Diagram (Long Frame Sync, Master Mode)



PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

PCM Timing Diagram (Long Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

3.5 Power Consumption*

3.5.1 WLAN

TBD

3.5.2 Bluetooth

TBD

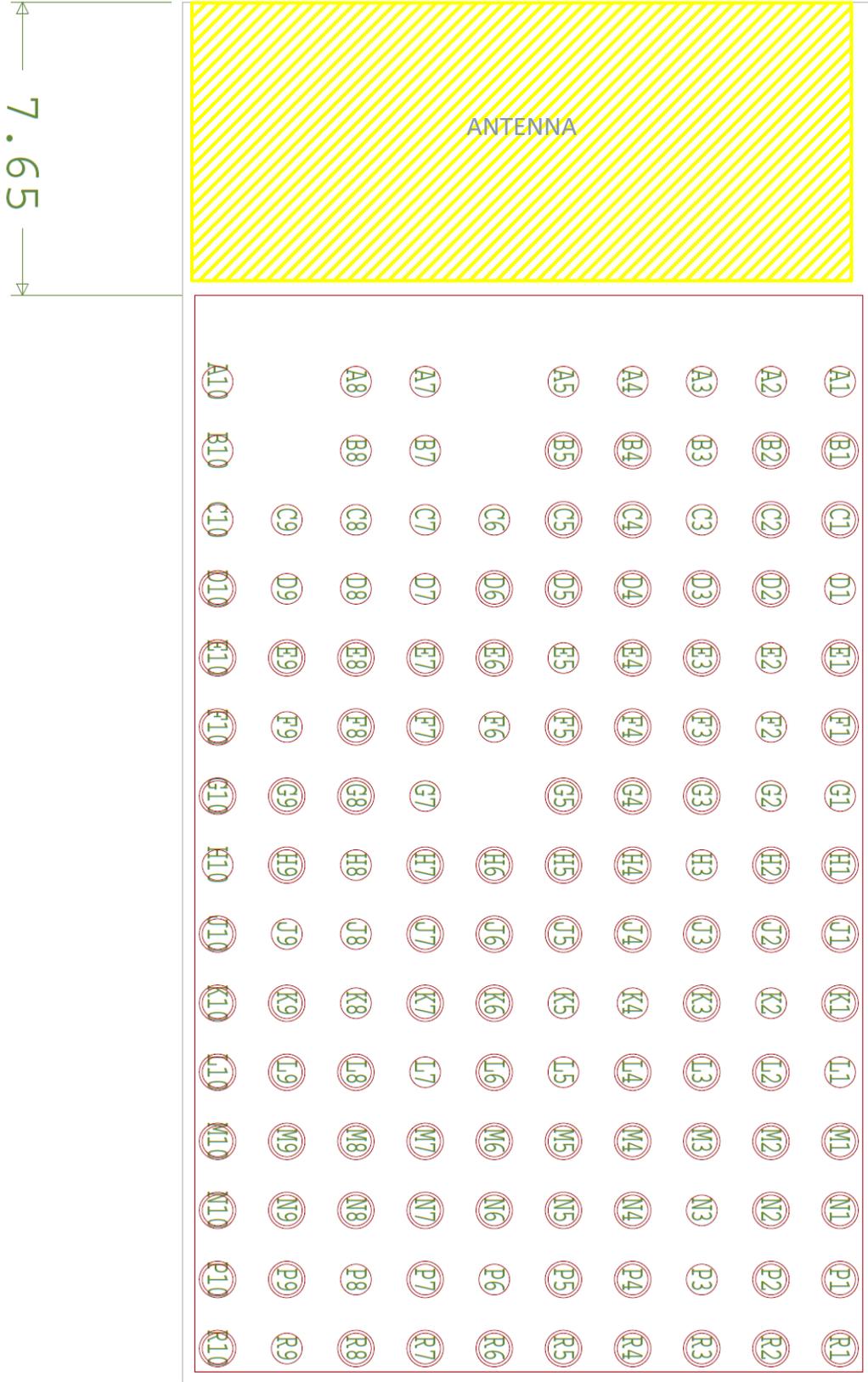
* The power consumption is based on Azurewave test environment, these data for reference only.

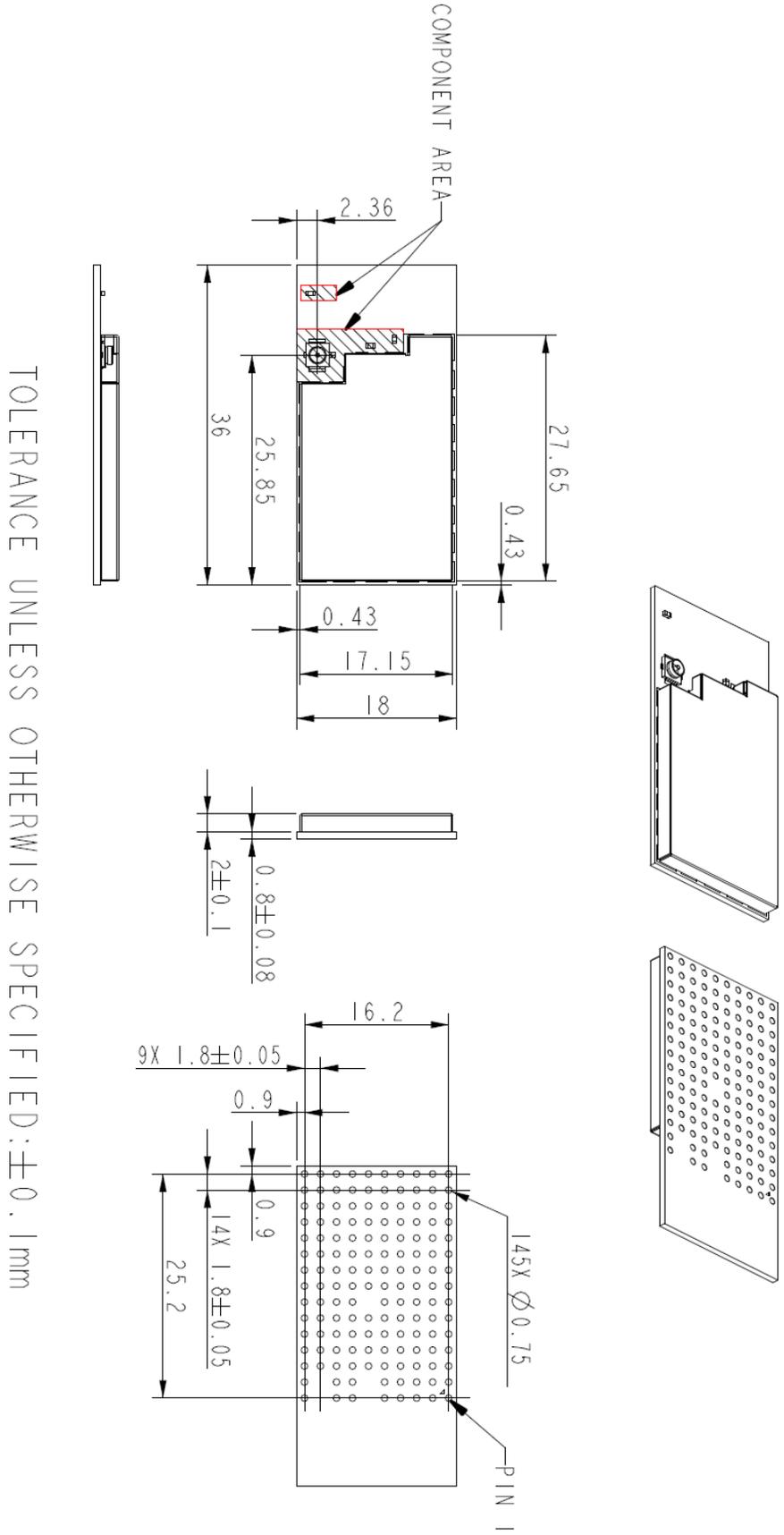
4. Mechanical Information

4.1 Mechanical Drawing

AW-CU427 TOP View PCB Layout Footprint (Unit in mm Dia=0.75mm Solder Mask Defined)

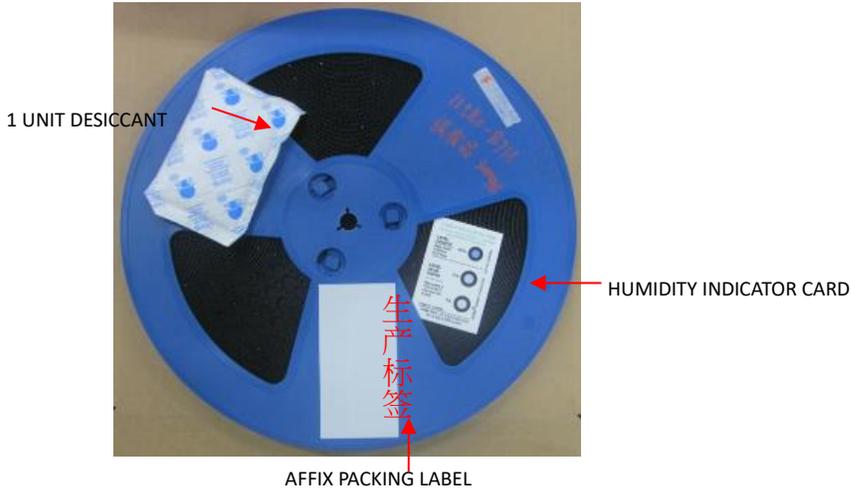
**Keep out distance of the print antenna is > 20mm for internal antenna option*



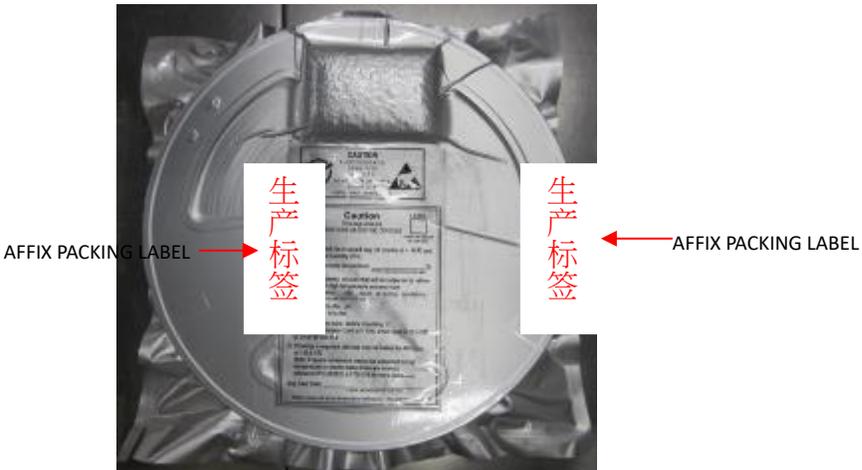


5. Packaging Information

5.1



5.2



5.3



5.4



5.5

1 Carton= 5 Boxes



5.6

