AW-CM389NF

IEEE 802.11 2X2 MIMO ac/a/b/g/n Wireless LAN + Bluetooth NGFF Module

Datasheet

Version 1.3

Document release	Date	Modification	Initials	Approved
Version0.1	2013/08/13	Initial version	Kai Wu	Chihhao Liao
Version0.2	2013/10/08	1. Update Pin Map 2. Update Interface Configuration straps	Alex Yu	Chihhao Liao
Version0.3	2013/11/07	1. Update Pin Map 2. Update Pin Definition 3. Update Dimension	Alex Yu	Chihhao Liao
Version0.4	2013/11/19	1. Update “2 Electrical Characteristic” 2. Update “3-1 SDIO Interface” 3. Update “4 Pin Definition” 4. Update “5 Mechanical Information” 5. Add “2-2.1 The interface pins power supply”	Alex Yu	Chihhao Liao
Version0.5	2013/12/03	Add “4 Pin Definition’s Notes”	Alex Yu	Chihhao Liao
Version0.6	2013/12/05	Update “4 Pin Definition’s Notes”	Alex Yu	Chihhao Liao
Version0.7	2013/12/11	1. Update “1-2 Block Diagram” 2. Update “5-2 Module Footprint”	Alex Yu	Chihhao Liao
Version0.8	2014/03/20	1. Update “1-4 Bluetooth Standard” 2. Update “5-1 Mechanical Information” 3. Update “2-3 Clock Specification” 4. Update “5-2 Module Footprint” 5. Add “7. Shipping Information”	Alex Yu	Chihhao Liao
Version0.9	2014/04/14	1. Update “1-4 Specifications Table” 2. Update “5-1 Mechanical Information”	Alex Yu	Chihhao Liao
Version 1.0	2015/01/24	1. Update“ Interface supports and combinations” 2. Update “1-4 Specifications Table” 3. Update “4. Pin Definitions”	Alex Yu	Chihhao Liao
Version 1.1	2015/10/21	1. Update“ Interface supports and combinations 2. Modify operating temperature 3. Support BT4.2	Peter Chen	Chihhao Liao
Version 1.2	2016/11/30	Remove NFC function	Peter Chen	Daniel Lee
Version 1.3	2019/08/06	Correct “5-2 Module Footprint”	Renton Tao	Daniel Lee

1. General Description

1-1. Product Overview and Functional Description

AzureWave Technologies, Inc. introduces the IEEE 802.11ac/a/b/g/n 2X2 MIMO WLAN & Bluetooth NGFF module --- **AW-CM389NF**. The module is targeted to mobile devices including **Notebook, TV, Tablet and Gaming Device** which need small package module, low power consumption, multiple interfaces and OS support. By using AW-CM389NF, the customers can easily enable the Wi-Fi, and BT embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11ac/a/b/g/n standard, the AW-CM389NF uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM389NF. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, the AW-CM389NF also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP)**, Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms.

For the video, voice and multimedia applications the AW-CM389NF support **802.11e Quality of Service** (**QoS).** The device also supports **802.11h Dynamic Frequency Selection (DFS)** for detecting radar pulses when operating in the 5GHz range.

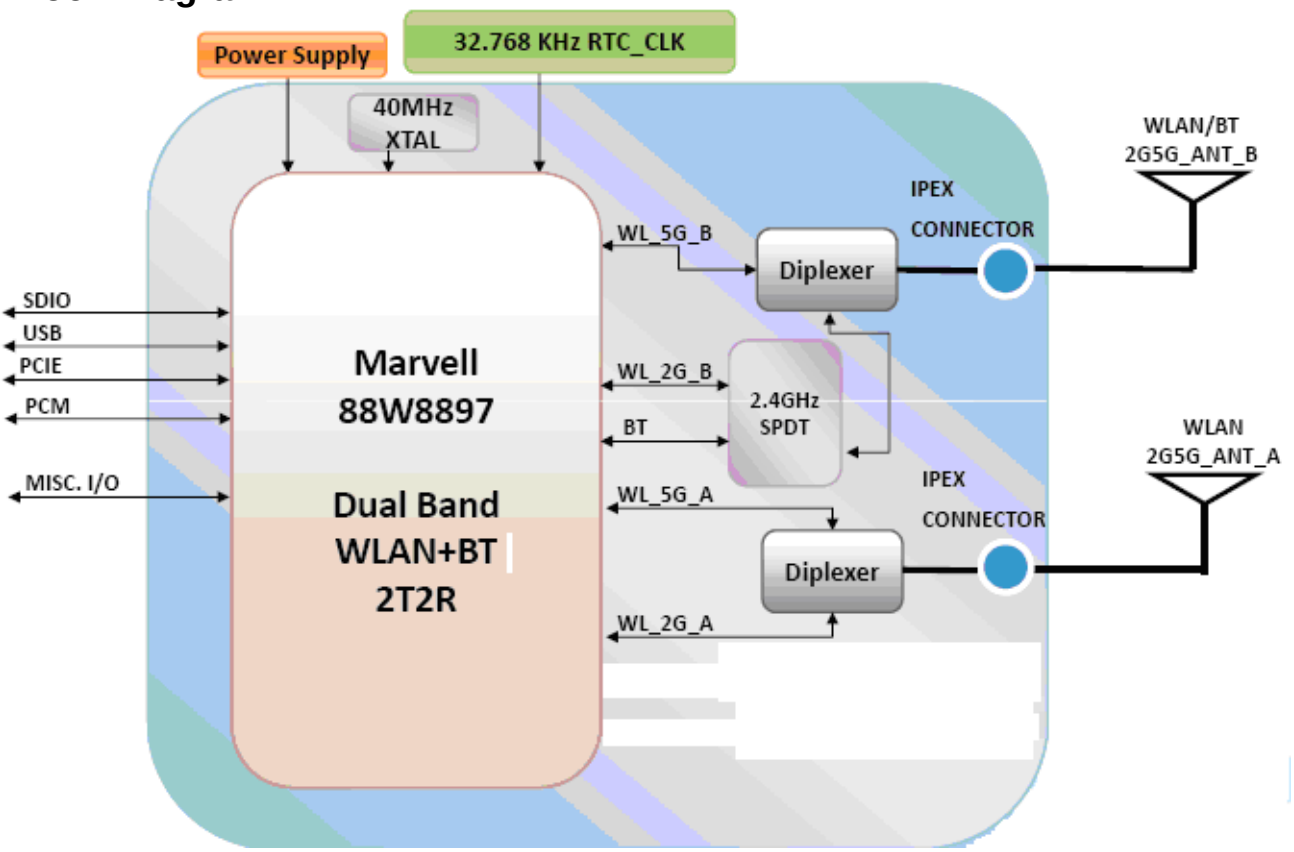
For Bluetooth operation, AW-CM389NF is **Bluetooth 4.2 (supports Low Energy).**

AW-CM389NF supports **SDIO, PCIE, USB,** and high speed **UART interfaces** for WLAN and Bluetooth to the host processor.

AW-CM389NF is suitable for multiple mobile processors for different applications with the support **cellular phone co-existence**.

AW-CM389NF module adopts Marvell's latest highly-integrated dual-band WLAN & Bluetooth SoC--- **88W8897**. All the other components are implemented by all means to reach the mechanical specification required.

1-2. Block Diagram



Note: Interface supports and combinations as shown below:

Scenario	WLAN	BT	BT_AMPS	Firmware Download I/F	Firmware Download Mode	Configuration*
1	SDIO	SDIO	--	SDIO	Serial	CON[3:0]=b'0001
2	SDIO	SDIO	SDIO	SDIO	Serial	CON[3:0]=b'0111
3	PCIe	UART	--	PCIe + UART	Parallel	CON[3:0]=b'1111
4	PCIe	UART	--	PCIe or UART	Serial	CON[3:0]=b'1100
5	PCIe	USB	USB	PCIe	Serial	CON[3:0]=b'1110

*Configuration pins:

Configuration	Pin No	Pin Name
CON[3]	13	CONFIG_HOST[3]
CON[2]	10	CONFIG_HOST[2]
CON[1]	9	CONFIG_HOST[1]
CON[0]	8	CONFIG_HOST[0]

1-3. Key feature:

- **Small footprint: 12mm(L) x 16mm(W) x 1.4 mm(H)**
- **SDIO3.0, G-SPI, USB interfaces support for WLAN**
- **High speed UART,PCM/Inter-IC Sound(I2S) and SDIO3.0, USB for Bluetooth**
- **Bluetooth 4.2 complaint with Bluetooth 2.1 + Enhanced Data Rate (EDR)**
- **Audio Codec interface support**
- **Cellular phone co-existence support**
- **Multiple power saving modes for low power consumption**
- **IEEE 802.11i for advanced security**
- **Quality of Service (QoS) support for multimedia applications**
- **Drip-in WLAN Linux drivers are Android ready and validated on Android based systems.**
- **Support for Linux kernel versions up to 2.6.32.**
- **Support for BlueZ v4.47 Bluetooth profiles stack used in Android Éclair**
- **Simultaneous AP-STA**
- **Support China WAPI**
- **Lead-free design**

1-4. Specifications Table

Model Name	AW-CM389NF
Product Description	**2x2 MIMO Wireless LAN + Bluetooth Combo Module**
WLAN Standard	IEEE 802.11 a/b/g/n/ac, Wi-Fi compliant
Bluetooth Standard	Bluetooth 4.2 complaint with Bluetooth 2.1+Enhanced Data Rate (EDR)
Host Interface	USB 2.0 for WLAN and Bluetooth
Major Chipset	Marvell 88W8897
Dimension	12mm x 16mm x 1.4mm
Weight	TBD
Package	LGA
Operating Conditions	
Voltage	3.3V+- 10%
Temperature	Operating: -30 ~ 85ºC ; Storage: -40 ~ 85ºC
Electrical Specifications	
Frequency Range	2.4 GHz ISM radio band / 5 GHz Unlicensed National Information Infrastructure (U-NII) band
Number of Channels	802.11ac: USA-4 802.11a: USA, Taiwan – 12/4 Most European Countries –19 Japan – 4 802.11b: USA, Canada and Taiwan – 11 Most European Countries – 13 France – 4 802.11g: USA, Canada and Taiwan – 11 Most European Countries – 13 Japan – 13 802.11n(HT20): Channel 1~13(2412~2472) 802.11n(HT40): Channel 1~7(2422~2452)
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM and 256-QAM for WLAN GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps) for Bluetooth
Output Power	WLAN G band: 11b:16dBm +/- 2dBm(11M) 11g:14dBm +/- 2dBm (54M) 11n:HT20 13dBm +/- 2dBm(MCS7) HT40 11dBm +/- 2dBm(MCS7) WLAN A band: 11a: 13dBm +/- 2dBm(54M) 11n:HT20 12dBm +/- 2dBm(MCS7) HT40 10dBm +/- 2dBm(MCS7) 11ac: 8dBm +/- 2dBm(MCS9) Bluetooth: Class 2
Antenna Connector	Main Connector: WLAN Aux Connector: WLAN + BT

Receive Sensitivity	**WLAN G band :** **11b:-83dBm (11M)** **11g:-72dBm (54M)** **11n:HT20 -68dBm (MCS7)** **HT40 -65dBm (MCS7)** **WLAN A band:** **11a: -67dBm (54M)** **11n:HT20 -67dBm (MCS7)** **HT40 -64dBm(MCS7)** **11ac: -54dBm(MCS9)** **Bluetooth:** **DH1:-70dBm** **3DH5:-70dBm**
Medium Access Protocol	**CSMA/CA with ACK**
Data Rates	**WLAN** **802.11b: 1, 2, 5.5, 11Mbps** **802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps** **802.11n: up to 150Mbps-single** **802.11n: up to 300Mbps-2x2 MIMO** **802.11ac:up to 192.6Mbps (20MHz channel)** **802.11ac:up to 400Mbps (40MHz channel)** **802.11ac:up to 866.7Mbps (80MHz channel)** **Bluetooth** **Bluetooth 2.1+EDR data rates of 1,2, and 3Mbps**
Power Consumption	**TBD**
Operating Range	**Open Space: ~300m ; Indoor: ~100m for WLAN** **Minimum 10 m indoor for Bluetooth** **The transmission speed may vary according to the environment)**
Security	◆ **WAPI** ◆ **WEP 64-bit and 128-bit encryption with H/W TKIP processing** ◆ **WPA/WPA2 (Wi-Fi Protected Access)** ◆ **AES-CCMP hardware implementation as part of 802.11i security standard**
Operating System Compatibility	**Linux(Android), Windows, More information please contact Azurewave FAE.**
Co-Existence	**Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence**

2. Electrical Characteristic

2-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Units
Pin73/ VIO	Host I/O power supply	-- -- --	-- -- --	1.8 2.5 3.3	2.2 3.0 4.0	V
Pin44/ VIO_SD	SDIO power supply	-- --	-- --	1.8 3.3	2.2 4.0	V
Pin5/ 3.3V	LDO VBAT input	--	--	3.3	5.0	V
Pin72/ 3V3_USB	LDO USB VBAT input	--	--	3.3	4.0	V
Pin4/ 3.3V	LDO RF VBAT input	--	--	3.3	4.0	V

2-2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Pin73/ VIO	1.8V/2.5V/3.3V digital I/O power supply	-- -- --	1.62 2.25 2.97	1.8 2.5 3.3	1.98 2.75 3.63	V
Pin44/ VIO_SD	1.8V/3.3V digital I/O SDIO power supply	-- --	1.62 2.97	1.8 3.3	1.98 3.63	V
Pin5/ 3.3V	LDO VBAT input	--	2.7	3.3	5.0	V
Pin72/ 3V3_USB	LDO USB VBAT input	--	2.97	3.3	3.63	V
Pin4/ 3.3V	LDO RF VBAT input	--	2.97	3.3	3.63	V

2-2.1 The interface pins power supply

The SDIO host interface pins are powered from the chip VIO_SD (pin 44) 1.8V/3.3V voltage supply.

- SDIO Defauld Speed, High Speed Modes (3.3V)
- SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)
- SDR104 Mode (208MHz) (1.8V)

The PCI Express host interface pins are powered from the module's chip LDO 1.8V voltage supply internal.

The USB2.0 host interface pins are powered from the 3V3_USB (pin 72) 3.3V voltage supply.

The UART Tx and Rx pins are powered from the VIO (pin 73) voltage supply.

The GPIO pins are powered from the VIO (pin 73) voltage supply (GPIO [9:8] from 3.3V voltage internal).

The clocked serial pins are powered from the module's chip LDO 1.8V voltage supply internal.

The audio pins are powered from the chip VIO (pin 73) voltage supply.

2-3. Clock Specifications

2-3.1 External Sleep Clock Timing

External Sleep Clock is necessary for two reasons:

1. Auto frequency Detection.
   This is where the internal logic will bin the Ref clock source to figure out what is the reference clock frequency is. This is done so no strapping is needed for telling 8897 what the ref clock input is.
2. Allow low current modes for BT to enter sleep modes such as sniff modes.
   The AW-CM389NF external sleep clock pin is powered from the 3.3V voltage supply.

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock Frequency Range	32 or 32.768 - 50ppm	32 or 32.768	32 or 32.768 +50ppm	KHz
T_{HIGH}	Clock high time	40	--	--	ns
T_{LOW}	Clock low time	40	--	--	ns
T_{RISE}	Clock rise time	--	--	5	ns
T_{FALL}	Clock fall time	--	--	5	ns

2-4. Reset Configuration

The AW-CM389NF is reset to its default operating state under the following conditions:

- Power-on reset (POR)
- Software/Firmware reset
- External pin reset (RESETn)

2-4-1. Internal Reset

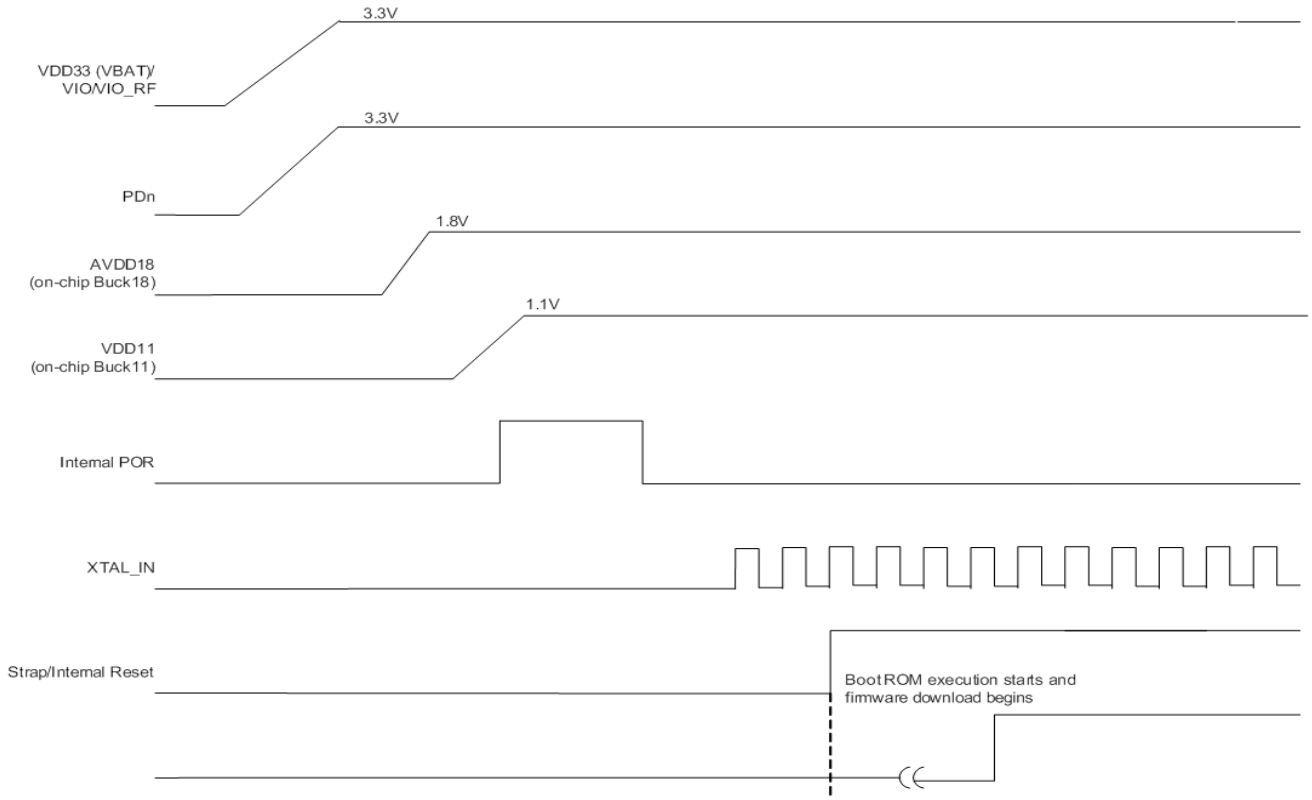
The AW-CM389NF device is reset, and the internal CPU begins the boot sequence when any of the following internal reset events occur:

- Device receives power and VDDL supplies rise (triggers internal POR circuit)
- External pin (PDn) assertion will generate POR

2-4-2. External Reset

The AW-CM389NF is reset when PDn pin is asserted low and the internal CPU begins the boot sequence when the PDn pin transitions from low to high.

2-5. Power up Timing Sequence



3. Host Interfaces

3-1. SDIO Interface

The AW-CM389NF supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless module device.

The AW-CM389NF acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

Supports SDIO 3.0 Standard

On-chip memory used for CIS

Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes

Special interrupt register for information exchange

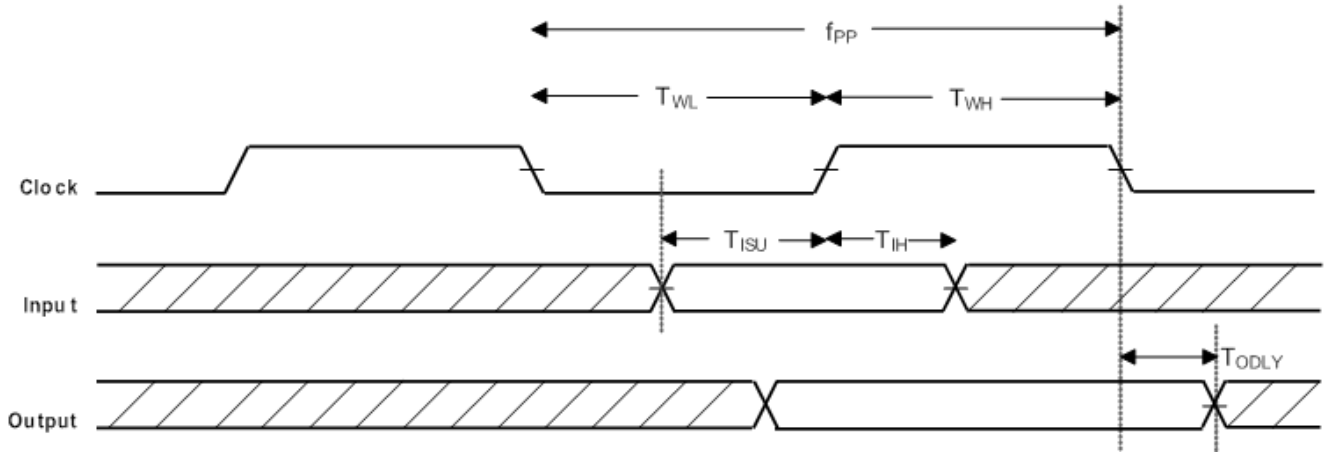
Allows card to interrupt host

3-1-1. SDIO Interface Signal Description

Pin Name	Signal Name	Type	Description
SD_CLK	CLK	I/O	SDIO 1-bit mode: Clock SDIO SPI mode: Clock
SD_CMD	CMD	I/O	SDIO 1-bit mode: Command line SDIO SPI mode: Data input
SD_DAT[3]	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (active low)
SD_DAT[2]	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPII mode: Reserved
SD_DAT[1]	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_DAT[0]	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data output

3-1-2. Default Speed, High Speed Modes (3.3V)

SDIO Protocol Timing Diagram – Default Speed Mode (3.3V)



SDIO Protocol Timing Diagram – HighSpeed Mode (3.3V)

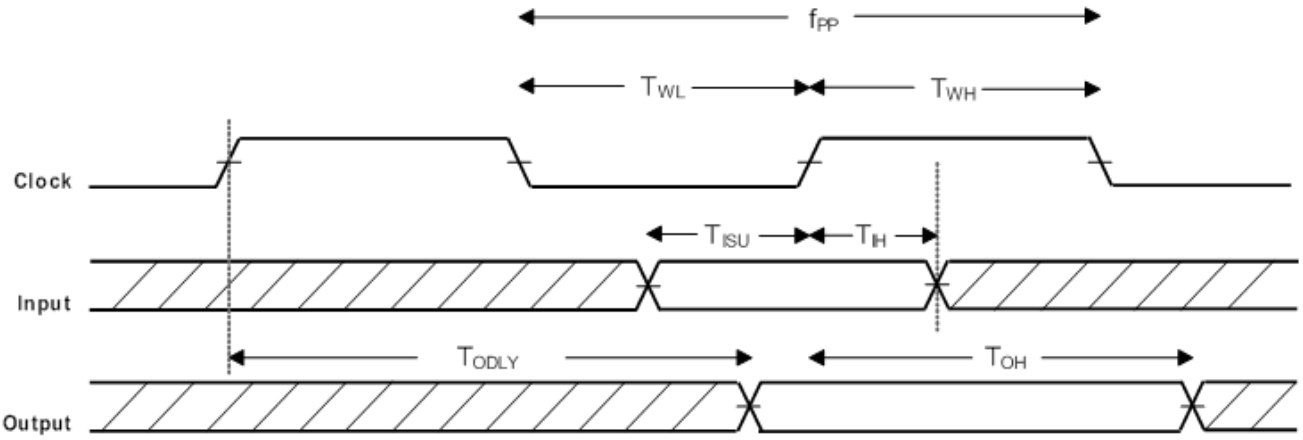


Table shows SDIO Timing Data—Default Speed, High Speed Modes (3.3V)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency	Default Speed	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WL}	Clock Low Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{WH}	Clock High Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Default Speed	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Default Speed	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time CL ≤ 40 pF (1 card)	Default Speed	--	--	14	ns
		High Speed	---	-1	4	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

3-1-3. SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

SDIO Protocol Timing Diagram – SDR12,SDR25,SDR50 Modes (up to 100MHz) (1.8V)

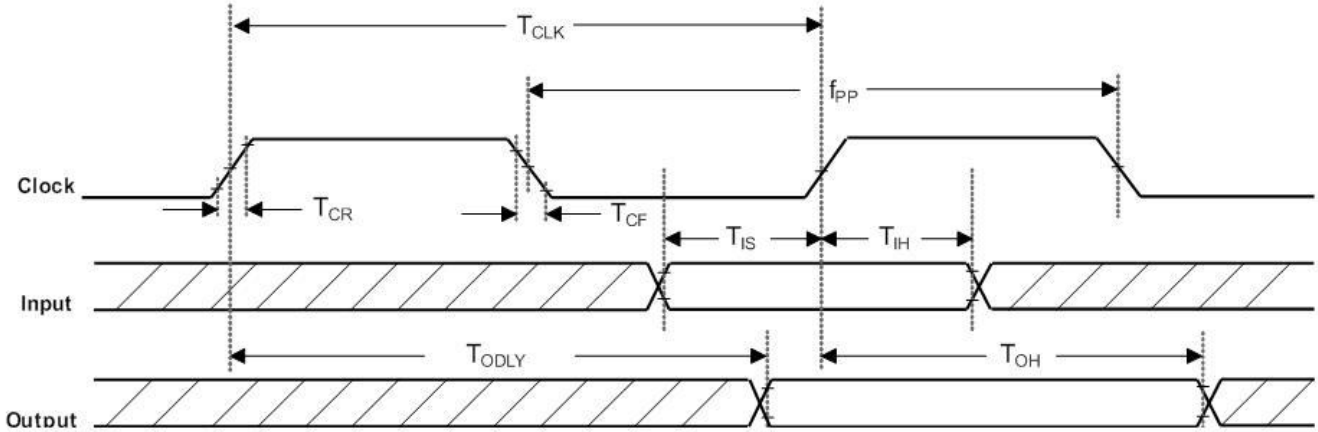


Table shows SDIO Timing Data—SDR12,SDR25,SDR50 Modes (up to 100MHz) (1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time C_L ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	--	--	ns

3-1-4. SDR104 Modes (208MHz) (1.8V)

SDIO Protocol Timing Diagram –SDR104 Mode (208MHz)

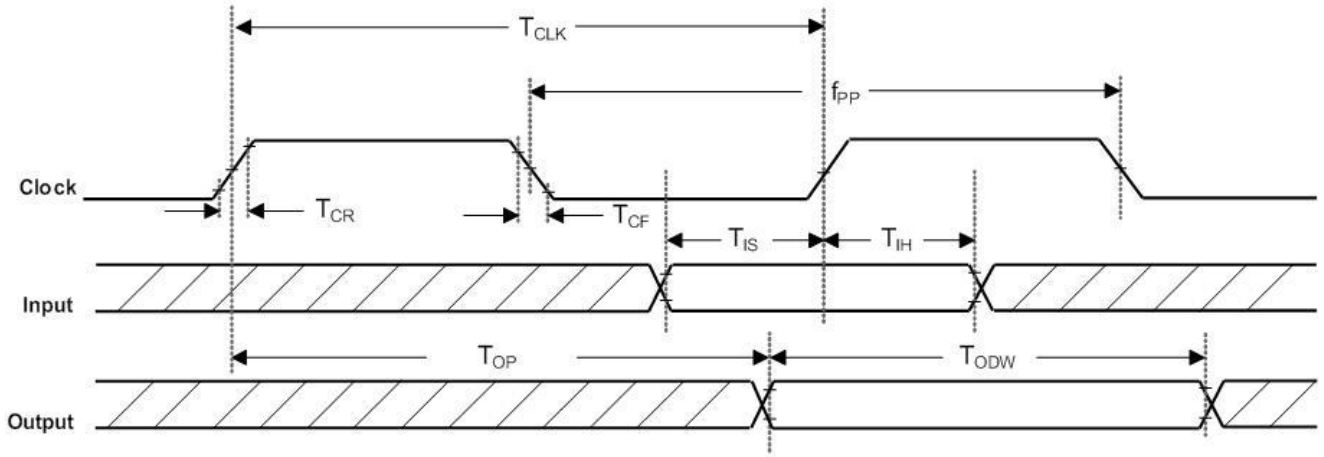


Table shows SDIO Timing Data—SDR104 Mode (208MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

3-2. PCI Express Interface

3-2-1 Differential Tx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 PPM. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Tx_DIFFpp}	Differential peak-to-peak output voltage $V_{Tx\_DIFFpp} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.800	--	1.2	V
$V_{Tx\_DE\_RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	db
T_{Rx_EYE}	Minimum Tx eye width	0.75	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.125	UI
T_{Tx_RISE}, T_{Tx_FALL}	D+/D- Tx output rise/fall time	0.125	--	--	UI
$V_{Tx\_CM\_DC\_ACTIVE\_IDLE\_DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0-	-	100	mV
$V_{Tx\_CM\_DC\_LINE\_DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0-	-	25	mV
$V_{Tx\_IDLE\_DIFFp}$	Electrical idle differential peak output voltage	0	--	20	mV
$V_{Tx\_RCV\_DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$V_{Tx\_DC\_CM}$	Tx DC common mode voltage	--	--	3.6	V
I_{Tx_SHORT}	Tx short circuit current limit	--	--	90	mA
$T_{Tx\_IDLE\_MIN}$	Minimum time spent in electrical idle	50	--	--	UI
$T_{Tx\_IDLE\_SET\_TO\_IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	20	UI
$T_{Tx\_IDLE\_TO\_DIFF\_DATA}$	Maximum time to transition to valid Tx specifications after leaving an electrical idle condition	--	--	20	UI
RL_{Tx_DIFF}	Differential return loss	10	--	--	dB
RL_{Tx_CM}	Common mode return loss	6	--	--	dB
C_{Tx}	AC coupling capacitor	75	--	200	nF
$T_{Crosstalk}$	Crosstalk random timeout	0	--	1	ms

3-2-2 Differential Rx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Rx_DIFFpp}	Differential peak-to-peak voltage $V_{Rx\_DIFFpp} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	--	1.2	V
T_{Rx_EYE}	Minimum receiver eye width	0.4	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.3	UI
$V_{Rx\_CM\_ACp}$	AC peak common mode input voltage	--	--	150	mV
RL_{Rx_DIFF}	Differential return loss	10	--	--	dB
RL_{Rx_CM}	Common mode return loss	6	--	--	dB
$Z_{Rx\_DIFF\_DC}$	DC differential input impedance	80	100	120	Ω
Z_{Rx_DC}	DC input impedance	40	50	60	Ω
$Z_{Rx\_HIGH\_IMP\_DC\_POS}$	Powered down DC input impedance positive	50	--	--	k
$Z_{Rx\_HIGH\_IMP\_DC\_NEG}$	Powered down DC input impedance negative	1	--	--	kΩ
$V_{Rx\_IDLE\_DET\_DIFFpp}$	Electrical idle detect threshold	65	--	175	mV
$T_{Rx\_IDLE\_DET\_DIFF\_ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
L_{Rx_SKEW}	Total skew	---	-2	0	ns

3-3. USB Interface

The USB device interface is compliant with the Universal Serial Bus Specification, Revision 2.0, April 27, 2000. A USB host uses the USB cable bus and the USB 2.0 device interface to communicate with the chip.

The main features of the USB device interface include:

High/full speed operation (480/12 Mbps)

Suspend/host resume/device resume (remote wake-up)

Built-in DMA engine that reduces interrupt loads on the embedded processor and reduces the system bus bandwidth requirement for serving the USB device operation

The USB 2.0 device interface is designed with 3.3V signal level pads.

3-3-1. USB 2.0 Device Interface Description

Table shows the signal mapping between the AW-CM389NF and the USB Specification, Revision 2.0.

Pin Name	USB 2.0 Specification Pin Name	Description
Pin72/ 3V3_USB	VBUS	USB Bus Power Supply On-board regulator regulates voltage from VBUS level to voltage levels used by USB PHY.
	GND	USB Bus Ground Common ground on SoC device.
Pin70/ USB_DP	D+	USB Bus Data Positive. One of the differential data pair.
Pin69/ USB_DN	D-	USB Bus Data Negative. One of the differential data pair.

3-3-2. USB 2.0 Device Functional Description

The device controller uses internal Scatter/Gather DMA engine to transfer the transmit packet from internal SRAM to USB and the receive packet from USB to internal SRAM. The Device IN Endpoint DMA (DIEPDMAn) and Device OUT Endpoint DMA (DOEPDMAn) registers are used by the DMA engine to access the base descriptor. The application is interrupted after the programmed transfer size extracted from the descriptors is transmitted or received. By using registers, interrupts, and special data structures, the device controller can communicate with the device controller driver (application/software) about bus states, host request, and data transfer status. The device controller driver also has all of the routines to respond to the device framework commands issued by a USB host, so it controls the attachment, configuration, operation, and detachment of the device.

3-4. High-Speed UART Interface

The AW-CM389NF supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data. Table shows the rates supported.

The UART interface features include:

FIFO mode permanently selected for transmit and receive operations

Two pins for transmit and receive operations

Two flow control pins

Interrupt triggers for low-power, high throughput operation

The UART interface operation includes:

Upload boot code to the internal CPU (for debug purposes)

Support diagnostic tests

Support data input/output operations for peripheral devices connected through a standard UART interface

UART Baud Rates Supported

Baud Rate				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	--

3-4-1. UART Interface Signal Description

Table shows the standard UART signal names on the device.

Signal Name	16550 Standard Pin Name	Description
Data Bus		
UART_SIN	SIN	Serial data input from modem, data set, or peripheral device
UART_SOUT	SOUT	Serial data output from modem, data set, or peripheral device
Modem Control		
UART_RTSN	RTS	Request To Send output to modem, data set, or peripheral device (active low)
UART_CTSN	CTS	Clear To Send input from modem, data set, or peripheral device (active low)

3-4-2. UART Interface Functional Description

3-3-2-1. Booting from UART

When booting from the UART, the AW-CM389NF device has the following requirements:

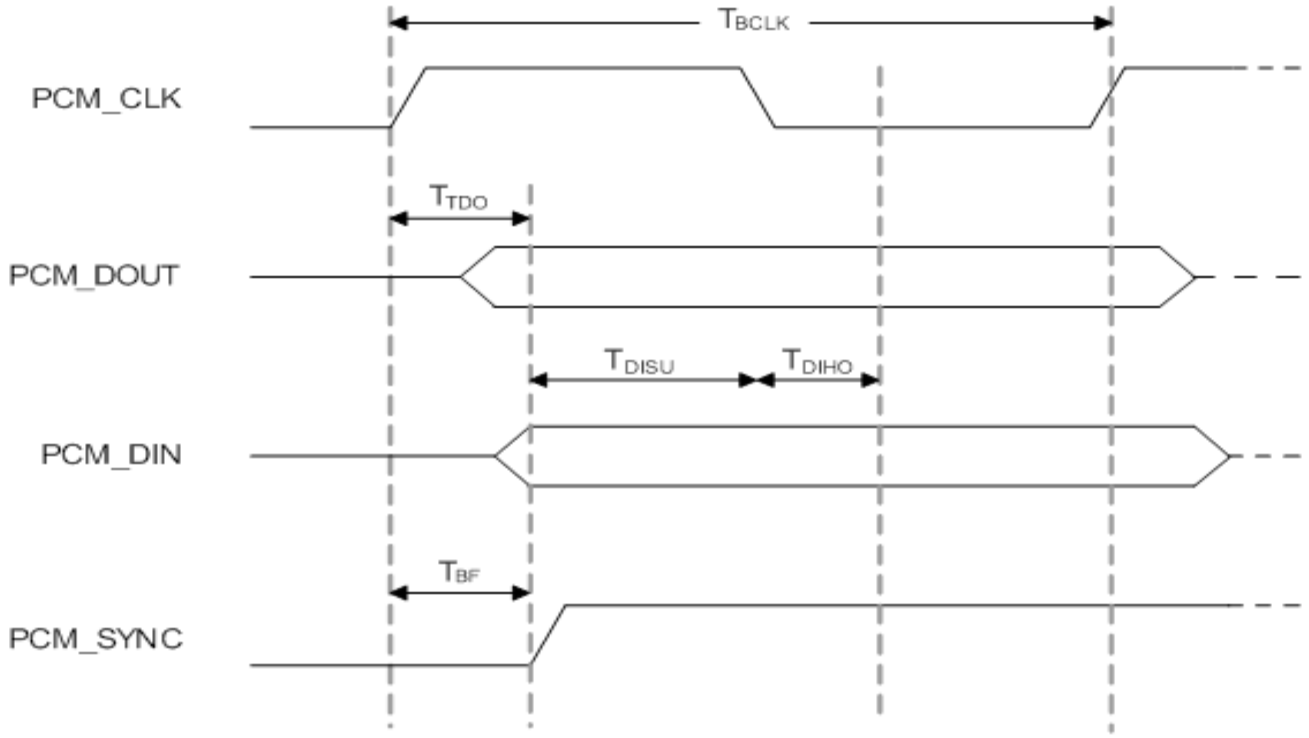
System Requirement	Description
Number of data bits	8 bits
Stop bits	1 bit
Parity	No parity
Baud Rate	115200

3-4-2-2. UART as Test Port

Test diagnostic programs may be uploaded to the CPU through the UART interface. During execution, the diagnostic program transmits performance and status information through the UART by performing a write to the PBU address space designated to the UART.

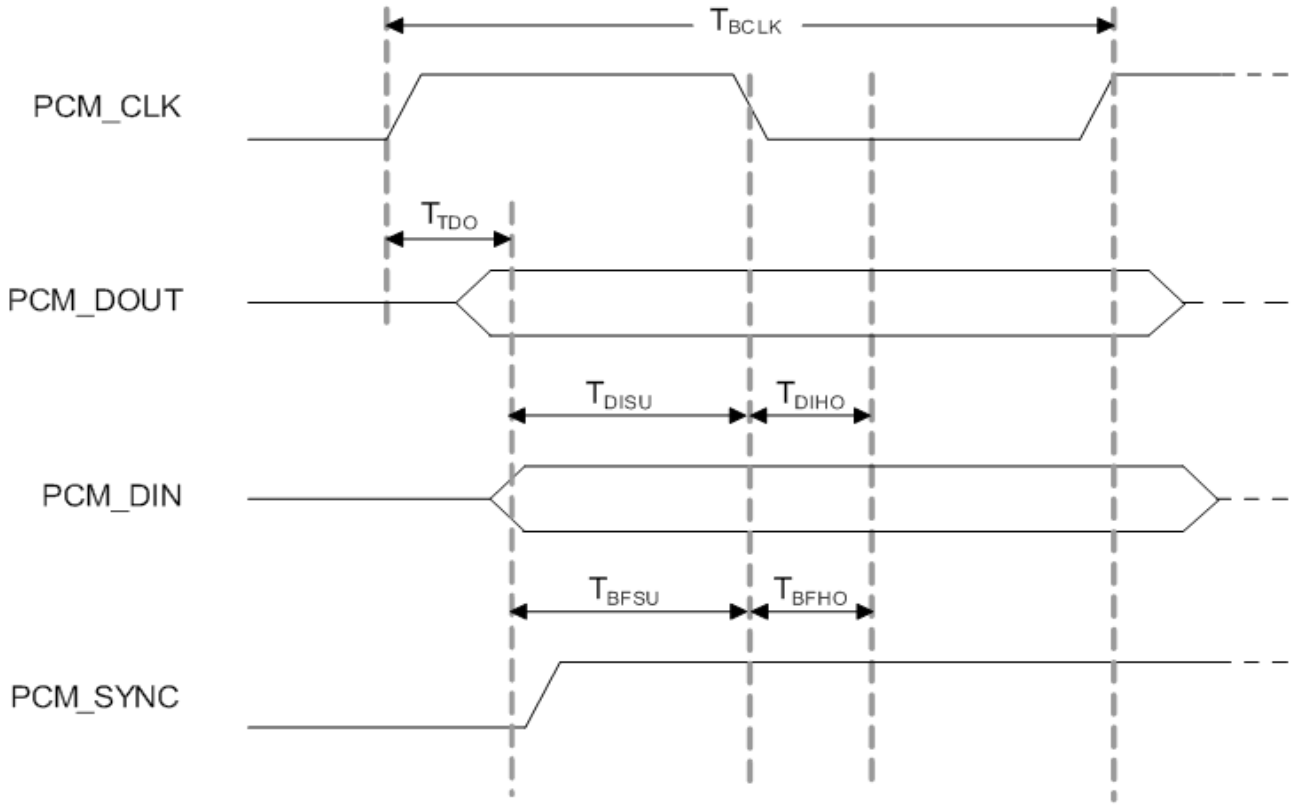
3-5. PCM Interface

3-5-1. PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

3-5-2. PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}	--	--	10	--	--	ns

4. Pin Definition

Pin No	Definition	Basic Description	Type
1	TMS	JTAG controller select	
2	TCK	JTAG test clock	
3	TDI	JTAG test data(input)	I
4	3.3V	3.3V Analog RF Power Supply	I
5	3.3V	3.3V VBAT system power supply input	I
6	GND	System Ground Pin	
7	TDO	JTAG test data(output)	O
8	CONFIG_HOST[0]	Configuration: CONFIG_HOST[0]	
9	CONFIG_HOST[1]	Configuration: CONFIG_HOST[1]	
10	CONFIG_HOST[2]	Configuration: CONFIG_HOST[2]	
11	GPIO[1]/LTE_SOUT	UART_LTE_SOUT (output)	I
12	GPIO[2]/LTE_SIN	UART_LTE_SIN (input)	I
13	CONFIG_HOST[3]	Configuration: CONFIG_HOST[3]	
14	GPIO[10]	GPIO[10] (input/output)	
15	NC	No Connect	
16	NC	No Connect	
17	GND	System Ground Pin	
18	NC	No Connect	
19	NC	No Connect	
20	GND	System Ground Pin	
21	NC	No Connect	
22	NC	No Connect	
23	GND	System Ground Pin	
24	NC	No Connect	
25	NC	No Connect	
26	GND	System Ground Pin	
27	SLP_CLK	Sleep Clock Input Used for WLAN and Bluetooth low- power modes. External sleep clock of 32.768 KHz must be used for auto reference clock calibration and for WLAN/Bluetooth low power operation.	I

Pin No	Definition	Basic Description	Type
28	GPIO[13]/BT IRQ(O)	GPIO[13] (input/output)	I/O
29	PCIE_WAKEn	PCIe wake signal (output) (active low)	O
30	PCIE_CLKREQn	PCIe clock request (input/output) (active low)	I/O
31	GPIO[12]/PCIE_PERSTn	PCIe host indication to reset the device (input) (active low)	I
32	GND	System Ground Pin	
33	PCIE_RCLK_N	PCI Express Differential Clock Input—Negative	I
34	PCIE_RCLK_P	PCI Express Differential Clock Input—Positive	I
35	GND	System Ground Pin	
36	PCIE_TX_N	PCI Express Transmit Data—Negative	O
37	PCIE_TX_P	PCI Express Transmit Data—Positive	O
38	GND	System Ground Pin	
39	PCIE_RX_N	PCI Express Receive Data—Negative	I
40	PCIE_RX_P	PCI Express Receive Data—Positive	I
41	GND	System Ground Pin	
42	GPIO[0]/CLK_REQ	GPIO[0] (input/output)	O
43	GPIO[11]	GPIO[11] (input/output)	
44	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply	I
45	PDn	Full Power Down (input) (active low)	I
46	GPIO[3]/WLAN IRQ(O)	GPIO[3] (input/output)	I
47	SD_DAT[3]	SDIO Data line Bit[3]	I/O
48	SD_DAT[2]	SDIO Data line Bit[2]	I/O
49	SD_DAT[1]	SDIO Data line Bit[1]	I/O
50	SD_DAT[0]	SDIO Data line Bit[0]	I/O
51	SD_CMD	SDIO Command/response (input/output)	I/O
52	SD_CLK	SDIO Clock input	I
53	NC	No Connect	
54	GPIO[6]	UART_CTSn (input)	I
55	GPIO[4]	UART_SOUT (output)	O
56	GPIO[5]	UART_SIN (input)	I
57	GPIO[7]	UART_RTSn (output)	O
58	GPIO[22]/PCM_SYNC	GPIO[22] (input/output)	I/O

Pin No	Definition	Basic Description	Type
59	GPIO[19]/PCM_IN	GPIO[19] (input/output)	I
60	GPIO[20]/PCM_OUT	GPIO[20] (input/output)	O
61	GPIO[21]/PCM_CLK	GPIO[21] (input/output)	I/O
62	GND	System Ground Pin	
63	GPIO[14]	GPIO[14] (input/output)	I/O
64	GPIO[8]/WLAN_LED	LED_OUT_WLAN (output)	O
65	GPIO[9]/BT_LED	LED_OUT_BT (output)	O
66	NC	No Connect	
67	NC	No Connect	
68	GND	System Ground Pin	
69	USB_DN	USB Serial Differential Data Negative	I/O
70	USB_DP	USB Serial Differential Data Positive	I/O
71	GND	System Ground Pin	
72	3V3_USB	3.3V USB Power Supply	I
73	VIO	Digital I/O Power Supply	I
74	GND	System Ground Pin	
75	GND	System Ground Pin	
76	GND	System Ground Pin	
77	GND	System Ground Pin	
78	GND	System Ground Pin	
79	GND	System Ground Pin	
80	GND	System Ground Pin	
81	GND	System Ground Pin	
82	GND	System Ground Pin	
83	GND	System Ground Pin	
84	GND	System Ground Pin	
85	GND	System Ground Pin	
86	GND	System Ground Pin	
87	GND	System Ground Pin	
88	GND	System Ground Pin	
89	GND	System Ground Pin	

Pin No	Definition	Basic Description	Type
90	GND	System Ground Pin	
91	GND	System Ground Pin	
92	GND	System Ground Pin	
93	GND	System Ground Pin	
94	GND	System Ground Pin	
95	GND	System Ground Pin	
96	GND	System Ground Pin	
G1	GND	System Ground Pin	
G2	GND	System Ground Pin	
G3	GND	System Ground Pin	
G4	GND	System Ground Pin	
G5	GND	System Ground Pin	
G6	GND	System Ground Pin	
G7	GND	System Ground Pin	
G8	GND	System Ground Pin	
G9	GND	System Ground Pin	
G10	GND	System Ground Pin	
G11	GND	System Ground Pin	
G12	GND	System Ground Pin	
G13	GND	System Ground Pin	
G14	GND	System Ground Pin	
G15	GND	System Ground Pin	
G16	GND	System Ground Pin	
G17	GND	System Ground Pin	
G18	GND	System Ground Pin	
G19	GND	System Ground Pin	
G20	GND	System Ground Pin	
G21	GND	System Ground Pin	
G22	GND	System Ground Pin	
G23	GND	System Ground Pin	
G24	GND	System Ground Pin	

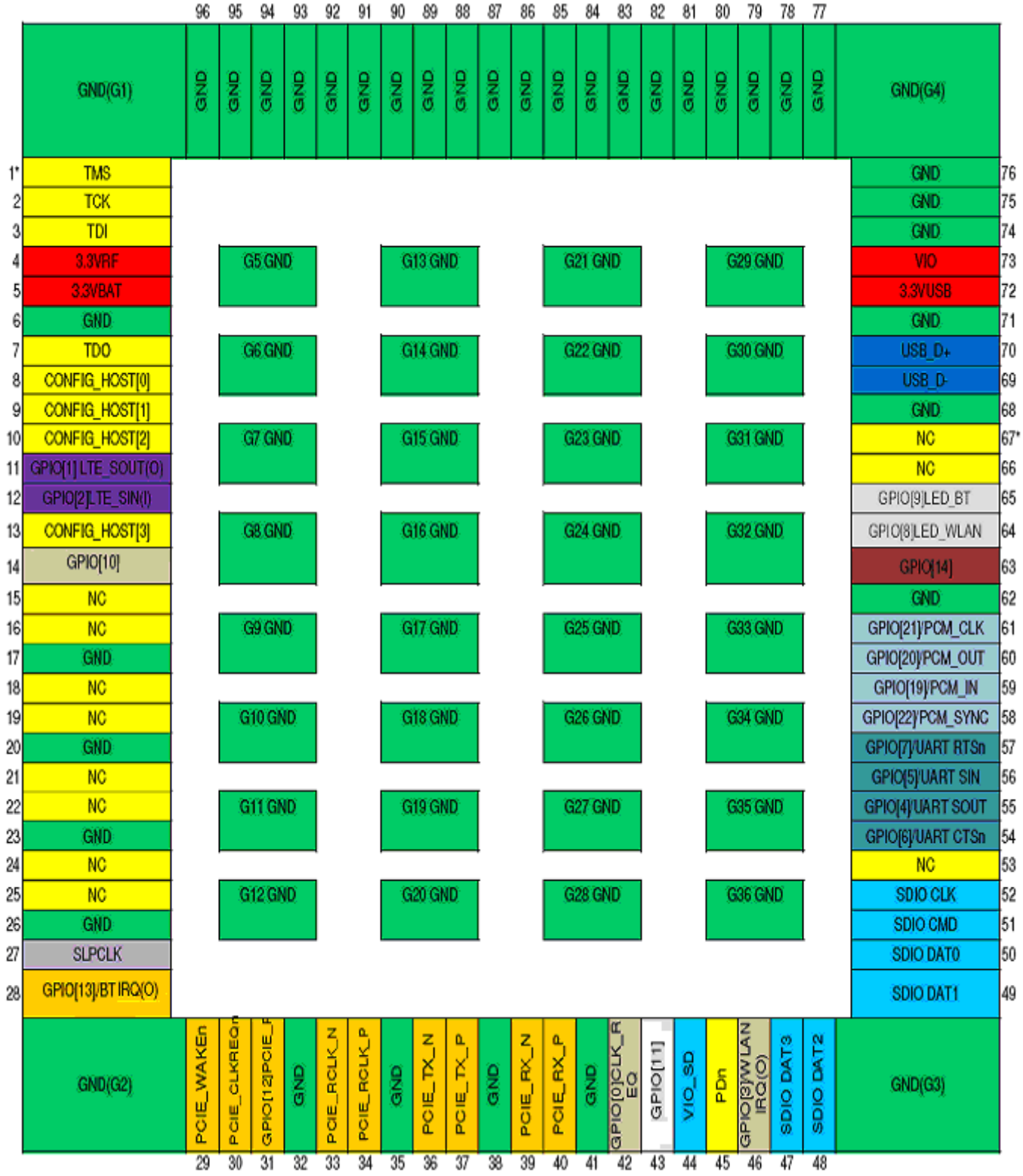
Pin No	Definition	Basic Description	Type
G25	GND	System Ground Pin	
G26	GND	System Ground Pin	
G27	GND	System Ground Pin	
G28	GND	System Ground Pin	
G29	GND	System Ground Pin	
G30	GND	System Ground Pin	
G31	GND	System Ground Pin	
G32	GND	System Ground Pin	
G33	GND	System Ground Pin	
G34	GND	System Ground Pin	
G35	GND	System Ground Pin	
G36	GND	System Ground Pin	

Notes:

1. SDIO signals should have 50 ohm impedances.
2. For SDIO interface, 33ohm inline resistor may be needed to help with signal integrity.
3. For GPIO[8] ,it's internal pull up to VIO-RF(3.3V).
4. For GPIO[9] ,it's internal pull up to VIO-RF(3.3V).
5. For PDn pin ,please pull up resistor(51k ohm) to host or VBAT(3V3).
6. For SDIO interface, the pull up value is between 10K to 100K ohm according to the SDIO v3.0 SPEC.
7. PCIE Impedance targets: Single-ended Z of 60 ohms +- 15% . Differential Impedance of ~100 ohm +- 20%.
8. USB Impedance targets: D+/D- are differential and should have 90ohms impedance.
9. For GPIO[3] pin ,please pull up resistor(10k ohm) to VIO.

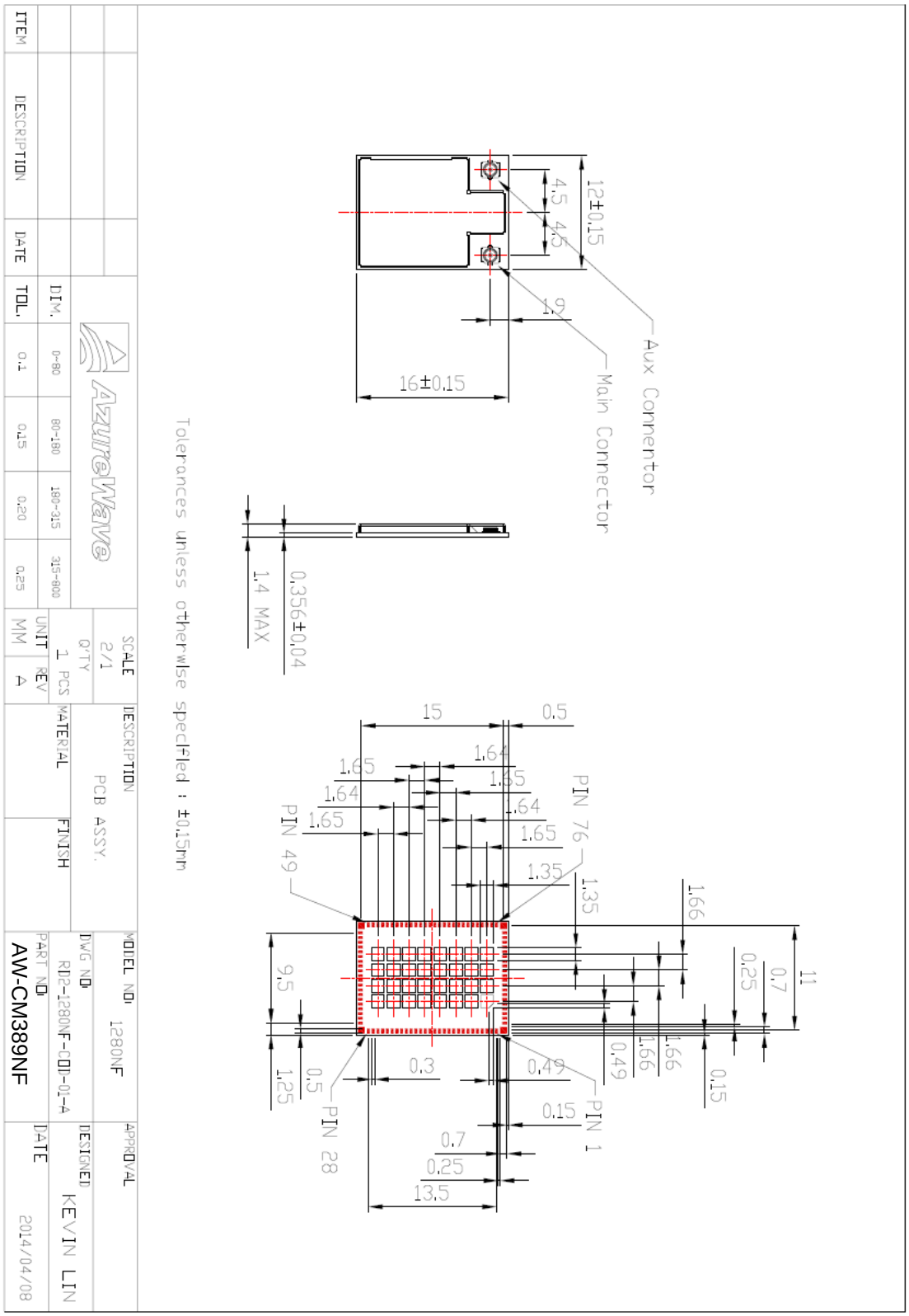
4-1 Pin Map

AW-CM389NF Top View Pin Map



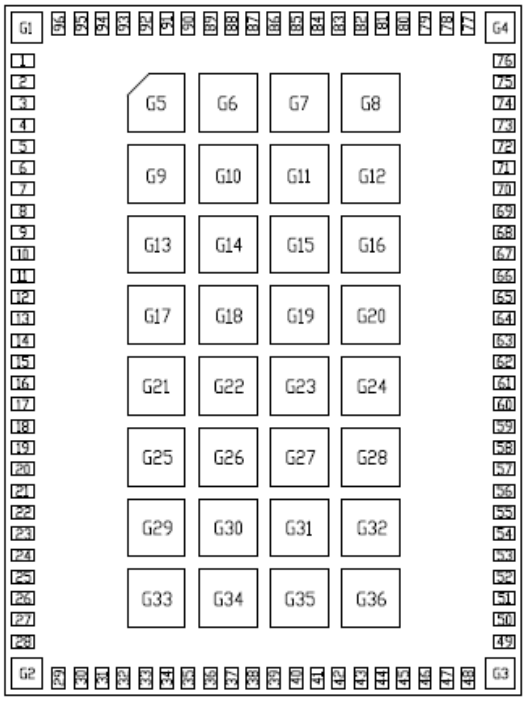
5. Mechanical Information

5-1. Package Outline Drawing

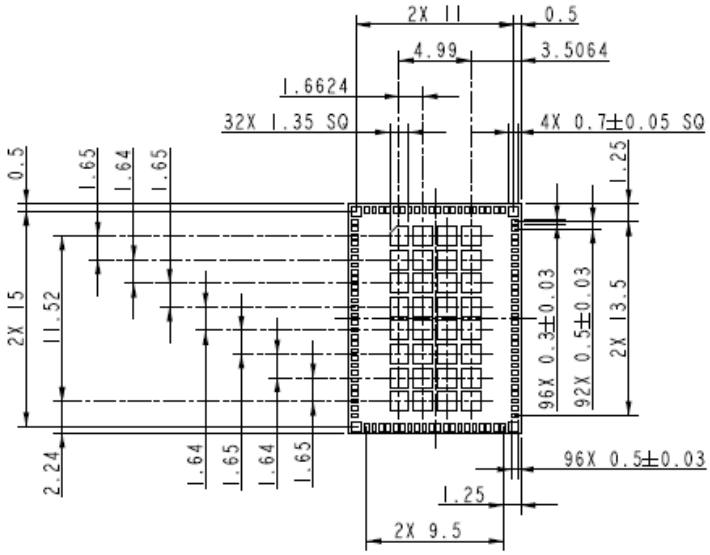


5-2. Module Footprint

AW-CM389NF PCB Layout Footprint



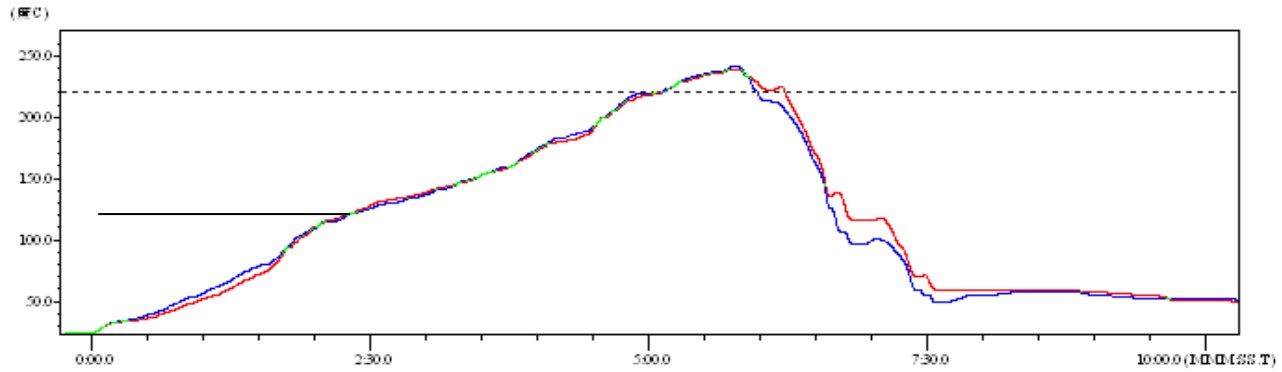
TOP VIEW



6. Package Information

6-1. Recommended Reflow Profile

Reflow Soldering Profile



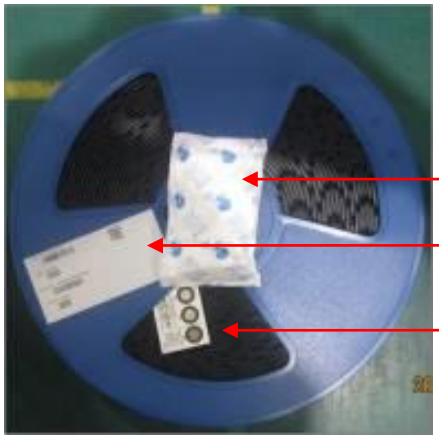
No	Item	Temperature(℃)	Time(sec)
1	Reflow Time	Time of above 220℃	35~55sec
2	Peak-Temp	260℃ max	

Note:

1. **Recommend to supply N_2 for reflow oven**
2. **N_2 atmosphere during reflow (O_2<300ppm)**

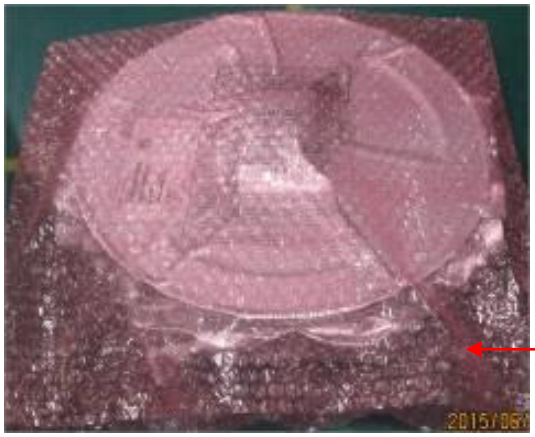
7. Shipping Information

7-1



7-2

7-3



7-4

7-5

1 Carton= 5 Boxes

7-6

Note: 1 tape reel = 1 box = 1,500pcs

1 carton = 5 boxes = 5 * 1,500pcs=7,500pcs