AzureWave Technologies, Inc.

AW-CM358SM

IEEE 802.11a/b/g/n/ac WLAN with Bluetooth 5 Combo Stamp Module

Datasheet

Rev. 0A

(For Standard)

Features

WLAN

- 1 antennas to support 1(Transmit) × 1(Receive) technology and Bluetooth
- High speed wireless connection up to 433.3Mbps transmit/receive PHY rate using 80MHz bandwidth
- Backward compatibility with legacy 802.11n/a/g/b technology.
- 20MHz bandwidth/ channel, 40MHz bandwidth/ channel, upper/ lower 20MHz packets in 40MHz channel, 20MHz duplicate legacy packets in 40MHz channel mode operation.
- 80MHz bandwidth/ channel, 4 positions of 20MHz packets in 80MHz channel, upper/ lower 40MHz packets in 80MHz channel, 20MHz quadruplicate legacy packets in 80MHz channel mode operation.
- Dynamic frequency selection (radar detection)

Bluetooth

- Baseband and radio BDR and EDR packet types – 1Mbps (GFSK), 2Mbps (π/4-DQPSK), and 3Mbps (8DPSK).
- Fully qualified Bluetooth BT4.2 and support Bluetooth 5.
- Enhanced Data Rate (EDR) compliant for both 2Mbps and 3Mbps supported.
- High speed UART and PCM for Bluetooth.
- Fully functional Bluetooth baseband-AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening.
- Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER).
- SCO/ eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement.
- Standard Bluetooth power saving mechanisms.
- Automatic ACL packet type selection.
- Full master and slave piconet support.
- Scatternet support.

- Enhanced radar detection for long and short pulse radar.
- Enhanced AGC scheme for DFS channel.
- 20/40/80Mhz coexistence with middle-packet detection (GI detection) for enhanced CCA.
- 1 spatial stream STBC reception.
- LDPC transmission and reception for both 802.11n and 802.11ac.
- 256 QAM (MCS 8, 9) modulation, optional support for 802.11ac MCS 9 in 20MHz using LDPC.
- Short guard interval.
- Temporal Ley Integrity Protocol (TKIP)/ Wired Equivalent Privacy (WEP)/ Advanced Encryption Standard (AES)/ Counter-Mode/ CBC-MAC Protocol (CCMP).
- Cipher-Based Message Authentication Code (CMAC)/ WLAN Authentication and Privacy Infrastructure (WAPI).
- External Crystal frequency

- Enhanced Power Control (EPC).
- Channel Quality Driven Data Rate (CQDDR).
- Encryption (AES) support.
- Supports link layer topology to be master and slave (connects up to 16 links).
- LE Privacy 1.2
- LE Secure Connection.
- LE Data Length Extension.
- 2 Mbps LE
- Direction Finding – Connectionless Angle of Departure (AoD).
- Direction Finding – Connection – oriented Angle of Arrival (AoA)

Revision History

Document NO: R2-2358SM-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
Version 0. 1	2018/01/18		Initial Version	N.C. Chen	Chihhao Liao
Version 0. 2	2018/10/18		WLAN Spec update	JM.Pang	Chihhao Liao
Version 0. 3	2018/10/18		Pin Table update	JM.Pang	Chihhao Liao
Version 0. 4	2018/11/21		Electrical Characteristics Specifications update	JM.Pang	Chihhao Liao
Version 0. 5	2019/01/16		WLAN Spec update	JM.Pang	Chihhao Liao
Version 0. 6	2019/06/14		1.3 Block Diagram update	JM.Pang	Chihhao Liao
Version 0. 7	2019/07/29		Update 1.4.3 Bluetooth 2.2 Pin Table 3.4 Power up Timing Sequence	JM.Pang	Chihhao Liao
Version 0. 8	2019/08/06		Modify 3.4 Power up Timing Sequence	JM.Pang	Chihhao Liao
Version 0A	2019/08/21	DCN015757	Datasheet format update	JM.Pang	Chihhao Liao

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1. Introduction

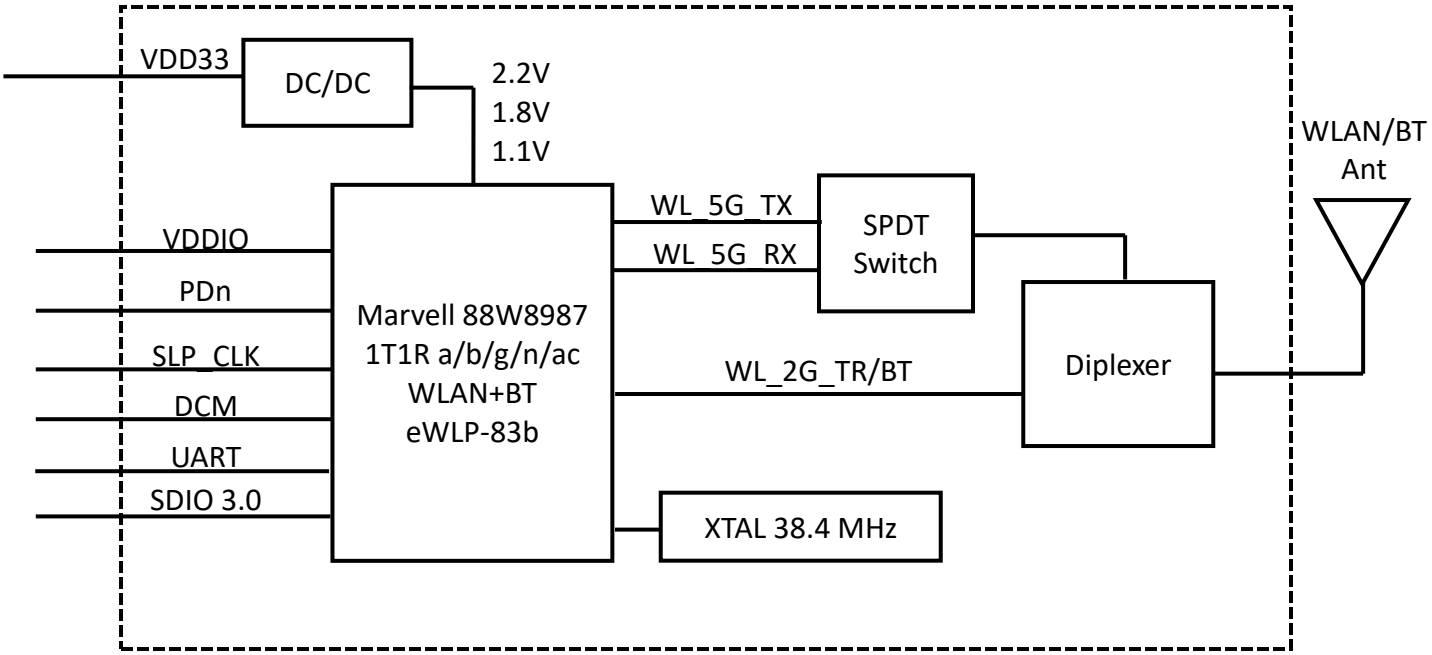
1.1 Product Overview

AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.11 a/b/g/n/ac WIFI with Bluetooth 5 combo SDIO and UART Stamp Module --- **AW-CM358SM.** The AW-CM358SM IEEE 802.11 a/b/g/n/ac WIFI with Bluetooth 5 combo module is a highly integrated wireless local area network (WLAN) solution to let users enjoy the digital content through the latest wireless technology without using the extra cables and cords. It combines with Bluetooth 4.2 and provides a complete 2.4GHz Bluetooth system which is fully compliant to Bluetooth 4.2 and v2.1 that supports EDR of 2Mbps and 3Mbps for data and audio communications. It enables a high performance, cost effective, low power, compact solution that easily fits onto the SDIO and UART combo stamp module. Generic interfaces include SDIO 3.0 and high-speed UART interfaces for connecting WLAN and Bluetooth technologies to the host processor.

AW-CM358SM uses Direct Sequence Spread Spectrum (DSSS), Orthogonal Frequency Division Multiplexing (OFDM), BPSK, QPSK, CCK and QAM baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM358SM. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, It also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP)**, Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms. For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported. The device also supports 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

Wireless home audio and video entertainment systems including DVT, set-top boxes, blue-ray DVD players, media servers, and gaming consoles. Mobile routers and Internet of Things (IoT) gateways. AW-CM358SM module adopts Marvell's latest highly-integrated WLAN & Bluetooth SoC---**88W8987**. All the other components are implemented by all means to reach the mechanical specification required.

1.2 Block Diagram



AW-CM385SM BLOCK DIAGRAM

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac Wi-Fi with Bluetooth 5 combo stamp module
Major Chipset	Marvell 88W8987
Host Interface	Wi-Fi: SDIO , BT: UART
Dimension	12 mm X 12mm x 1.65 mm
Package	Stamp module
Antenna	Single (1X1)
Weight	0.5 g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE802.11 a/b/g/n/ac
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	802.11a/g/n/ac: OFDM 802.11b: CCK(11, 5.5Mbps), DQPSK(2Mbps), BPSK(1Mbps)
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 802.11g: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13

802.11n:

USA and Canada – 1 ~ 11

Most European Countries – 1 ~ 13

802.11a:

USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

Output Power (Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<35%	14	16	18	dBm
11g (54Mbps) @EVM≦-27 dB	12	14	16	dBm
11n (HT20 MCS7) @EVM≦-28 dB	11	13	15	dBm
11n (HT40 MCS7) @EVM≦-28 dB	10	12	14	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM≦-27 dB	11	13	15	dBm
11n (HT20 MCS7) @EVM≦-28 dB	8	10	12	dBm
11n (HT40 MCS7) @EVM≦-28 dB	8	10	12	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	8	10	12	dBm
11ac (VHT40 MCS9) @EVM≦-32 dB	7	9	11	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	6	8	10	dBm

Receiver Sensitivity

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-87	-84	dBm
11g (54Mbps)		-73	-70	dBm
11n (HT20 MCS7)		-69	-66	dBm
11n (HT40 MCS7)		-67	-64	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		-71	-68	dBm
11n (HT20 MCS7)		-67	-64	dBm

	11n (HT40 MCS7)		-63	-60	dBm
	11ac (VHT20 MCS8)		-67	-64	dBm
	11ac (VHT40 MCS9)		-59	-56	dBm
	11ac (VHT80 MCS9)		-55	-52	dBm
Data Rate	WLAN: 802.11b : 1, 2, 5.5, 11Mbps 802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac/n : Maximum data rates up to 86.7 Mbps(20MHz channel),200 Mbps (40 MHz channel), 433 Mbps (80 MHz channel)				
Security	WPA/WPA2 and WEP 64-bit and 128-bit encryption Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP) Wired Equivalent Privacy (WEP) /Temporal Key Integrity Protocol (TKIP) Advanced Encryption Standard (AES)/Cipher-Based Message Authentication Code (CMAC) WLAN Authentication and Privacy Infrastructure (WAPI)				

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	Description
Bluetooth Standard	BT4.2+Enhanced Data Rate (EDR) Bluetooth 5 support
Bluetooth VID/PID	N/A
Frequency Rage	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: π/4-DQPSK Payload 3M: 8DPSK

Output Power

	Min	Typ	Max	Unit
BDR	0	2	4	dBm
EDR	-4	-1	1	dBm
Low Energy	0	2	4	dBm

Receiver Sensitivity

BT Sensitivity (BER<0.1%)

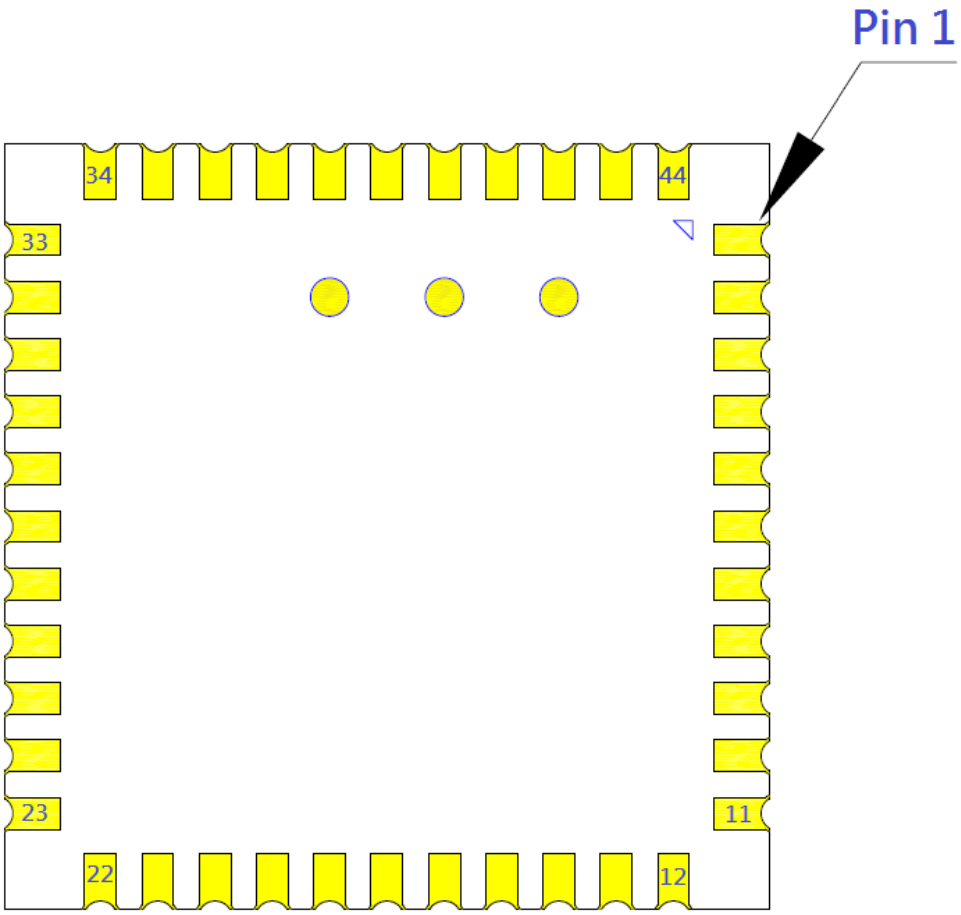
	Min	Typ	Max	Unit
GFSK		-88	-86	dBm
π/4-DQPSK		-88	-86	dBm
8DPSK		-80	-78	dBm

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT: 3.07~3.53 VIO : 1.8 ~ 3.3V
Operating Temperature	-30 to +85 °C
Operating Humidity	Less than 60%R.H.
Storage Temperature	-40 to +105 °C
Storage Humidity	Less than 85%R.H.
ESD Protection	
Human Body Model	>2KV per MIL-STD-883H Method 3015.8
Changed Device Model	>500V per JEDEC EIA/JESD22-C101E

2. Pin Definition

2.1 Pin Map



AW-CM358SM Bottom View Pin Map

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
3	GND	Ground.		GND
4	NC	Floating Pin, No connect to anything.		Floating
5	NC	Floating Pin, No connect to anything.		Floating
6	HOST_WAKE_BT	Host wake-up Bluetooth device		I
7	BT_WAKE_HOST	Bluetooth device to wake-up Host		O
8	NC	Floating Pin, No connect to anything.		Floating
9	VBAT	3.3V power pin	3.3V	VCC
10	XTAL_IN	Crystal Input(38.4MHz)		I
11	XTAL_OUT	Crystal Output(38.4MHz)		O
12	PDn	Power up/ down internal regulators. 0 = full power-down mode 1 = normal mode Default pull high in module internal		I
13	WL_HOST_WAKE	WLAN to wake-up HOST		O
14	SDIO_DATA2	SDIO Data Line 2		I/O
15	SDIO_DATA3	SDIO Data Line 3		I/O
16	SDIO_CMD	SDIO Command Input		I/O
17	SDIO_CLK	SDIO Clock Input		I
18	SDIO_DATA0	SDIO Data Line 0		I/O
19	SDIO_DATA1	SDIO Data Line 1		I/O
20	GND	Ground.		GND
21	VIN_LDO_OUT	Switch Node of Internal DC-DC convertor	1.8V	VCC
22	VDDIO	1.8V-3.3V VDDIO supply for WLAN and Bluetooth	1.8V/3.3V	VCC
23	VIN_LDO	DC-DC convertor to supply AVDD18 of IC	1.8V	VCC
24	SUSCLK_IN	External 32K or RTC clock		I
25	BT_PCM_OUT	PCM data out		O
26	BT_PCM_CLK	PCM Clock		I/O
27	BT_PCM_IN	PCM data Input		I
28	BT_PCM_SYNC	PCM Synchronization control		O
29	NC	Floating Pin, No connect to anything.		Floating
30	NC	Floating Pin, No connect to anything.		Floating
31	GND	Ground.		GND
32	NC	Floating Pin, No connect to anything.		Floating
33	GND	Ground.		GND
34	NC	Floating Pin, No connect to anything.		Floating
35	NC	Floating Pin, No connect to anything.		Floating

36	GND	Ground.		GND
37	NC	Floating Pin, No connect to anything.		Floating
38	NC	Floating Pin, No connect to anything.		Floating
39	HOST_WL_WAKE	Host wake-up WLAN device		Floating
40	NC	Floating Pin, No connect to anything.		Floating
41	UART_RTS_N	High-Speed UART RTS		O
42	UART_TXD	High-Speed UART Data Out		O
43	UART_RXD	High-Speed UART Data In		I
44	UART_CTS_N	High-Speed UART CTS		I
45	TP1 (NC)	Floating Pin, No connect to anything.		Floating
46	TP2 (NC)	Floating Pin, No connect to anything.		Floating
47	TP3 (NC)	Floating Pin, No connect to anything.		Floating

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD33	DC supply for the 3.3V input	-0.5	3.3	4.0	V
VDDIO	DC supply voltage for digital I/o		3.3	4.0	V
			1.8	2.2	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD33	DC supply for the 3.3V input	3.07	3.3	3.53	V
VDDIO	DC supply voltage for digital I/O	3.07	3.3	3.53	V
		1.67	1.8	1.98	V

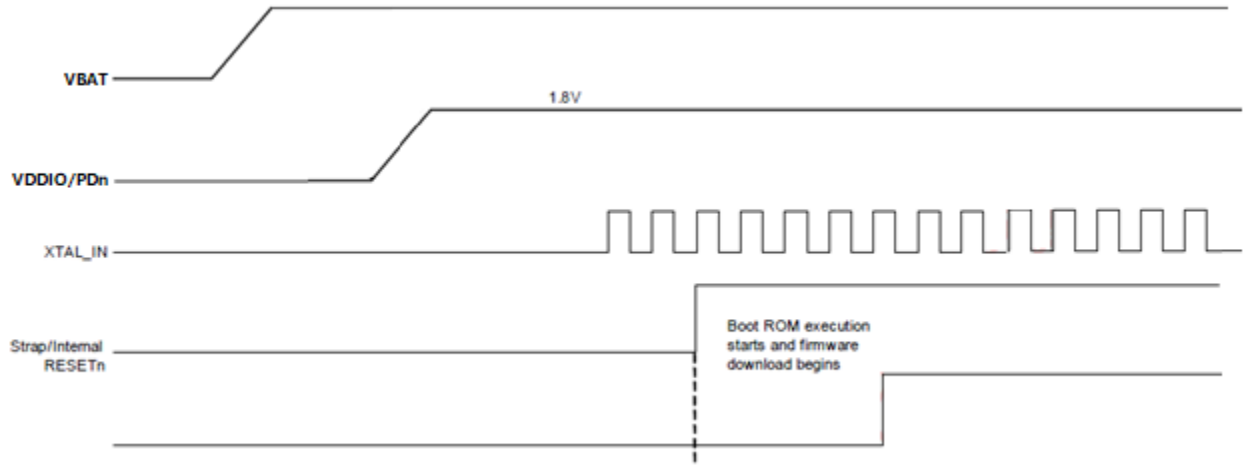
3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital I/O pins, VDDIO=1.8V					
V_{IH}	Input high voltage	1.26	-	2.2	V
V_{IL}	Input low voltage	-0.4	-	0.54	V
V_{OH}	Output High Voltage	1.4	-	-	V
V_{OL}	Output Low Voltage	-	-	0.4	V
Digital I/O pins, VDDIO=3.3V					
V_{IH}	Input high voltage	2..31	-	3.7	V
V_{IL}	Input low voltage	-0.4	-	0.99	V
V_{OH}	Output High Voltage	2.9	-	-	V
V_{OL}	Output Low Voltage	-	-	0.4	V

3.4 Power up Timing Sequence

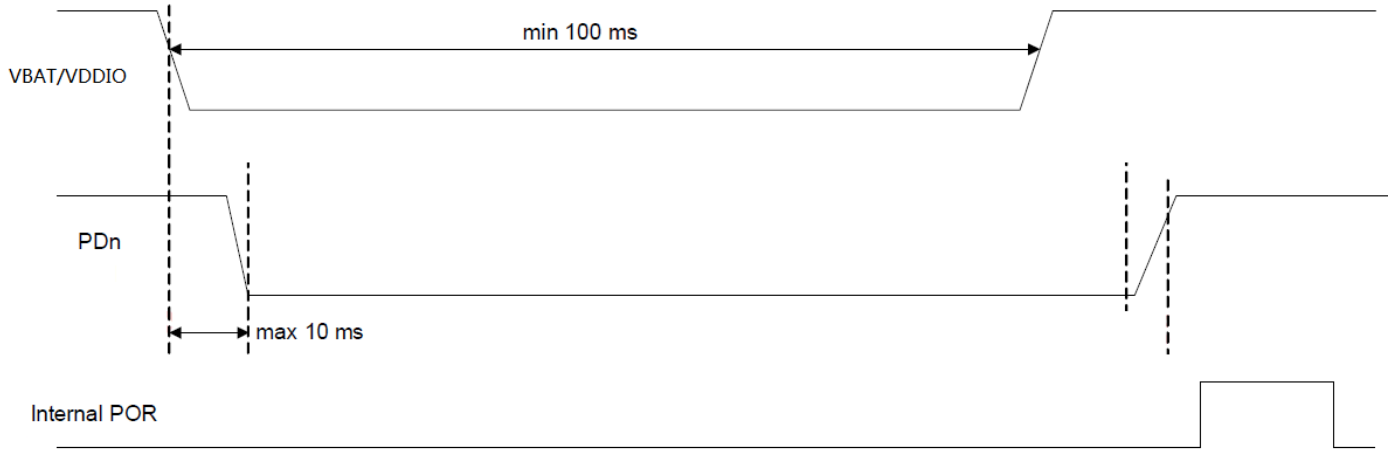
Power-up Sequence

VDDIO/Pdn no specific time requirement, just need to follow up the power on sequence waveform.



Power-down Sequence

The table is AW-CM358SM module power down sequence, the maximum ramp-down time for PDn from VBAT assertion is 10ms.VBAT must be asserted a minimum of 100 ms to guarantee that PDn are discharged to less than 0.2V for the POR generate properly after VBAT is deasserted.



3.4.1 SDIO Host Interface Specification

The AW-CM358SM supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-CM358SM acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the frvice through the use of BARs and a DMA engine.

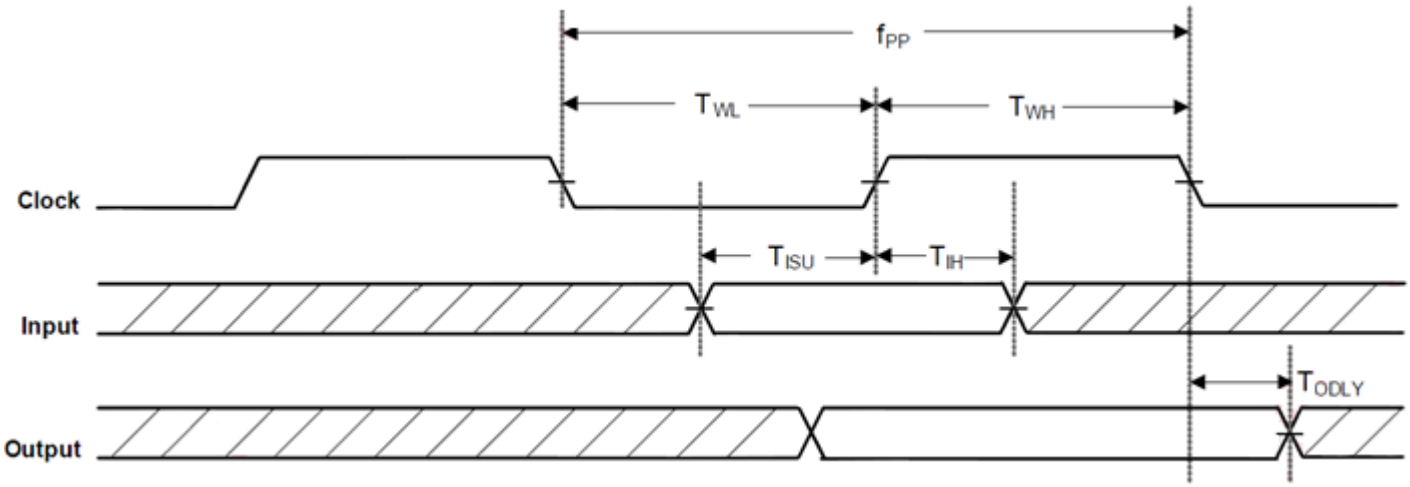
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.

SDIO Interface Signals

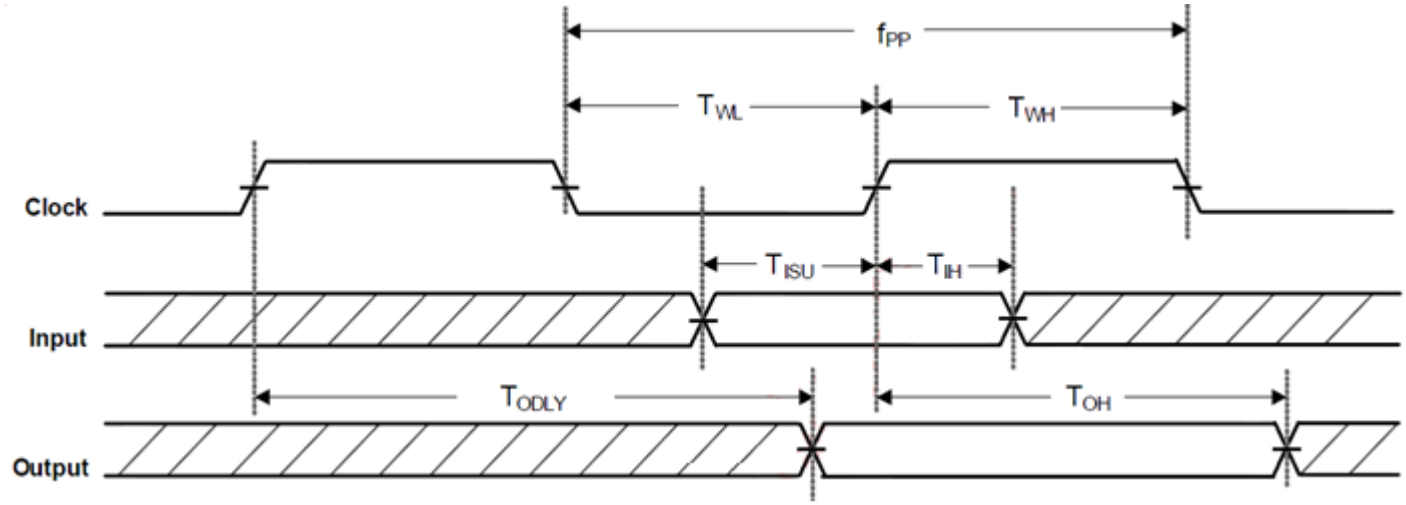
AW-CM358SM SDIO Pin Name	Type	Description
SDIO_DATA_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_DATA_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA_3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA_2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA_1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA_0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

Default Speed, High-Speed Modes

SDIO Protocol Timing Diagram – Default Speed Mode (3.3V)



SDIO Protocol Timing Diagram – High Speed Mode (3.3V)



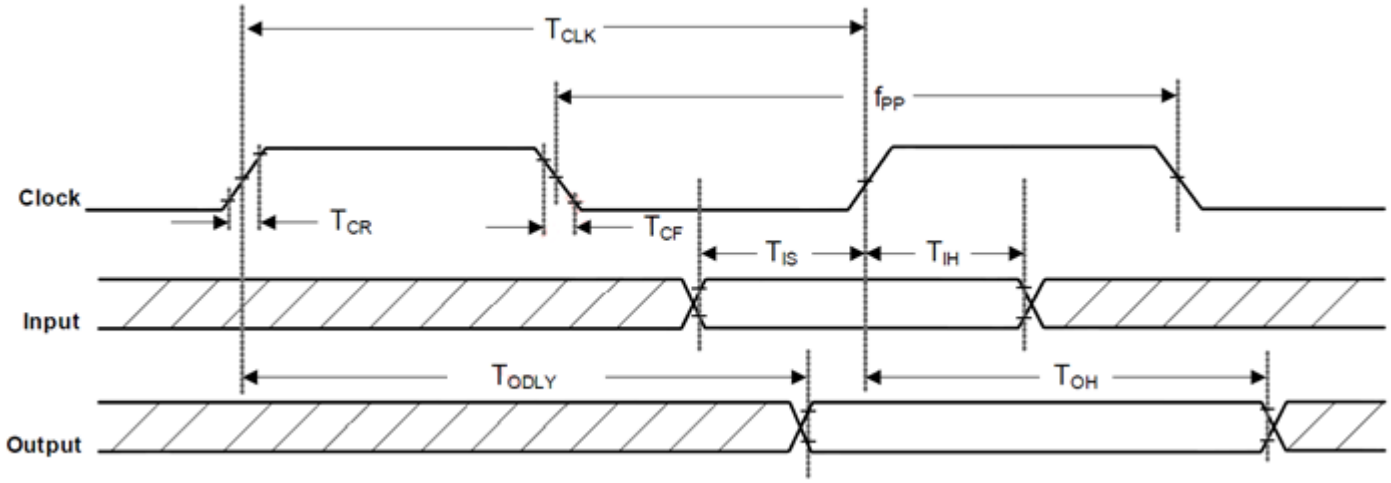
SDIO Timing Data- Default Speed, High-Speed Modes (3.3V)

Symbol	Parameter	Condition	Min	Max	Units
f_{pp}	CLK Frequency	Normal	0	25	MHz
		High Speed	0	50	
t_{WL}	CLK low Time	Normal	10	-	ns
		High Speed	7	-	
t_{WH}	CLK High Time	Normal	10	-	
		High Speed	7	-	
t_{ISU}	Input Setup Time	Normal	5	-	
		High Speed	6	-	

t_{IH}	Input Hold Time	Normal	5	-	
		High Speed	2	-	
t_{ODLY}	Output Delay Time	Normal	-	14	
		High Speed	-	14	
T_{OH}	Output hold time	High Speed	2.5		

1. For SDIO 2.0 running at 50MHz clock frequency, only 1.8V is supported.
2. For SDIO 2.0 running at 25MHz clock frequency, 1.8V or 3.3V is supported.

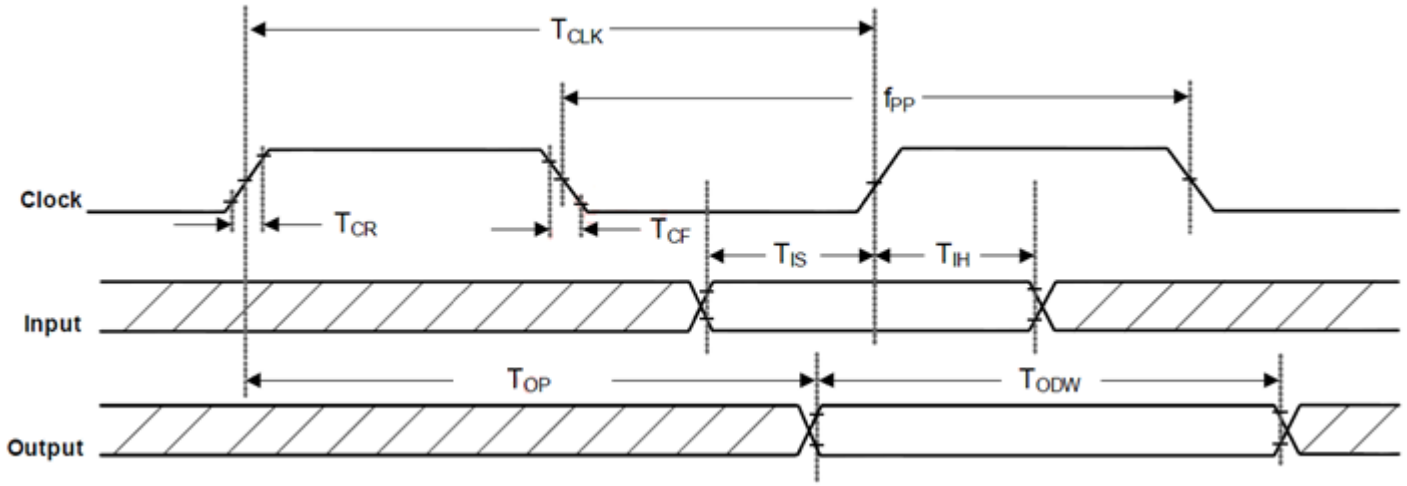
SDIO Protocol Timing Diagram – SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)



SDIO Timing Data- SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	-	-	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	-	-	ns
T_{CLK}	Clock time	SDR12/25/50	10	-	40	ns
T_{CR}, T_{CF}	Rise time, fall time	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output hold time	SDR12/25/50	1.5	-	-	ns

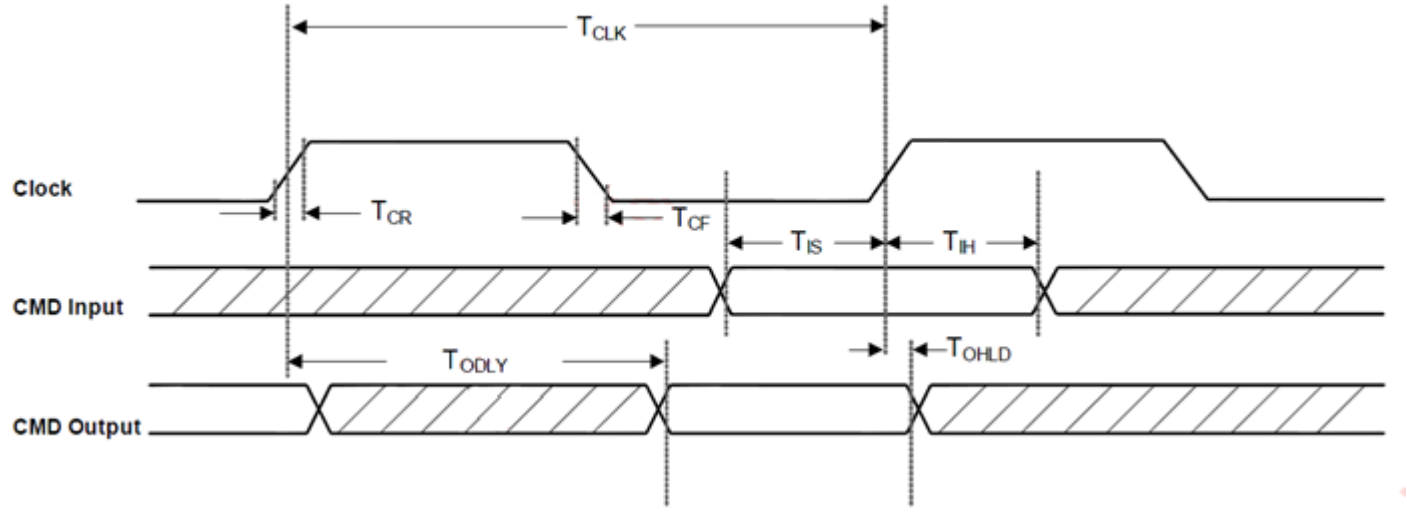
SDIO Protocol Timing Diagram – SDR104 Mode (208MHz)



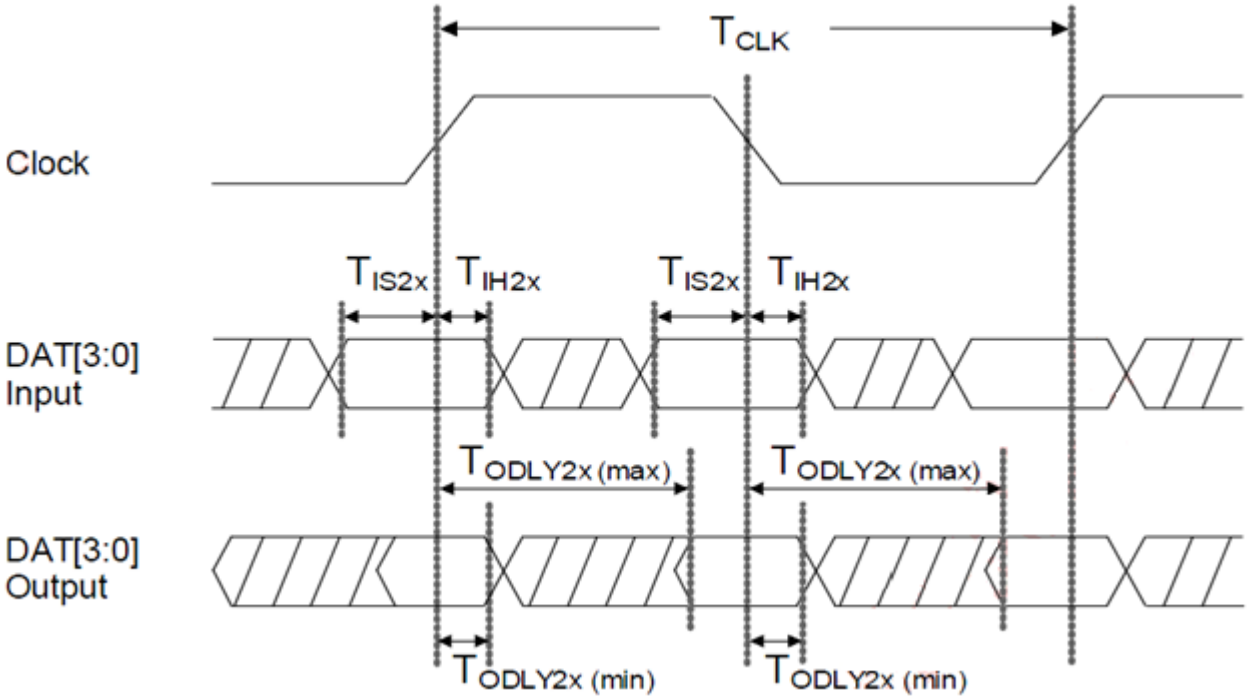
SDIO Timing Data- SDR104 Mode (208MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	CLK Frequency	SDR104	0	-	208	MHz
T_{IS}	Input setup time	SDR104	1.4	-	-	ns
T_{IH}	Input hold time	SDR104	0.8	-	-	ns
T_{CLK}	Clock time	SDR104	4.8	-		ns
T_{CR}, T_{CF}	Rise time, fall time	SDR104	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time	SDR104	0	-	10	ns
T_{OH}	Output hold time	SDR104	2.88	-	-	ns

SDIO CMD Timing Diagram – DDR50 Mode (50MHz)



SDIO SAT [3:0] Timing Diagram – SDR50 Mode (50MHz)



SDIO Timing Data- DDR50 Mode (50MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time	DDR50	20	-	-	ns
T_{CR}, T_{CF}	Rise time, fall time	DDR50	-	-	0.2*T_{CLK}	Ns
Clock Duty		DDR50	45	-	55	%
CMD Input						
T_{IS}	Input setup time	DDR50	6	-	-	ns
T_{IH}	Input hold time	DDR50	0.8	-	-	ns
CMD Output						
T_{ODLY}	Output delay time during data transfer mode	DDR50	-	-	13.7	ns
T_{OHLD}	Output hold time	DDR50	1.5	-	-	ns
DAT [3:0] Input						
T_{IS2X}	Input hold time	DDR50	3	-	-	ns
T_{IH2X}	Input hold time	DDR50	0.8	-	-	ns
DAT [3:0] Output						
$T_{ODLY2X(max)}$	Output delay time during data transfer mode	DDR50	-	-	7	ns
$T_{ODLY2X(min)}$	Output hold time	DDR50	1.5	-	-	ns

3.4.2 UART Interface

High-Speed UART interface

The AW-CM358SM supports a high-speed Universal Asynchronous Receiver/ Transmitter (UART) interface, compliant to the industry standard 16550 specification.

- FIFO mode permanently selected for transmit and receive operations.
- 2 pins for transmit and receive operations.
- 2 flow control pins.
- Interrupt triggers for low-power, internal CPU (for debug purposes).
- Support diagnostic tests.
- Support data input/ output operations for peripheral devices connected through a standard UART interface.

UART Interface Signals

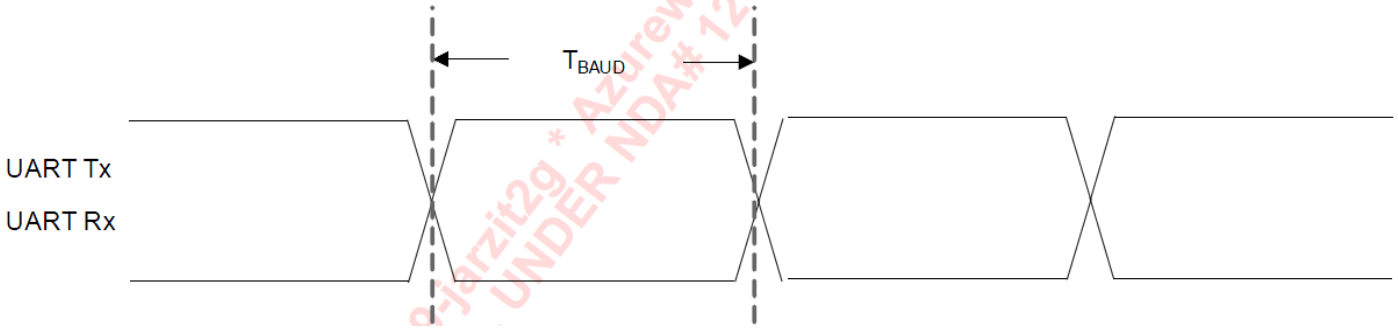
Pin Number	Signal Name	16550 Standard Name	Type	Description
42	UART_SOUT	SOUT	O	Serial data
43	UART_SIN	SIN	I	Serial data
44	UART_CTSn	CTSn	I	Clear To Send
41	UART_RTSn	RTSn	O	Request To Send

UART Baud Rates Supported

Baud Rate				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	-

The UART Tx and Rx pins are powered from the VDDIO voltage supply.

UART Timing Diagram



UART Timing Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
TBAUD	Baud rate	26MHz input clock	250	-	-	ns
TBAUD	Baud rate	38.4MHz input clock	250	-	-	ns

3.4.3 Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock frequency range/ accuracy CMOS input clock signal type ±250 ppm (initial, aging, temperature)	-	32.768	-	kHz
V_{IH}	Input levels, where VDDIO=1.8, 3.3V for VIH, VIL	0.7*VDDIO	-	VDDIO_0.4	V
V_{IL}		-0.4	-	0.3*VDDIO	V
PN	Phase noise requirement (@ 100KHz)	-	-125	-	dBc/Hz
J_C	Cycle jitter	-	1.5	-	ns (RMS)
SR	Slew rate limit (10-90%)	-	-	100	ns
DC	Duty cycle tolerance	20	-	80	%

The AW-CM358SM module crystal specifications

Parameter	Condition	Typical	Units
Fundamental Frequencies	-	26/ 38.4	MHz
Frequency tolerance	Over operating temperature	<±10	ppm
	Over process at 25℃	<±10	ppm
SMD and AT cut height	-	<1.2	Mm
Load Capacitance	-	5	pF
Maximum series resistance	-	45	Ω
Resonance mode	-	A1, Fundamental	-

3.5 Power Consumption*

3.5.1 WLAN

Band (GHz)	Item			VBAT=3.3V				
	Mode	BW (MHz)	RF Power (dBm)	Transmit			Receive	
				Max.	Avg.	DUTY %	Max.	Avg.
2.4	11b@1Mbps	20	18	TBD	TBD	TBD	TBD	TBD
	11g@54Mbps	20	16	TBD	TBD	TBD	TBD	TBD
	11n@MCS7	20	15	TBD	TBD	TBD	TBD	TBD
	11n@MCS7	40	14	TBD	TBD	TBD	TBD	TBD
5	11a@54Mbps	20	15	TBD	TBD	TBD	TBD	TBD
	11n@MCS7	20	15	TBD	TBD	TBD	TBD	TBD
	11n@MCS7	40	13	TBD	TBD	TBD	TBD	TBD
	11ac@MCS9 NSS1	80	12	TBD	TBD	TBD	TBD	TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

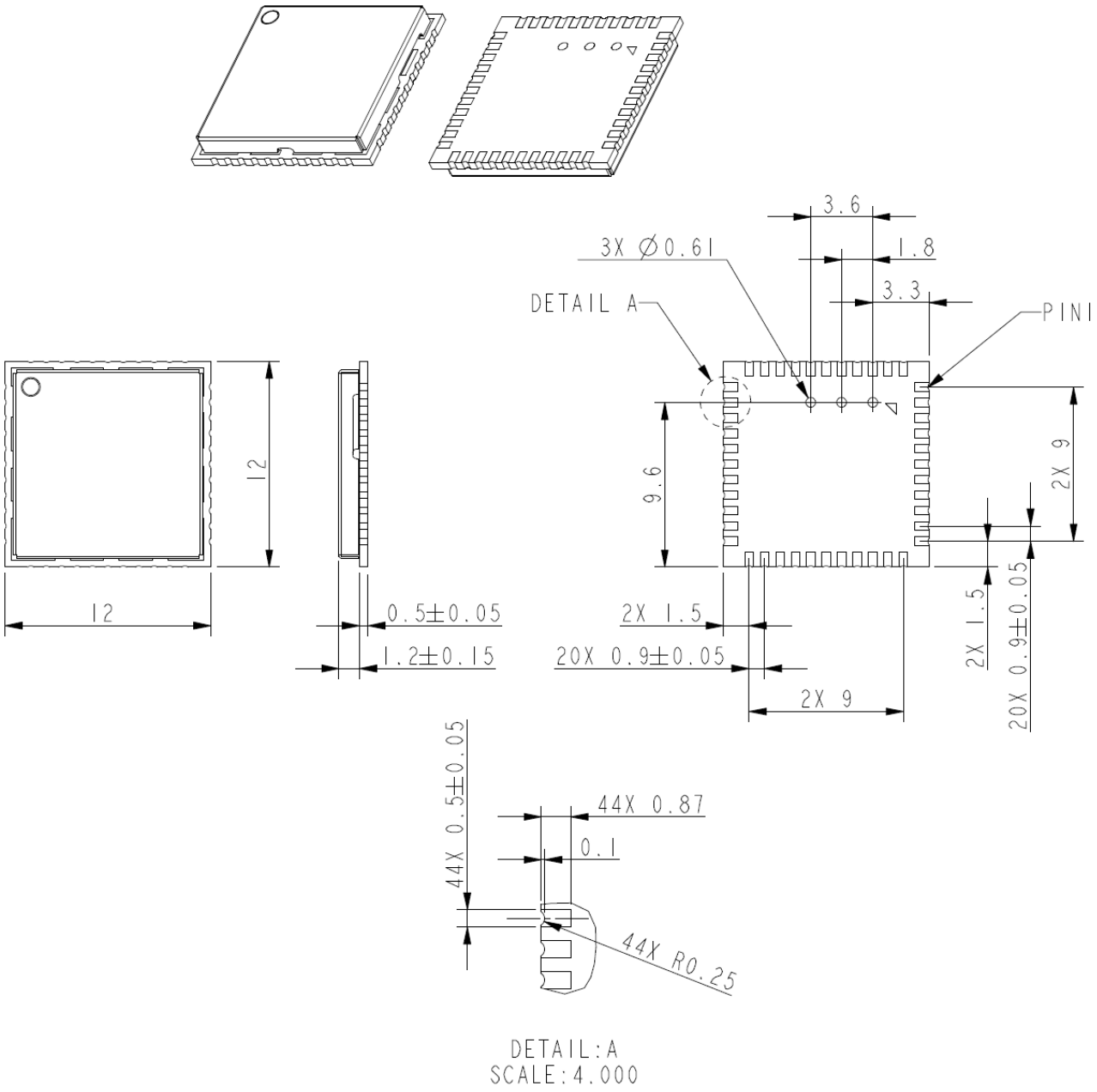
3.5.2 Bluetooth

No.	Mode	VBAT=3.3V			
		Transmit		Receive	
		Max.	Avg.	Max.	Avg.
1	Transmit (DH5)	TBD	TBD	TBD	TBD
2	Receive (3-DH5)	TBD	TBD	TBD	TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

4. Mechanical Information

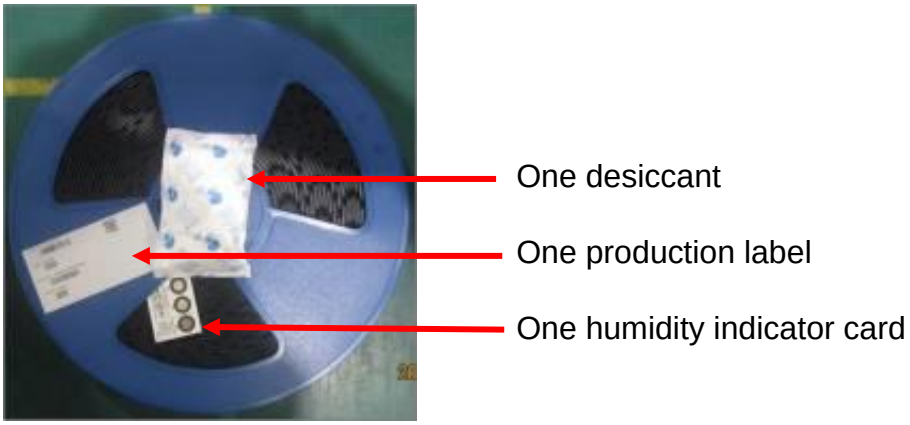
4.1 Mechanical Drawing



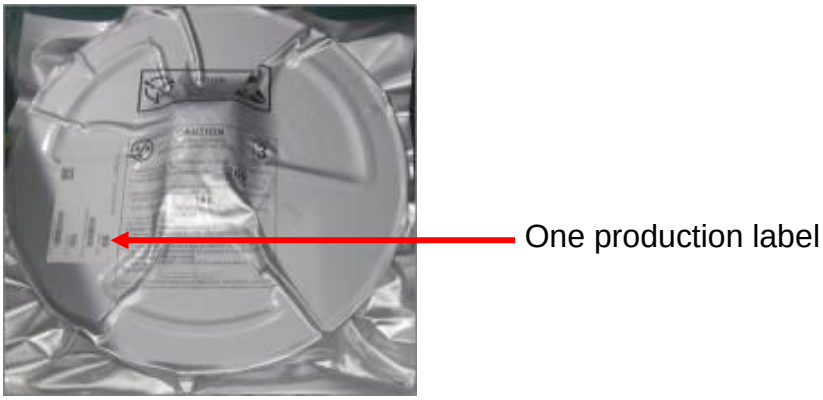
5. Packaging Information

1. One reel can pack 1,500pcs 12x12 stamp modules

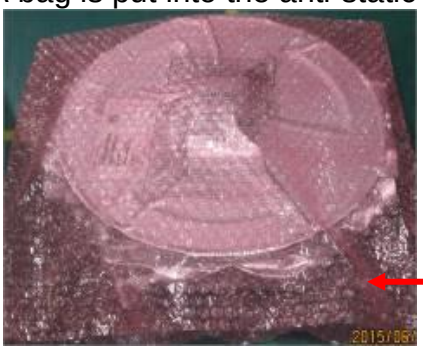
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag (卷軸放進防靜電鋁箔袋，再貼上一張生產標籤)



4. A bag is put into the anti-static pink bubble wrap



One anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box

One production label

6. **5 inner boxes** could be put into one carton

Production

7. Sealing the carton by AzureWave tape

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton