

AW-CM235NF

IEEE 802.11 a/b/g/n/ac Wireless LAN and Bluetooth Datasheet Mindential M.2 Combo Module

AZUreWave

Version 1.1



Revision History

Revision	Date	Description	Initials	Approved
Version 0.1	2014/12/31	Initial release	Alex Yu	Chihhao
version o.1	2014/12/31	Illitial release		Liao
Version 0.2	2015/2/10	Update pin map & pin definition & Specification	Stanley	Chihhao
version 0.2	2013/2/10	Opuate pin map & pin demittion & specification	Wang	Liao
Version 0.3	2015/4/15	Update Update Electrical Characteristics	Stanley	Chihhao
version 0.3	2013/4/13	Opuate Opuate Electrical Characteristics	Wang	Liao
		Modified Key Features	Steven	Chihhao
Version 0.4	2015/5/15	Modified Recommended Operating Conditions	Jian	Liao
		Update Specification & power consumption		
		Changed document format Updated 1.4.4 Operating Conditions	1	
Version 0.5	2017/10/12	Updated 4.1 Mechanical Drawing	Steven Jian	Chihhao
10131011 0.3	2017/10/12	Updated 3. Electrical Characteristics	Stevensian	Liao
		Updated 2.2 Pin Table		
Version 0.6	2017/11/27	Updated 1.4.4 Operating Conditions	Steven Jian	Chihhao
VC131011 0.0	2017/11/27	opaated 1.4.4 Operating conditions	Steven han	Liao
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				Liao Chihhao
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		Modified pin18 in 2.2 Pin Table		Chihhao
Version 0.9	2018/09/20	Updated Title	Steven Jian	Liao
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Version 1.0	2018/12/24	Support BT 5.0 Core Std	Steven Jian	Liao
Version 1.1	2019/07/11	Updated 1.4.2	Steven Jian	Chihhao
VC131011 1.1	2013/07/11	Updated 2.1	Steven Jian	Liao



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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced IEEE 802.11 ac/a/b/g/n 2x2 MIMO WLAN and Bluetooth M.2 combo module - AW-CM235NF. The module is targeted to mobile and embedded devices which need small footprint package, low power consumption, and multiple OS support. The module supports 2.4GHz and 5GHz bands IEEE 802.11ac MAC/baseband/radio and Bluetooth 5.0 + EDR. It also features an integrated Power Management Unit (PMU), Power Amplifiers (PAs), and a Low Noise Amplifier (LNA) to address the needs of mobile devices that require minimal power consumption and compact size. By using AW-CM235NF, the customers can easily enable the Wi-Fi and BT embedded applications with the benefits of high design flexibility, short development cycle, and quick time-to-market.

For the WLAN operation, the AW-CM235NF uses DSSS, OFDM, DBPSK, DQPSK, CCK and QAM baseband modulation technologies. In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in **20 MHz, 40 MHz, and 80 MHz channels** for data rates up to 867 Mbps. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM235NF. In addition to the support of **WPA/WPA2** (personal) and **WEP** encryption, the AW-CM235NF also supports the IEEE 802.11i security standard through **AES** and **TKIP** acceleration hardware for faster data encryption. For the video, voice and multimedia applications the AW-CM235NF support 802.11e Quality of Service (QoS).

For Bluetooth operation, the AW-CM235NF is **Bluetooth 5.0**. The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability. The AW-CM235NF supports **extended Synchronous Connections** (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets, and **Adaptive Frequency Hopping (AFH)** for reducing radio frequency interference. It incorporates all Bluetooth 5.0 features.



1.2 Features

- Integrates CYPRESS solutions of CYW4354 Wi-Fi /BT Single Chip
- Concurrent Bluetooth and WLAN operation
- ECI—enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- Multiple power saving modes for low power consumption
- Lead-free /Halogen Free Design
- 12 mm(L) x 16mm(W) x 1.5mm(H) 132 pin LGA package

1.2.1 WLAN

- IEEE 802.11ac Draft compliant
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance
- IEEE 802.11a/b/g/n/ac dual-band radio with virtual-simultaneous dual-band operation
- IEEE 802.11ac 2x2 MIMO supports for 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation) provides data rates up to 866.7 Mbps.
- Tx and Rx low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other colocated wireless technologies such as LTE, GPS, or WiMAX
- Supports IEEE 802.11d, e, h, i, r, k, w
- WLAN host interface options
 - SDIO
- Security-WEP, WPA/WPA2 (personal), AES (HW), TKIP (HW), CKIP (SW).
- WMM/WMM-PS/WMM-SA
- Proprietary protocol –CCXv2/CCXv3/CCXv4/CCXv5
- Integrated CPU with on-chip memory for a complete WLAN subsystem minimizing the need to wake up the applications processor



1.2.2 Bluetooth

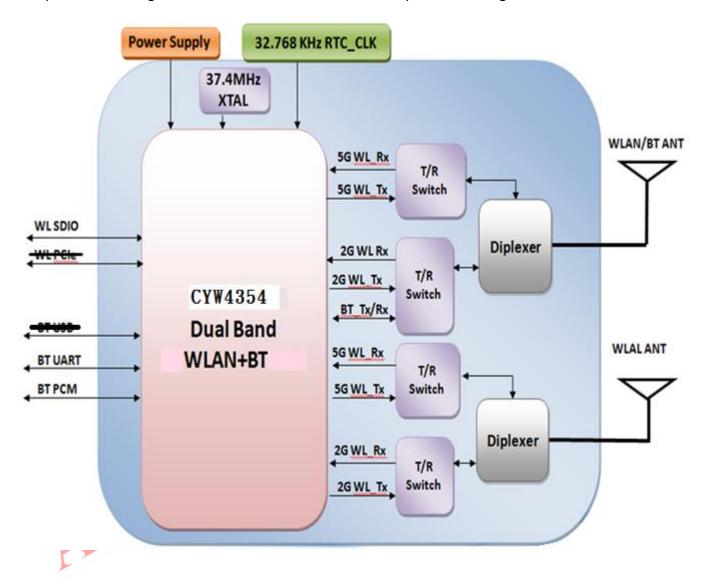
- Bluetooth Class 1 or Class 2 transmitter operation
- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 5.0 + (Enhanced Data Rate) EDR features:
 - Adaptive Frequency Hopping (AFH)
 - Quality of Service (QoS)
 - Extended Synchronous Connections (eSCO) Voice Connections
 - Fast Connect (interlaced page and inquiry scans)
 - Secure Simple Pairing (SSP)
 - Sniff Subrating (SSR)
 - Encryption Pause Resume (EPR)
 - Extended Inquiry Response (EIR)
 - Link Supervision T imeout (LST)
- Multipoint operation with up to seven active slaves
 - Maximum of seven simultaneous active ACL links
 - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Full support for power savings modes
 - Bluetooth clock request
 - Bluetooth standard sniff
 - Deep-sleep modes and software regulator shutdown
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I2S and PCM interface)
- Multiple simultaneous A2DP audio stream





1.3 Block Diagram

A simplified block diagram of the AW-CM235NF module is depicted in the figure below.





1.4 Specifications Table

1.4.1 General

Features	Description			
Product Description	IEEE 802.11 a/b/g/n/ac Wireless LAN and Bluetooth M.2 Combo Module			
Major Chipset	CYPRESS CYW4354			
Host Interface	WLAN: SDIO V 3.0 Bluetooth: UART			
Dimension	16mm(L) 12xmm(W) x 1.5mm(H)			
Package	M.2 1216 Solder down			
Antenna	I-PEX MHF4 Connector Receptacle (20449) Ant 1: WiFi/BT Main Ant 2: WIFI AUX			
Weight	0.6g			
1.4.2 WLAN	COIL			

1.4.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant
WLAN VID/PID	n/a
WLAN SVID/SPID	n/a
Frequency Rage	WLAN: 2.4 GHz / 5GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9)
Number of Channels	802.11b: USA, Canada and Taiwan - 1 ~ 11 Most European Countries - 1 ~ 13 Japan - 1 ~ 13 802.11g: USA and Canada - 1 ~ 11 Most European Countries - 1 ~ 13 802.11n:



USA and	Canada -	1 ~ 11
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Most European Countries − 1 ~ 13

802.11a:

USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

2.4G

2.10				
	Min	Тур	Max	Unit
11b (11Mbps) @EVM<35%	14	16	18	dBm
11g (54Mbps) @EVM≦-25 dB	12	14	16	dBm
11n (HT20 MCS7) @EVM≦-27 dB	11	13	15	dBm
11n (HT40 MCS7) @EVM≦-27 dB	9	11	13	dBm

Output Power (Board Level Limit)*

5G

	Min	Тур	Max	Unit
11a (54Mbps) @EVM≦-25 dB	11	13	15	dBm
11n (HT20 MCS7) @EVM≦-27 dB	10	12	14	dBm
11n (HT40 MCS7) @EVM≦-27 dB	8	10	12	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	6	8	10	dBm

2.4G

	Min	Тур	Max	Unit
11b (11Mbps)		-88	-78	dBm
11g (54Mbps)		-74	-65	dBm
11n (HT20 MCS7)		-71	-64	dBm
11n (HT40 MCS7)		-68	-61	dBm

Receiver Sensitivity

5G

	Min	Тур	Max	Unit
11a (54Mbps)		-73	-65	dBm
11n (HT20 MCS7)		-70	-64	dBm
11n (HT40 MCS7)		-67	-61	dBm
11ac (VHT80 MCS9)		-59	-51	dBm

802.11b: 1, 2, 5.5, 11Mbps

802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps

Data Rate 802.11n: MCS0~7 HT20/HT40

802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps

802.11ac: MCS0~8 VHT20

9



	802.11ac: MCS0~9 VHT40/VHT80
Security	 WPA™- and WPA2™- (Personal) support for powerful encryption and authentication AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility Secure Easy Setup™ for simple Wi-Fi® setup and WPA2/WPA security configuration Wi-Fi Protected Setup (WPS) WEP WMM / WMM-SA CKIP(Software)

^{*} If you have any certification questions about output power please contact FAE directly.

1.4.3 Bluetooth

Features	Description	Description			
Bluetooth Standard	Bluetooth 2.1+E	Bluetooth 2.1+Enhanced Data Rate (EDR) / BT5.0			
Bluetooth VID/PID	n/a	n/a			
Frequency Rage	2350~2483.5MH	2350~2483.5MHz			
Modulation	GFSK (1Mbps),	GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)			
Output Power	Class 2	Class 2			
		Min	Тур	Max	Unit
Receiver Sensitivity	DH5		-92	-82	dBm
	2DH5		-94	-84	dBm
	3DH5		-88	-78	dBm

1.4.4 Operating Conditions

Features	Description	
Operating Conditions		
Voltage	power supply for host:3.3V+-5%	
Operating Temperature	-30~85°C (Functionality is guaranteed. Optimal RF operating is 0~55°C)	
Operating Humidity	<85%	
Storage Temperature	-40~85°C	
Storage Humidity	<60 %	



ESD Protection				
Human Body Model	>1kV			
Changed Device Model	>300V			

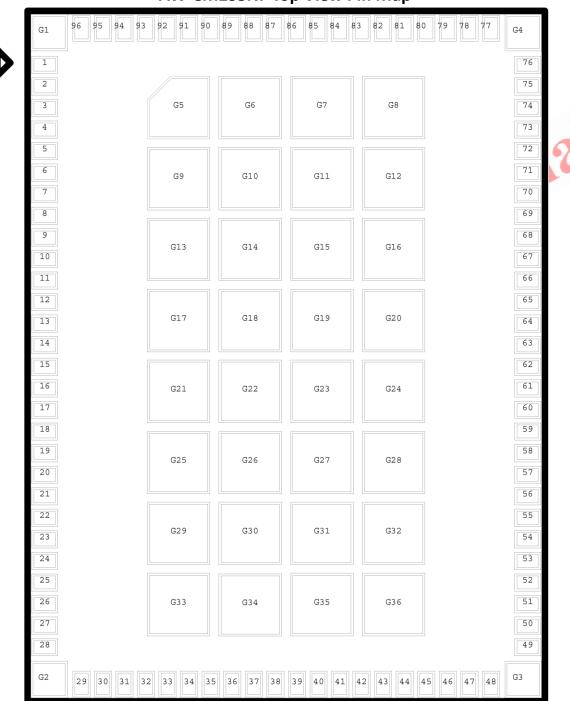
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2. Pin Definition

2.1 Pin Map

AW-CM235NF Top View Pin Map





2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Туре
1	NC	No Connect		
2	JTAG_SEL	JTAG test on/off(pull high to enable JTAG)	VIO	I
3	NC	No Connect		
4	3.3V	3.3V Power Supply	3.3V	l
5	3.3V	3.3V Power supply input	3.3V	I
6	GND	System Ground Pin		
7	JTAG_TDO_GPIO_5	GPIO_5 (input/output)	VIO	0
8	GPIO_8	Strapping option(please pull down with 10k resistor)	VIO	l
9	GPIO_9	Strapping option(please pull down with 10k resistor)	VIO	l
10	JTAG_TDI_GPIO_4	0: SPROM is absent (default). *Please reserve pull-down resistor	VIO	I
11	JTAG_TMS_COEX2_GPIO_3	GPIO_3 (input/output)	VIO	I/O
12	JTAG_TCK_COEX1_GPIO_2	GPIO_2 (input/output)	VIO	I/O
13	JTAG_TRST_N_COEX0_GPIO_6	GPIO_6 (input/output)	VIO	I/O
14	NC	No Connect		
15	NC	No Connect		
16	NC	No Connect		
17	GND	System Ground Pin		
18	NC	No Connect		
19	NC	No Connect		
20	GND	System Ground Pin		
21	NC	No Connect		
22	NC	No Connect		
23	GND	System Ground Pin		
24	BT_DEV_WAKE	Bluetooth DEV_WAKE.	VIO	I
25	NC	No Connect		
26	GND	System Ground Pin		
27	SLPCLK	External sleep clock input (32.768 kHz).	0.2~3.3Vp-p	I
28	WL_RFDISABLE_L_GPIO1	WL_DEV_WAKE/GPIO1	VIO	I



30 PCIE_CLKREQN Reserved 31 PCIE_PERSTN Reserved 32 GND System Ground Pin 33 PCIE_RCLK_N Reserved 34 PCIE_RCLK_P Reserved 35 GND System Ground Pin 36 PCIE_TX_N Reserved 37 PCIE_TX_P Reserved 38 GND System Ground Pin 39 PCIE_RX_N Reserved 40 PCIE_RX_P Reserved 41 GND System Ground Pin 42 NC No Connect 43 NC No Connect 44 VIO_SD 1.8V/3.3V Digital I/O SDIO Power Supply VIO 45 WL_REG_ON Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. 46 SDIO_WAKE_L_GPIO_0 W_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT1 <th>O O I I</th>	O O I I
32 GND System Ground Pin 33 PCIE_RCLK_N Reserved 34 PCIE_RCLK_P Reserved 35 GND System Ground Pin 36 PCIE_TX_N Reserved 37 PCIE_TX_P Reserved 38 GND System Ground Pin 39 PCIE_RX_N Reserved 40 PCIE_RX_P Reserved 41 GND System Ground Pin 42 NC No Connect 43 NC No Connect 44 VIO_SD 1.8V/3.3V Digital I/O SDIO Power Supply VIO 45 WL_REG_ON Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. 46 SDIO_WAKE_L_GPIO_0 WL_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[1] VIO	
33	
34 PCIE_RCLK_P Reserved 35 GND System Ground Pin 36 PCIE_TX_N Reserved 37 PCIE_TX_P Reserved 38 GND System Ground Pin 39 PCIE_RX_N Reserved 40 PCIE_RX_P Reserved 41 GND System Ground Pin 42 NC No Connect 43 NC No Connect 44 VIO_SD 1.8V/3.3V Digital I/O SDIO Power Supply VIO 45 WL_REG_ON Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. VIO 46 SDIO_WAKE_L_GPIO_0 WL_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[2] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	
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36 PCIE_TX_N Reserved 37 PCIE_TX_P Reserved 38 GND System Ground Pin 39 PCIE_RX_N Reserved 40 PCIE_RX_P Reserved 41 GND System Ground Pin 42 NC No Connect 43 NC No Connect 44 VIO_SD 1.8V/3.3V Digital I/O SDIO Power Supply VIO Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. VIO 46 SDIO_WAKE_L_GPIO_0 WL_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[2] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	
37 PCIE_TX_P Reserved 38 GND System Ground Pin 39 PCIE_RX_N Reserved 40 PCIE_RX_P Reserved 41 GND System Ground Pin 42 NC No Connect 43 NC No Connect 44 VIO_SD 1.8V/3.3V Digital I/O SDIO Power Supply VIO 45 WL_REG_ON Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. VIO 46 SDIO_WAKE_L_GPIO_0 WL_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[2] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	
38 GND System Ground Pin 39 PCIE_RX_N Reserved 40 PCIE_RX_P Reserved 41 GND System Ground Pin 42 NC No Connect 43 NC No Connect 44 VIO_SD 1.8V/3.3V Digital I/O SDIO Power Supply VIO 45 WL_REG_ON Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. VIO 46 SDIO_WAKE_L_GPIO_0 WL_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[2] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	O I I
39 PCIE_RX_N Reserved 40 PCIE_RX_P Reserved 41 GND System Ground Pin 42 NC No Connect 43 NC No Connect 44 VIO_SD 1.8V/3.3V Digital I/O SDIO Power Supply VIO 45 WL_REG_ON Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. VIO 46 SDIO_WAKE_L_GPIO_0 WL_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[2] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	l I
40 PCIE_RX_P Reserved 41 GND System Ground Pin 42 NC No Connect 43 NC No Connect 44 VIO_SD 1.8V/3.3V Digital I/O SDIO Power Supply VIO 45 WL_REG_ON Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. 46 SDIO_WAKE_L_GPIO_0 WL_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[1] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	l I
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Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. 46 SDIO_WAKE_L_GPIO_0 WL_HOST_WAKE VIO 47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[2] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	
WL_REG_ON internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. WL_HOST_WAKE VIO SDIO DAT3 SDIO Data line Bit[3] VIO SDIO DAT2 SDIO Data line Bit[2] VIO SDIO DAT1 SDIO Data line Bit[1] VIO	I
47 SDIO DAT3 SDIO Data line Bit[3] VIO 48 SDIO DAT2 SDIO Data line Bit[2] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	I
48 SDIO DAT2 SDIO Data line Bit[2] VIO 49 SDIO DAT1 SDIO Data line Bit[1] VIO	0
49 SDIO DAT1 SDIO Data line Bit[1] VIO	I/O
49 SDIO DATT STORY IN THE STORY	I/O
50 SDIO DATO SDIO Data line Bit[0] VIO	I/O
ODIO DATO	I/O
51 SDIO CMD SDIO Command/response (input/output) VIO	I/O
52 SDIO CLK SDIO Clock input VIO	I
53 BT_HOST_WAKE Bluetooth HOST_WAKE. VIO	0
54 UART CTSn UART_CTSn (input) VIO	I
55 UART SOUT UART_TXD (output) VIO	0
56 UART SIN UART_RXD (input) VIO	
57 UART RTSn UART_RTSn (output) VIO	I



	71241011410 10011110109	1100, 1110.		
58	PCM_SYNC	PCM sync; can be master (output) or slave (input).	VIO	I/O
59	PCM_IN	PCM data input	VIO	I
60	PCM_OUT	PCM data output	VIO	0
61	PCM_CLK	PCM bus clock; can be master (output) or slave (input)	VIO	I/O
62	GND	System Ground Pin		
63	BT_REG_ON	Used by PMU to power up or power down the internal module regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset.	VIO	I
64	WL_LED_GPIO_7	It can be used as WL_LED.	VIO	0
65	BT_I2S_DO_BT_LED_L	It can be used as BT_LED.	VIO	0
66	NC	No Connect		
67	NC	No Connect		
68	GND	System Ground Pin		
69	USB_D-	No Connect		
70	USB_D+	No Connect		
71	GND	System Ground Pin		
72	3.3V	3.3V Power Supply	3.3V	I
73	VIO	Digital I/O Power Supply	VIO	I
74	GND	System Ground Pin		
75	GND	System Ground Pin		
76	GND	System Ground Pin		
77	GND	System Ground Pin		
78	GND	System Ground Pin		
79	GND	System Ground Pin		
80	GND	System Ground Pin		
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85	GND	System Ground Pin		



86	GND	System Ground Pin	
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92	GND	System Ground Pin	
93	GND	System Ground Pin	
94	GND	System Ground Pin	
95	GND	System Ground Pin	
96	GND	System Ground Pin	
G1	GND	System Ground Pin	
G2	GND	System Ground Pin	
G3	GND	System Ground Pin	
G4	GND	System Ground Pin	
G5	GND	System Ground Pin	
G6	GND	System Ground Pin	
G7	GND	System Ground Pin	
G8	GND	System Ground Pin	
G9	GND	System Ground Pin	
G10	GND	System Ground Pin	
G11	GND	System Ground Pin	
G12	GND	System Ground Pin	
G13	GND	System Ground Pin	
G14	GND	System Ground Pin	
G15	GND	System Ground Pin	
G16	GND	System Ground Pin	
G17	GND	System Ground Pin	
G18	GND	System Ground Pin	
G19	GND	System Ground Pin	



		Puriodition P / Supplied Stocks				
G20	GND	System Ground Pin				
G21	GND	System Ground Pin				
G22	GND	System Ground Pin				
G23	GND	System Ground Pin				
G24	GND	System Ground Pin				
G25	GND	System Ground Pin				
G26	GND	System Ground Pin				
G27	GND	System Ground Pin				
G28	GND	System Ground Pin				
G29	GND	System Ground Pin				
G30	GND	System Ground Pin				
G31	GND	System Ground Pin				
G32	GND	System Ground Pin				
G33	GND	System Ground Pin				
G34	GND	System Ground Pin				
G35	GND	System Ground Pin				
G36	GND	System Ground Pin				
G36 GND System Ground Pin						



3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
3.3V	Power supply for Internal Regulators	-0.3	5.5	V
VIO	DC supply voltage for digital I/O	-0.5	3.9	V

3.2 Recommended Operating Conditions

Symbol	Pai	rameter	Туре	Min	Тур	Max	Units
3.3V	Power supply for Interi	nal Regulators	Input	3.13	-	3.46	V
3.3 Digital IO P	in DC Character	ristics	C	9	NS		
	<u></u>						

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Condition	Min	Тур	Max	Unit
SDIO Interfa	ce I/O pins		U			_
V _{IH}	Input high voltage (VDDIO)	VDDIO=1.8V	1.27	-	-	V
V _{IL}	Input low voltage (V _{DDIO})	VDDIO=1.8V	-	-	0.58	V
Vон	Output High Voltage @ 2mA	VDDIO=1.8V	1.4	-	-	V
Vol	Output Low Voltage @ 2mA	VDDIO=1.8V	-	-	0.45	V
V _{IH}	Input high voltage (V _{DDIO})	VDDIO=3.3V	0.625xVDDIO	-	-	V
VIL	Input low voltage (V _{DDIO})	VDDIO=3.3V	-	-	0.25xVDDIO	V
VoH	Output High Voltage @ 2mA	VDDIO=3.3V	0.75xVDDIO	-	-	V
VoL	Output Low Voltage @ 2mA	VDDIO=3.3V	-	-	0.125xVDDIO	V
Other Digita	Il I/O pins					
V _{IH}	Input high voltage (VDDIO)	VDDIO=1.8V	0.65xVDDIO	-	-	V
VIL	Input low voltage (V _{DDIO})	VDDIO=1.8V	-	-	0.35xVDDIO	V
V _{OH}	Output High Voltage @ 2mA	VDDIO=1.8V	VDDIO-0.45	-	-	V
Vol	Output Low Voltage @ 2mA	VDDIO=1.8V	-	-	0.45	V
ViH	Input high voltage (V _{DDIO})	VDDIO=3.3V	2.0	-	-	V
VIL	Input low voltage (V _{DDIO})	VDDIO=3.3V	-	-	0.8	V
Vон	Output High Voltage @ 2mA	VDDIO=3.3V	VDDIO-0.4	-	-	V
V_{OL}	Output Low Voltage @ 2mA	VDDIO=3.3V	-	-	0.4	V



3.4 Power up Timing Sequence

3.4.1 Sequencing of Reset and Regulator Control Signals

The AW-CM235NF has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Note:

- For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.
- VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

3.4.2 Description of Control Signals

The AW-CM235NF has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption.

PIN No.	Name	Description	Туре
45	WL_REG_ON	Used by PMU to power up or power down the internal AW-CM235NF regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 k Ω pull-down resistor that is enabled by default. It can be disabled through programming.	I
63	BT_REG_ON	Used by PMU to power up or power down the internal AW-CM235NF regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 k Ω pull-down resistor that is enabled by default. It can be disabled through programming.	I

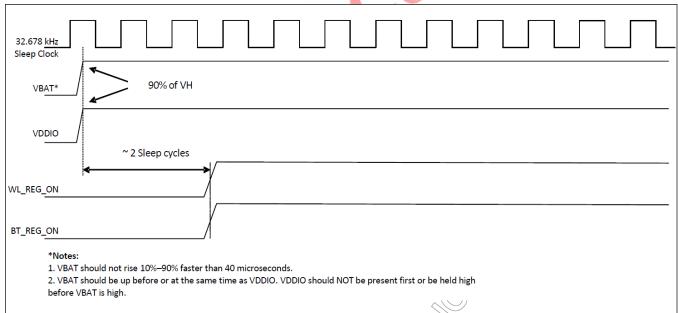


Power-Up/Power-Down/Reset Control Signals

	, ,
Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also ORgated with the BT_REG_ON input to control the internal AW-CM235NF regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 k Ω pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal AW-CM235NF regulators. If both BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset. This pin has an internal 200 k Ω pull-down resistor that is enabled by default. It can be disabled through programming.

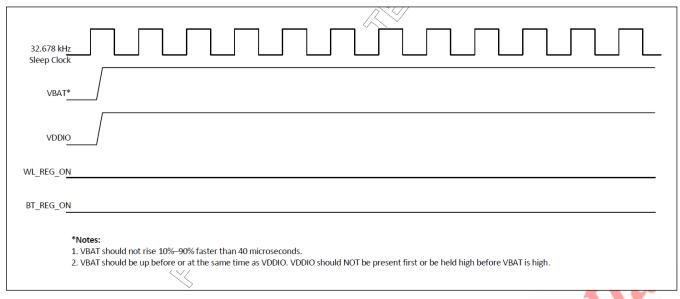
3.4.3 Control Signal Timing Diagrams

WLAN = ON, Bluetooth = ON

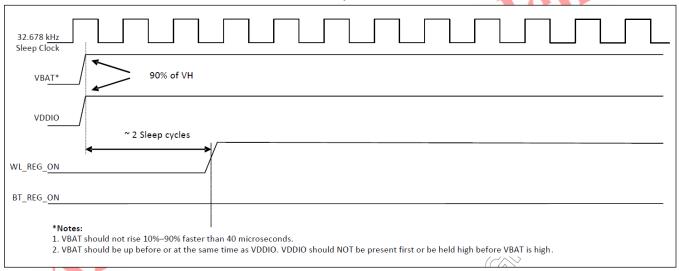


WLAN = OFF, Bluetooth = OFF



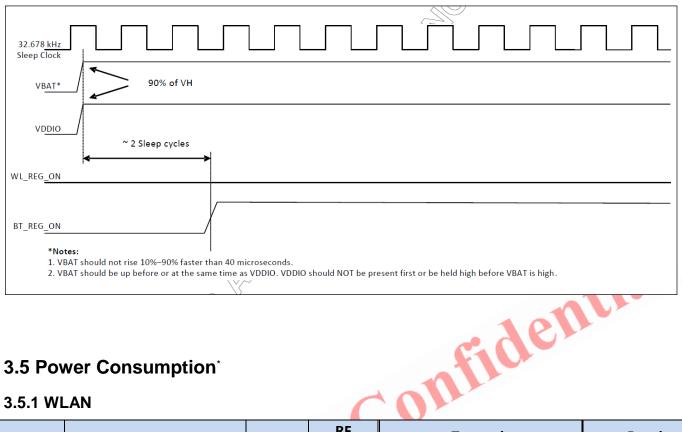


WLAN = ON, Bluetooth = OFF



WLAN = OFF, Bluetooth = ON





3.5 Power Consumption*

3.5.1 WLAN

Band	Mode	BW	RF Power	Transmit			Receive	
(GHz)	Wiode	(MHz)	(dBm)	Max.	Avg.	Duty. (%)	Max.	Avg.
	11b@1Mbps	20	16	316.4mA	291.9mA	98.9%	69.4 mA	68.1 mA
	11g@54Mbps	20	14	333.1mA	212.1mA	64.8%	68.0 mA	67.6 mA
2.4	11n@MCS7	20	13	309.7mA	210.6mA	63.3%	73.4 mA	67.5mA
	11n@MCS7	40	11	306.9mA	200 mA	57.9%	81.8mA	81.5mA
	11n@MCS15	40	11	530.8mA	308 mA	50%	114.4mA	114.2mA
	11a@54Mbps	20	13	297.1mA	212.2mA	87.6%	83.0mA	82.8mA
	11n@MCS7	20	12	284.5mA	227.5mA	78.2%	84.6mA	82.7mA
5	11n@MCS7	40	10	290.8mA	200.2mA	51.2%	98.6mA	98.4mA
	11ac@MCS9 NSS1	80	8	320.6mA	237.8mA	47.8%	125.0mA	124.9mA
	11ac@MCS9 NSS2	80	8	564.3mA	347.1mA	47.1%	184.9mA	184.7mA

3.5.2 Bluetooth

No.	Mode	Packet Type	VBAT_IN=3.3 V			
NO.	Wiode	racket Type	Max.	Avg.		
1	Sleep	n/a		5.29 uA		
2	Page scan	n/a	10.9mA	158.2uA		



3	Transmit *(4)	DH5	23.5 mA	22.6 mA		
4	Receive	3-DH5	15.6 mA	15.3 mA		

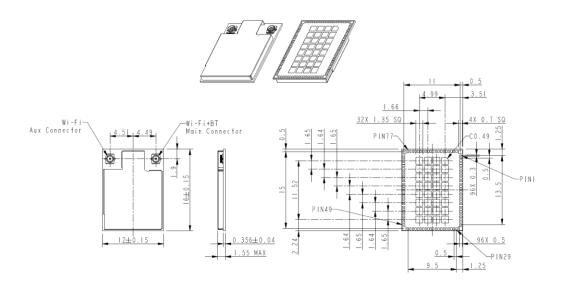
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^{*} The power consumption is based on Azurewave test environment, these data for reference only.



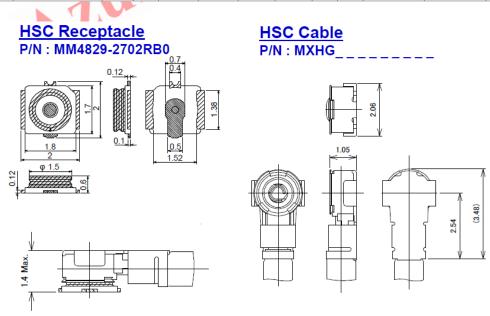
4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCES UNLESS OTHERWISE SPECIFIED : ± 0.15 mm

								SCA	\LE	DESCRIPTION		MODEL NO:	APPROVAL	
			AzureWave				2/	1	PCB ASSEMBLY		2235NF			
						0 ′	ΤY	DWG NO:			DESIGNED			
			DIM.	0~80	80~180	180~315	315~800		PCS	MATERIAL	FINISH	2235NF-COD-001		STEVE CHANG
								UNIT REV			PART NO:	DATE		
ITEM	DESCRIPTION	DATE	TOL.	0.1	0.15	0.20	0.25	MM	Α					2017/10/11



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5. Packaging Information

5.1 1 UNIT DESICCANT **HUMIDITY INDICATOR CARD** AFFIX PACKING LABEL 5.2



AFFIX PACKING LABEL

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PINK BUBBLE WRAP



5.4



AFFIX PACKING LABEL

5.51 Carton= 5 Boxes





Confidential

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