AzureWave Technologies, Inc.

AW-XM646x Series

IEEE 802.11 a/b/g/n/ac/ax Wireless LAN 1T1R and BLE/802.15.4 Solution Family 12 x 12 LGA Module

Datasheet

Rev. A

DF

For Standard

Features

WLAN

- 1x1 dual-band 2.4 GHz/5 GHz Wi-Fi 6 radio
- Integrated Wi-Fi PA, LNA, and T/R switch, up to +23 dBm TX power
- 20 MHz channel operation
- Wi-Fi 6 Target Wake Time (TWT) support
- Wi-Fi 6 Extended Range (ER) and Dual Carrier Modulation (DCM)
- Low-power Wi-Fi idle, standby, and sleep modes
- WPA2/WPA3 security
- Support for Matter over Wi-Fi

Bluetooth

- Bluetooth Low Energy 5.4
- Bluetooth LE 1 Mbps and 2 Mbps high-speed uncoded modes, and Long Range operation (125 kbps and 500 kbps coded data rates)
- IEEE 802.15.4-2015 compliant MAC
- Support for Matter over Thread

802.15.4

- IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
- Shared transmitter and antenna pin with Bluetooth
- Simultaneous receive with Wi-Fi and Bluetooth
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers

Revision History

Document NO: R2-2646-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2024/12/12	DCN033008	Initial version	Vigil Tsai	N.C. Chen

AzureWave Technologies, Inc.

Table of Contents

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n/ac/ax 1x1 dual band WLAN, BLE/802.15.4, module – **AW-XM646.** With full-feature Wi-Fi subsystem integrated into a module, **AW-XM646** provides the best and most convenient SMT process. The module is targeted to smart entertainment, gateways, hubs, bridges, smart home, industrial, point of sale (POS) terminal, smart appliances which need convenient SMT process.

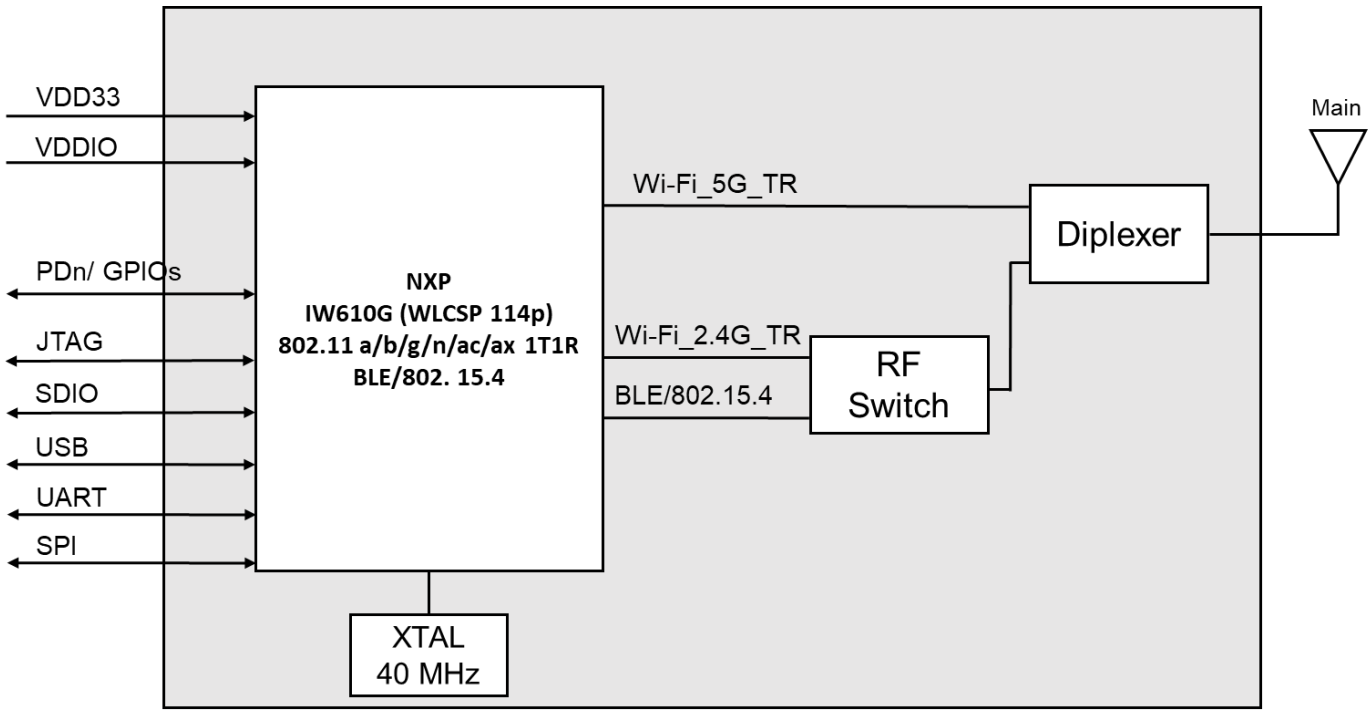
By using **AW-XM646**, the customers can easily integrate the Wi-Fi, BLE, by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11 a/b/g/n/ac/ax standard, the **AW-XM646** uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using **AW-XM646**.

The **AW-XM646** supports standard interface **USB 2.0 / SDIO3.0 for WLAN**, **USB 2.0 / UART for BLE, SPI for 802.15.4**. **AW-XM646** is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the **AW-XM646** is the best solution for the consumer electronics and smart applications.

1.2 Block Diagram

A simplified block diagram of the AW-XM646 module is depicted in the figure below.



AW-XM646 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6 with BLE/802.15.4 Combo Solution
Major Chipset	NXP IW610F/G WLCSP (114pins)
Host Interface	Wi-Fi + BLE + 802.15.4 ● SDIO + UART + SPI (Optional) ● USB + USB + SPI (Optional)
Dimension	12 mm X 12 mm x 2 mm(Max)
Form Factor	LGA module, 48 pins
Antenna	ANT1(Main)：Wi-Fi / BLE / 802.15.4 → TX/RX
Weight	TBD

AW-XM646x variants

Product name	Features	Interface
AW-XM646F-USB	1x1 Dual-band (2.4 / 5 GHz) Wi-Fi 6 + BLE	USB+USB
AW-XM646F-SUR	1x1 Dual-band (2.4 / 5 GHz) Wi-Fi 6 + BLE	SDIO+UART
AW-XM646G-USB	1x1 Dual-band (2.4 / 5 GHz) Wi-Fi 6 + BLE/802.15.4	USB+USB+SPI
AW-XM646G-SUR	1x1 Dual-band (2.4 / 5 GHz) Wi-Fi 6 + BLE/802.15.4	SDIO+UART+SPI

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6
WLAN VID/PID	NA
WLAN SVID/SPID	NA
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-AQM, OFDMA

<table>
<tr><td>Number of Channels</td><td>2.4GHz:
■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11
■ China, Australia, Most European Countries - 1 ~ 13
■ Japan, 1 ~ 13

5GHz:
■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140
■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power
(Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)
@EVM<35%</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦-27 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-28 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS9)
@EVM≦-35 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)
@EVM≦-27 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-28 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)
@EVM≦-31 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS9)
@EVM≦-35 dB</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS9)</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS9)</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n : Maximum data rates up to 72 Mbps
802.11ac: Maximum data rates up to 86 Mbps
802.11ax: Maximum data rates up to 144 Mbps</td></tr>
<tr><td>Security</td><td>■ WiFi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP
■ BT: AES</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth LE 5.4 certified</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>Low Energy</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>Low Energy</td><td></td><td>TBD</td><td></td><td>dBm</td></tr>
</table>
</td></tr>
</table>

1.3.4 Thread

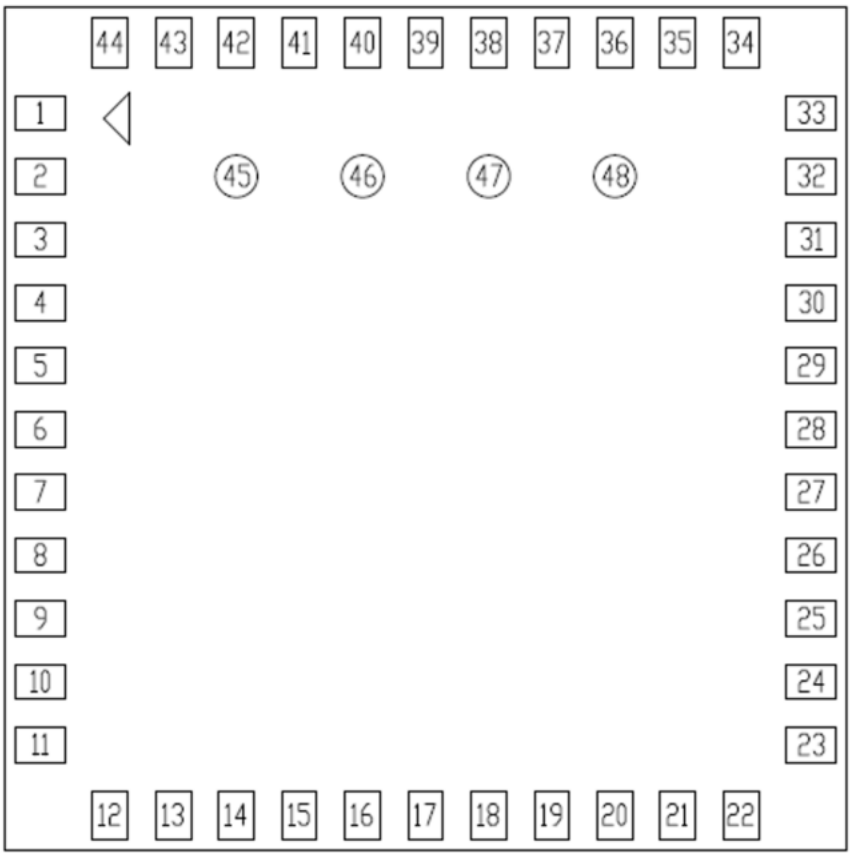
Features	Description
Thread Standard	IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
Frequency Rage	2400MHz~2483.5MHz
Modulation	O-QPSK
Output Power	<table><tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr><tr><td>Thread</td><td></td><td>TBD</td><td></td><td>dBm</td></tr></table>

1.3.5 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	0 °C to +70 °C
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 °C to +85 °C
Storage Humidity	Less than 60% R.H.
Thermal Shield Performance Target	Full performance at shield temperatures up to TBD℃
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

2. Pin Definition

2.1 Pin Map



AW-XM646 Pin Map (top view)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND1	Ground	---	---
2	RF_ANT	RF pin out	---	I/O
3	GND	Ground	---	---
4	SPI_TXD	SPI receive output signal. GPIO[6]	VDDIO	I/O
5	SPI_RXD	SPI receive input signal. GPIO[7]. PCM mode PCM sync signal	VDDIO	I/O
6	HOST_WAKE_ BT	GPIO Mode : GPIO[17]. Host wake BLE/802.15.4 device	VDDIO	I/O
7	BT_WAKE_Host	JTAG_TDO mode test data output signal. GPIO[5]. BLE/802.15.4 device wake Host	VDDIO	O
8	SPI_FRM	SPI_FRM - SPI frame signal. GPIO[8]	VDDIO	I/O
9	VBAT	3.3V power voltage source input	3.3V	P
10	JTAG_TMS	JTAG test mode select input signal. GPIO[3]	VDDIO	I/O
11	SPI_CLK	SPI_CLK - SPI clock signal. GPIO[9]	VDDIO	I/O
12	PDn	Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode (Need external pull high 51k resistor to VDDIO)	1.8V/3.3V	I
13	WL_WAKE_Host	JTAG_TDI Mode test data input signal. GPIO[4]. Wake up mode WIFI wake host output signal	VDDIO	I/O
14	SDIO_DATA2	SDIO Data line Bit[2]	VDDIO	I/O
15	SDIO_DATA3	SDIO Data line Bit[3]	VDDIO	I/O
16	SDIO_CMD	SDIO Command	VDDIO	I/O
17	SDIO_CLK	SDIO Clock input	VDDIO	I
18	SDIO_DATA0	SDIO Data line Bit[0]	VDDIO	I/O
19	SDIO_DATA1	SDIO Data line Bit[1]	VDDIO	I/O
20	GND	Ground	---	---
21	DCDC_1V8_OUT	Internal DC-DC output (Need external 1uH power inductor and 22μF capacitance)	1.8V	P
22	VDDIO	1.8V/3.3V Digital I/O Power Supply	1.8V/3.3V	P
23	DCDC_1V8_IN	1.8V power voltage source input	1.8V	P
24	NC	Floating Pin, No connect to anything.	---	Floating
25	NC	Floating Pin, No connect to anything.	---	Floating
26	NC	Floating Pin, No connect to anything.	---	Floating
27	NC	Floating Pin, No connect to anything.	---	Floating
28	PCM_SYNC	PCM sync signal / GPIO[7]	VDDIO	I/O
29	NC	Floating Pin, No connect to anything.	---	Floating
30	NC	Floating Pin, No connect to anything.	---	Floating
31	GND	Ground	---	---
32	NC	Floating Pin, No connect to anything.	---	Floating

33	GND	Ground	---	---
34	RST_NB	Host-to-BT reset /IND_RST_BT – Independent. GPIO[11]	---	I
35	JTAG_TCK	JTAG test clock input signal. GPIO[2]	VDDIO	I
36	GND	Ground	---	---
37	USB_DM	USB Serial Differential Data Minus	3.3V	I/O
38	USB_DP	USB Serial Differential Data Plus	3.3V	I/O
39	GND	Ground	---	---
40	HOST_WAKE_WL	Host wake WLAN radio input signal. GPIO[16].	VDDIO	I
41	UART_RTS_N	UART_RTSn (active low)	VDDIO	O
42	UART_TXD	UART_SOUT	VDDIO	O
43	UART_RXD	UART_SIN(active high)	VDDIO	I
44	UART_CTS	UART_CTS(active high)	VDDIO	I
45	GND	Ground	---	---
46	RST_WL	Independent software reset for Wi-Fi. GPIO[10]	VDDIO	I/O
47	NC	Floating Pin, No connect to anything.	VDDIO	I/O
48	SPI_INT	SPI interrupt signal / BOOT3	VDDIO	I/O

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	-	3.3	3.96	V
VDDIO	I/O power supply	-	3.3	3.96	V
		-	1.8	2.16	

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	3.14	3.3	3.46	V
VDDIO	1.8V/3.3V digital I/O power supply	3.14	3.3	3.46	V
		1.71	1.8	1.98	

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.4 Host Interface

3.4.1 SDIO Interface

The AW-XM646 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-XM646 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

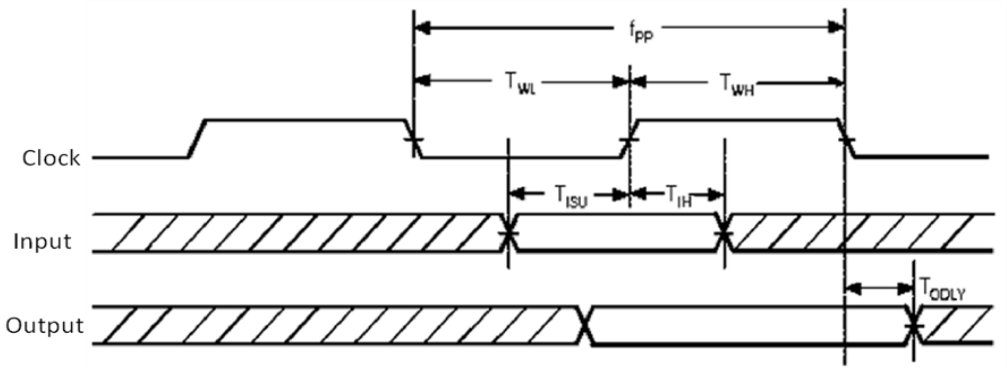
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

SDIO Interface Signals

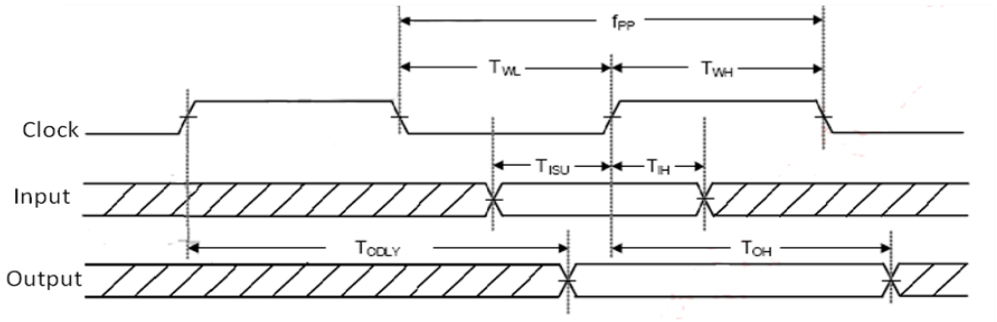
AW-XM646 SDIO Pin Name	Type	Description
SDIO_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

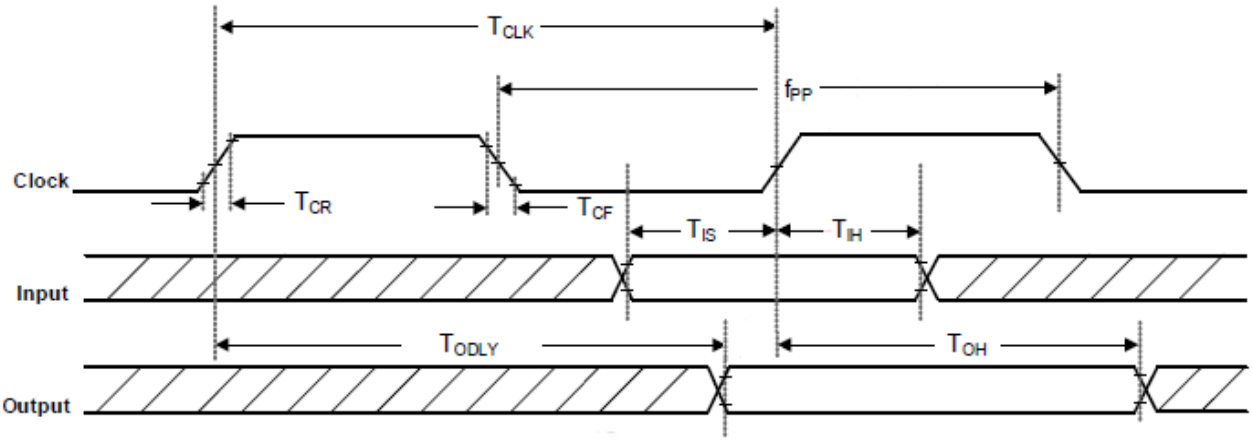


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≦ 40pF (1 card)	High Speed	--	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

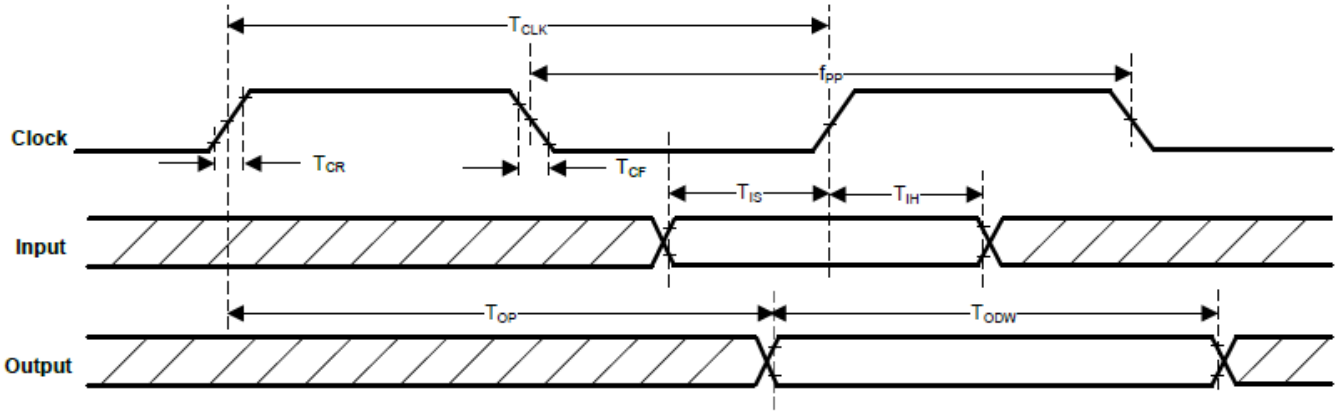


SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR ,TCF <2ns(max) at 100MHz CCARD =10pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output Delay Time CL ≦ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL =15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

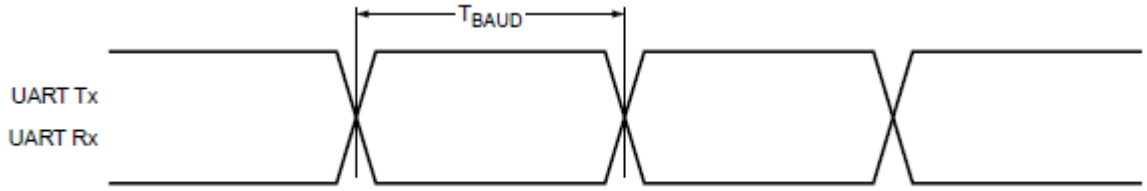
3.4.2.3 SDR104 mode (208MHz) (1.8V)



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR104	0	-	208	MHz
T_{CLK}	Clock Time	SDR104	4.8	-	-	ns
T_{IS}	Input Setup Time	SDR104	1.4	-	-	ns
T_{IH}	Input Hold Time	SDR104	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR,TCF<0.96ns(max) at 208MHz CCARD =10pF	SDR104	-	-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	-	-	ns

3.4.3.High-Speed UART Interface

The AW-XM646 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz or 40MHz input clock	250	-	-	ns

3.4.4 USB Interface

3.4.4.1 USB LS driver and receiver parameters

Symbol	Parameter	Min	Typ	Max	Units
BR	Valid power to PDn deasserted	-	1.5	-	Mbit/s
BR_{PPM}	Input high voltage		-		ppm
Driver specifications					
V_{OH}	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V	-2.8	-	3.6	V
V_{OL}	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground	0.0	-	0.3	V
V_{CRS}	Output single crossover voltage	1.3	-	2.0	V
T_{LR}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	-	300.0	ns
T_{LF}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	-	300.0	ns
T_{LRFM}	Rise and fall time matching	80.0	-	125.0	%
T_{UDJ1}	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals.	-95.0	-	95.0	ns

	• Defined at crossover point of differential data signals.				
T_{UDJ2}	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-150.0	-	150.00	ns
Receiver specifications					
V_{IH}	Input single ended high	2.0	-	-	V
V_{IL}	Input single ended low	-	-	0.8	V
V_{DI}	Differential input sensitivity	0.2	-	-	V

3.4.4.2 USB FS driver and receiver parameters

Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	-	12.0	-	Mbit/s
BR_{PPM}	Baud rate tolerance	-2500.0	-	2500.0	ppm
Driver specifications					
V_{OH}	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.	2.8	--	3.6	V
V_{OL}	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground	0.0	--	0.3	V
V_{CRS}	Output single crossover voltage	1.3	-	2.0	V
T_{FR}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	-	20.0	ns
T_{FL}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	-	20.0	ns
T_{DJ1}	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-3.5	-	3.5	ns
T_{DJ2}	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals.	-4.0	-	4.0	ns

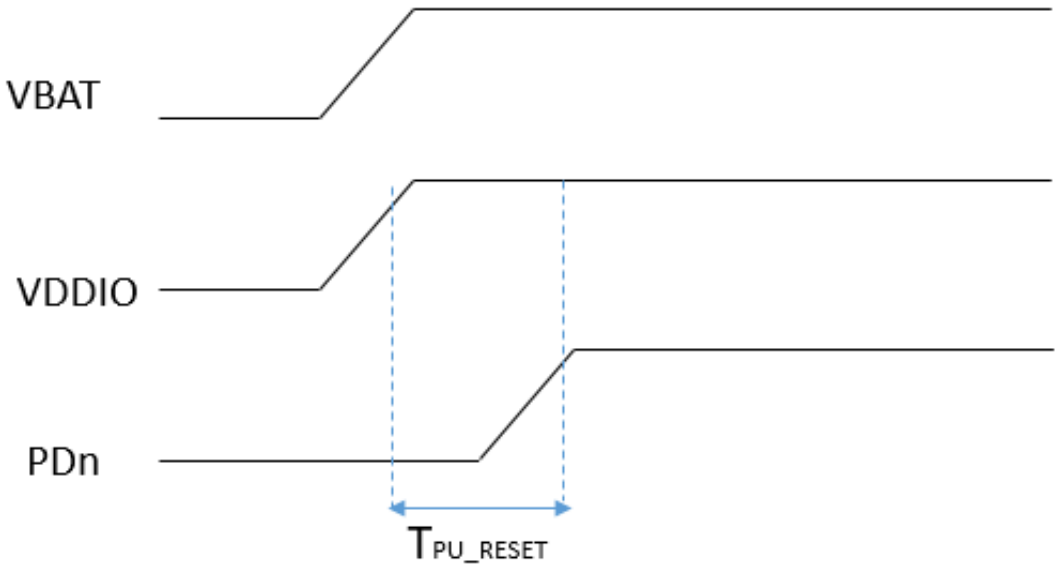
	• Defined at crossover point of differential data signals.				
T_{FDEOP}	Source jitter for differential transition to SE0 transition Defined at crossover point of differential data signals.	-2.0	-	5.0	ns
Receiver specifications					
V_{IH}	Input single ended high	2.0	-	-	V
V_{IL}	Input single ended low	-	-	0.8	V
V_{DI}	Differential input sensitivity	0.2	-	-	V

3.4.4.3 USB HS driver and receiver parameters

Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	-	480.0	-	Mbit/s
BR_{PPM}	Baud rate tolerance	-500.0	-	500.0	ppm
Driver specifications					
V_{HSOH}	Data signaling high	360.0	-	440.0	mV
V_{HSOL}	Data signaling low	-10.0	-	10.0	mV
T_{HSR}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	500.0	-	-	ns
T_{HSF}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-500.0	-	-	ns
Receiver specifications					
V_{HSCM}	Input single ended low	-50	-	500.00	mV

3.5 Timing Sequence

AW-XM646 power up timing sequence.



Symbol	Parameter	Min	Typ	Max	Units
TPU_RESET	Valid power to PDn deasserted	0	-	-	ms
V_{IH}	Input high voltage	1.4	-	4.5	V
V_{IL}	Input low voltage	-0.4	-	0.5	V

3.6 Power Consumption*

3.6.1 WLAN

TBD

3.6.2 Bluetooth

TBD

3.7 Sleep Clock(Optional)

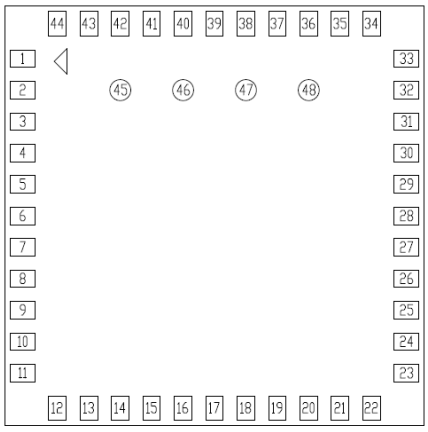
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

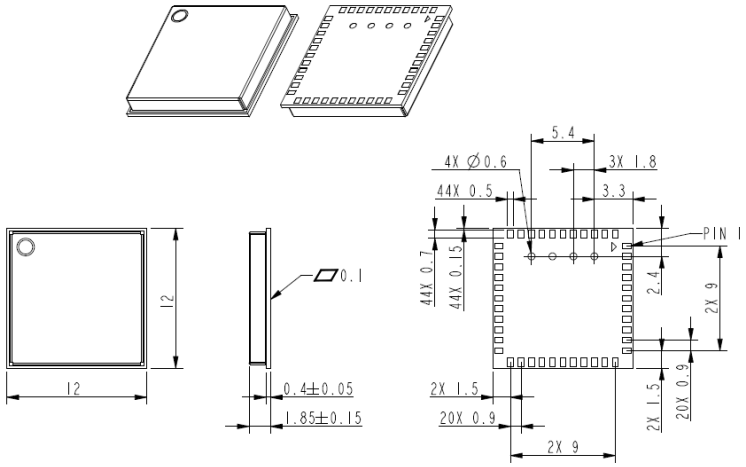
Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock frequency range/ accuracy ■ CMOS input clock signal type ■ ±250 ppm (initial, aging, temperature)	-	32.768	-	kHz
PN	Phase noise requirement (@ 100KHz)	-	-125	-	dBc/Hz
J_C	Cycle jitter	-	1.5	-	ns (RMS)
SR	Slew rate limit (10-90%)	-	-	100	ns
DC	Duty cycle tolerance	20	-	80	%

4. Mechanical Information

4.1 Mechanical Drawing



PIN DEFINED (TOP VIEW)



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

5. Packing Information

TBD