AzureWave Technologies, Inc.

AW-XM553

IEEE 802.11 1X1 a/b/g/n/ac/ax Wireless LAN + Bluetooth 5.3 Combo 12 x 12 LGA Module

Datasheet

Rev. C

DF

For STD

Features

WLAN

- IEEE 802.11a/b/g/n/ac/ax, 1x1 SISO 2.4 GHz and 5 GHz, up to 80 MHz channel
- Integrated high power PA up to +21 dBm transmit power
- Integrated LNA and T/R switches
- UL/DL OFDMA, UL/DL MU-MIMO
- 802.11ax ER, DCM, TWT
- 802.11az accurate ranging
- Security: WPA3 security with hardware encryption engines

Bluetooth

- Supports Bluetooth 5.3 Class 2 and Bluetooth Low Energy
- BDR/EDR packet types—1 Mbps (GFSK), 2 Mbps (/4-DQPSK), 3 Mbps (8DPSK)
- Bluetooth LE long range (125/500 kbps) support improving range by 4x
- Bluetooth LE 2 Mbps
- Bluetooth LE advertising extensions for improved capacity
- Isochronous channels (ISOC) supporting Bluetooth Low Energy (LE) audio
- Security: AES

Revision History

Document NO: R2-2553-DST-02

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2022/09/30	DCN027592	● Initial version	Roger Liu	N.C Chen
B	2023/03/16	DCN028874	● Update power consumption ● Update ESD information ● Update packing information	Roger Liu	N.C Chen
C	2023/07/05	DCN029432	● Update BT feature to 5.3	Roger Liu	N.C Chen

Table of Contents

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n/ac/ax 1x1 dual band WLAN, BT combo module – **AW-XM553.** With full-feature Wi-Fi subsystem integrated into a module, **AW-XM553** provides the best and most convenient SMT process. The module is targeted to smart entertainment, gateways, hubs, bridges, smart home, industrial, point of sale (POS) terminal, smart appliances which need convenient SMT process.

By using **AW-XM553**, the customers can easily integrate the Wi-Fi, BT by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

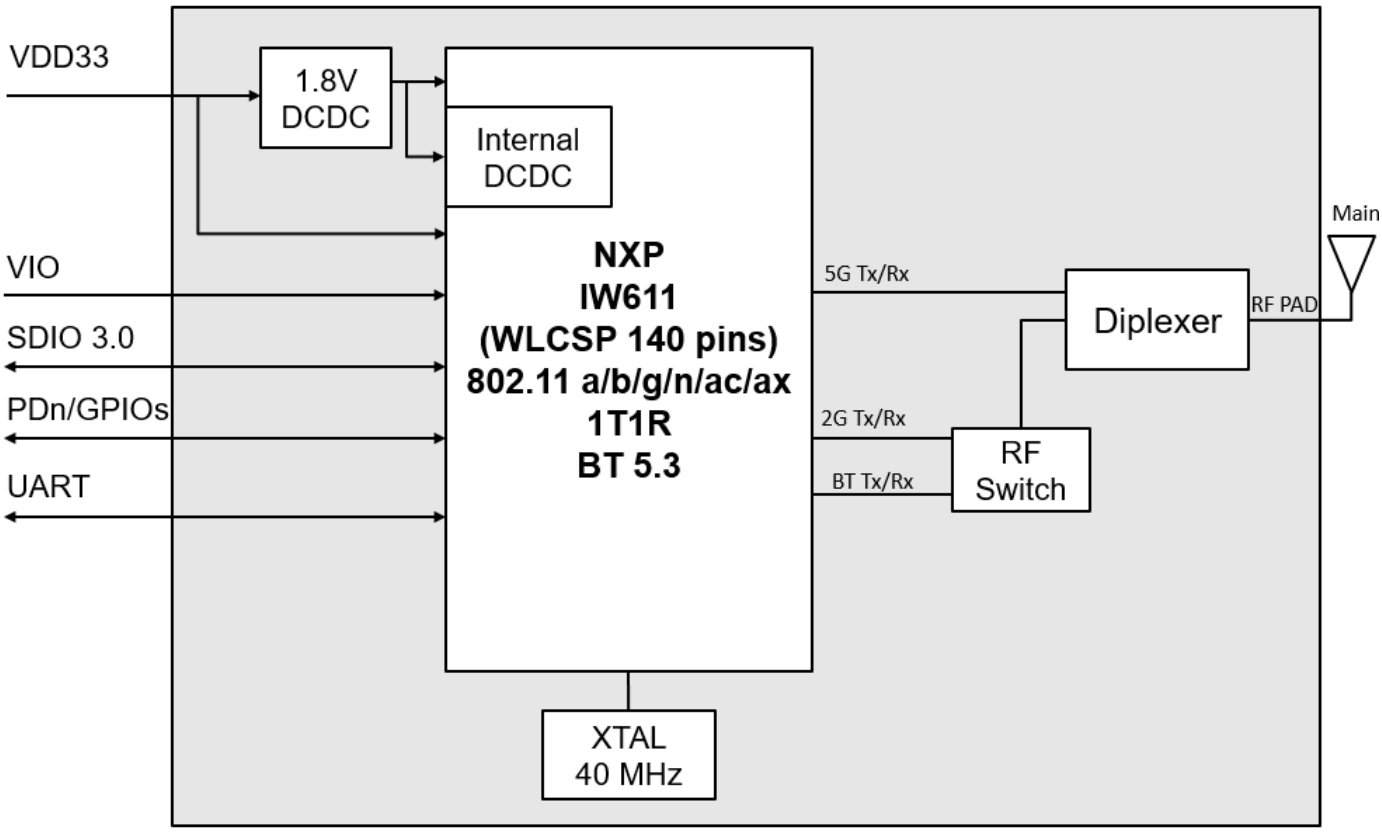
Compliance with the IEEE 802.11 a/b/g/n/ac/ax standard, the **AW-XM553** uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using **AW-XM553**.

The **AW-XM553** supports standard interface **SDIO3.0 for WLAN**, **UART for BT**.

AW-XM553 is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the **AW-XM553** is the best solution for the consumer electronics and smart applications.

1.2 Block Diagram

A simplified block diagram of the AW-XM553 module is depicted in the figure below.



AW-XM553 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi with Bluetooth 5.3 Combo Module
Major Chipset	NXP IW611 WLCSP (140pins)
Host Interface	Wi-Fi + BT ● SDIO + UART
Dimension	12 mm X 12 mm x 2 mm(Max)
Form Factor	LGA module, 48 pins
Antenna	For LGA, “1T1R, external” ANT(Main)：Wi-Fi / Bluetooth→ TX / RX
Weight	0.6 g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6
WLAN VID/PID	NA
WLAN SVID/SPID	NA
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-AQM, 1024-QAM, OFDMA

<table>
<tr><td>Number of Channels</td><td>2.4GHz:
■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11
■ China, Australia, Most European Countries - 1 ~ 13
■ Japan, 1 ~ 13

5GHz:
■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,144,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,144
■ China - 36,40,44,48,52,56,60,64,149,153,157,161,165</td></tr>
<tr><td>Output Power (Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps) @EVM<35%</td><td>15</td><td>17</td><td>19</td><td>dBm</td></tr>
<tr><td>11g (54Mbps) @EVM≦-27 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11) @EVM≦-35 dB</td><td>10.5</td><td>12</td><td>13.5</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11) @EVM≦-35 dB</td><td>10.5</td><td>12</td><td>13.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps) @EVM≦-25 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-27 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8) @EVM≦-31 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9) @EVM≦-32 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9) @EVM≦-32 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11) @EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>11ax(HE40 MCS11)
@EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11)
@EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-85</td><td>-82</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-67</td><td>-64</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS11)</td><td>-</td><td>-57</td><td>-54</td><td>dBm</td></tr>
<tr><td>11ax (HE40 MCS11)</td><td>-</td><td>-57</td><td>-54</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-68</td><td>-65</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-63</td><td>-60</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)</td><td>-</td><td>-62</td><td>-59</td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9)</td><td>-</td><td>-58</td><td>-55</td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9)</td><td>-</td><td>-56</td><td>-53</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11)</td><td>-</td><td>-56</td><td>-53</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11)</td><td>-</td><td>-54</td><td>-51</td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11)</td><td>-</td><td>-53</td><td>-50</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n : Maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)
802.11ac: Maximum data rates up to 433 Mbps (80 MHz channel)
802.11ax: Maximum data rates up to 600 Mbps (80 MHz channel)</td></tr>
<tr><td>Security</td><td>■ Wi-Fi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP
■ BT: AES</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.
* Unless otherwise stated, all RF specifications are at 25°C, nominal voltage, and at chip port.

1.3.3 Bluetooth

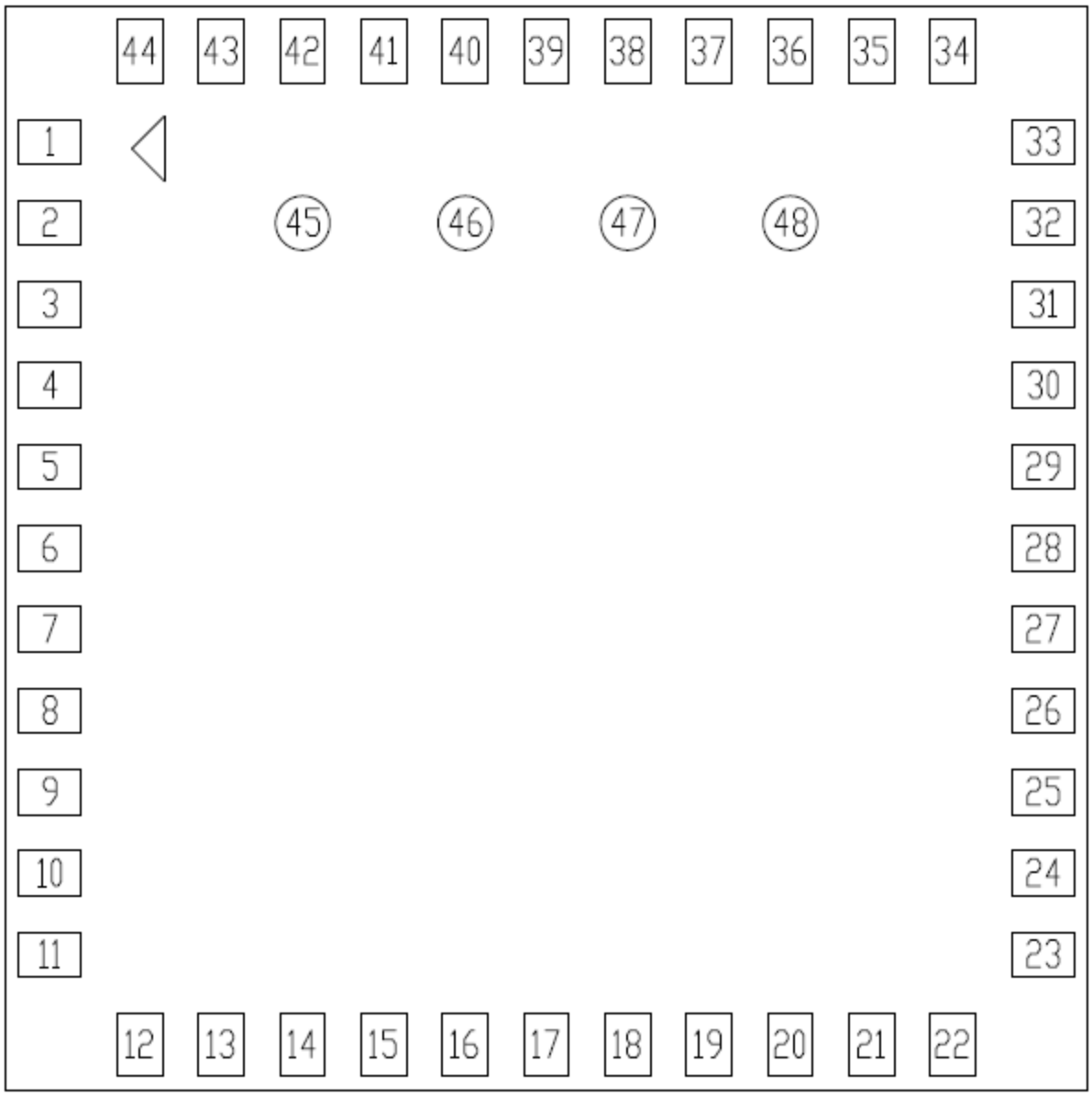
<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Full Bluetooth 5.3 features</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK
Payload 2M: π/4-DQPSK
Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>BDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>BDR(DH1)
(BER<0.1%)</td><td>-</td><td>-89</td><td>-86</td><td>dBm</td></tr>
<tr><td>EDR(2DH5)
(BER<0.007%)</td><td>-</td><td>-87</td><td>-84</td><td>dBm</td></tr>
<tr><td>EDR(3DH5)
(BER<0.007%)</td><td>-</td><td>-81</td><td>-78</td><td>dBm</td></tr>
<tr><td>Low Energy
(PER<30.8%)</td><td>-</td><td>-91</td><td>-88</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	0 ℃ to +70 ℃
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 ℃ to +85 ℃
Storage Humidity	Less than 60% R.H.
ESD Protection	
Human Body Model	+-2kV
Changed Device Model	+-500V

2. Pin Definition

2.1 Pin Map



AW-XM553 Pin Map (top view)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND1	Ground	---	---
2	RF_ANT	WLAN/BT RF pin out	---	I/O
3	GND3	Ground	---	---
4	GPIO[15]	GPIO[15]	VDDIO	I/O
5	GPIO[14]	GPIO[14]	VDDIO	I/O
6	GPIO[18].	GPIO[18].	VDDIO	I/O
7	BT_WAKE_HOST	GPIO Mode : GPIO[19]. BT Host Wake	VDDIO	O
8	GPIO[13]	GPIO[13]	VDDIO	I/O
9	VBAT	3.3V power voltage source input	3.3V	P
10	JTAG_TMS	JTAG test mode select input signal. GPIO[29]	VDDIO	I
11	GPIO[12]	GPIO[12]	VDDIO	I/O
12	PDn	Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode (Need external pull high 51k resistor to VDDIO)	1.8V/3.3V	I
13	WL_WAKE_HOST	GPIO Mode : GPIO[17]. Wi-Fi radio wake-up output signal	VDDIO	O
14	SDIO_DATA2	SDIO Data line Bit[2]	VDDIO	I/O
15	SDIO_DATA3	SDIO Data line Bit[3]	VDDIO	I/O
16	SDIO_CMD	SDIO Command	VDDIO	I/O
17	SDIO_CLK	SDIO Clock input	VDDIO	I
18	SDIO_DATA0	SDIO Data line Bit[0]	VDDIO	I/O
19	SDIO_DATA1	SDIO Data line Bit[1]	VDDIO	I/O
20	GND20	Ground	---	---
21	DCDC_1V8_OUT	Internal DC-DC output (Need external 1uH power inductor)	1.8V	P
22	VDDIO	1.8V/3.3V Digital I/O Power Supply	1.8V/3.3V	P
23	1V8_IN	1.8V power voltage source input	1.8V	P
24	NC24	Floating Pin, No connect to anything.	---	Floating
25	BT_PCM_OUT	PCM Data output / GPIO[5]	VDDIO	O
26	BT_PCM_CLK	PCM Clock / GPIO[4]	VDDIO	I/O
27	BT_PCM_IN	PCM data input / GPIO[6]	VDDIO	I
28	BT_PCM_SYNC	PCM sync signal / GPIO[7]	VDDIO	I/O
29	JTAG_TDO	JTAG test data output signal. GPIO[31]	VDDIO	O
30	JTAG_TDI	JTAG test data input signal. GPIO[30]	VDDIO	I
31	GND31	Ground	---	---
32	NC32	Floating Pin, No connect to anything.	---	Floating
33	GND33	Ground	---	---
34	BT_DIS	Host-to-BT reset /IND_RST_BT - Independent software reset for Bluetooth / GPIO[2]	VDDIO	I

35	JTAG_TCK	JTAG test clock input signal. GPIO[28]	VDDIO	I
36	GND36	Ground	---	---
37	Host-to-Wi-Fi reset	GPIO Mode : GPIO[1] Independent software reset for Wi-Fi	VDDIO	I
38	WCI_SOUT	WCI-2 MWS coexistence serial transport interface(TX) / GPIO[26]	VDDIO	I/O
39	WCI_SIN	WCI-2 MWS coexistence serial transport interface(RX) / GPIO[25]	VDDIO	I/O
40	GPIO[16]	GPIO[16]	VDDIO	I/O
41	UART_RTS_N	UART_RTSn (active low)	VDDIO	O
42	UART_TXD	UART_SOUT	VDDIO	O
43	UART_RXD	UART_SIN	VDDIO	I
44	UART_CTS	UART_CTS (active low)	VDDIO	I
45	GND45	Ground	---	---
46	GPIO[24]	GPIO[24]	VDDIO	I/O
47	GPIO[22]	GPIO[22]	VDDIO	I/O
48	GPIO[20]	GPIO[20]	VDDIO	I/O

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	-	3.3	3.96	V
VDDIO	I/O power supply	-	3.3	3.96	V
		-	1.8	2.16	

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	3.14	3.3	3.46	V
VDDIO	1.8V/3.3V digital I/O power supply	3.14	3.3	3.46	V
		1.71	1.8	1.98	

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.4 Host Interface

3.4.1 SDIO Interface

The AW-XM553 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-XM553 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

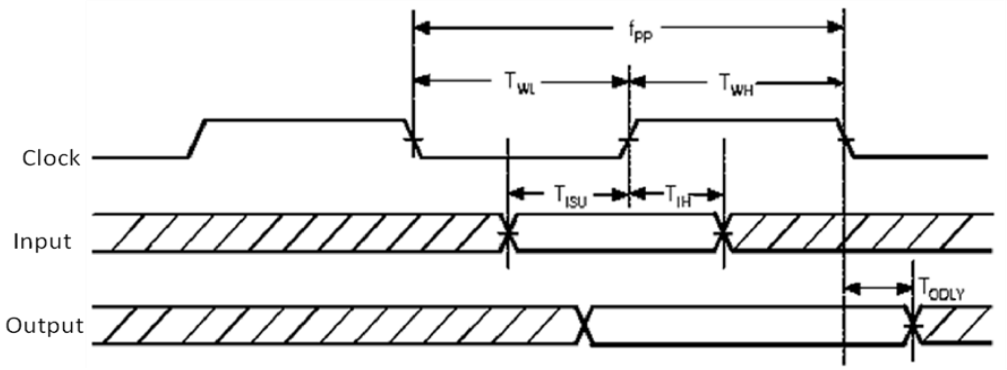
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

SDIO Interface Signals

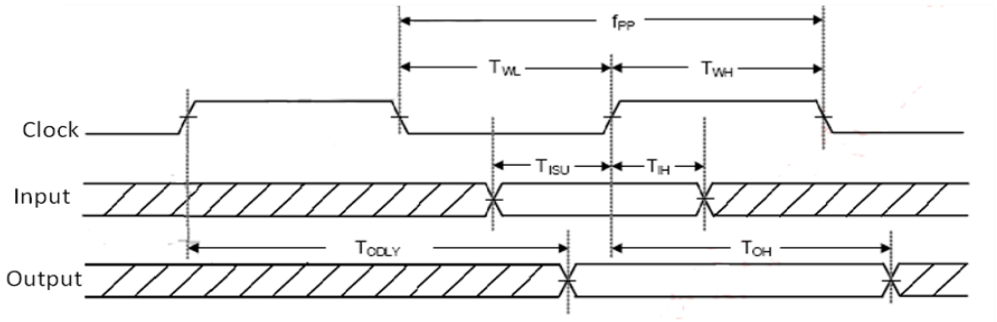
AW-XM553 SDIO Pin Name	Type	Description
SDIO_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

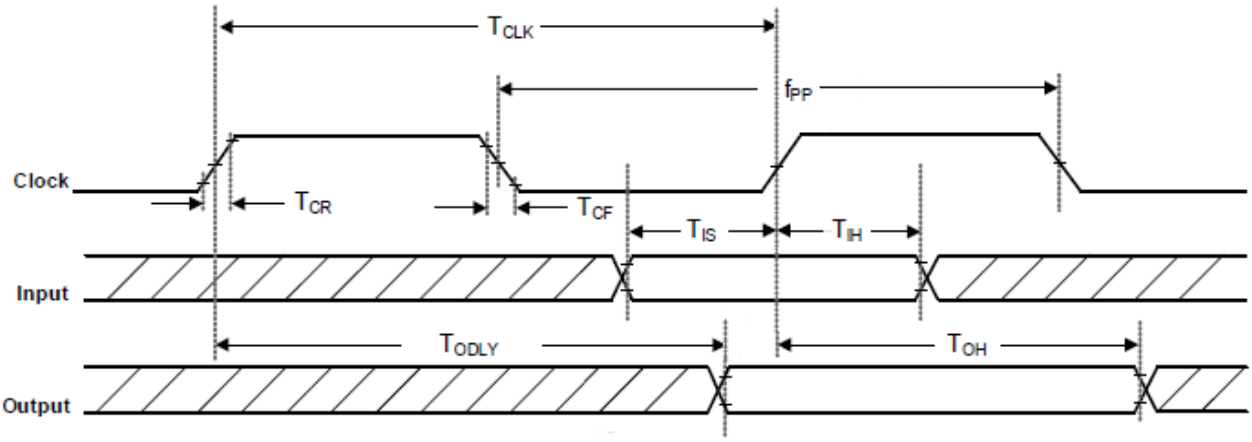


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≦ 40pF (1 card)	High Speed	--	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

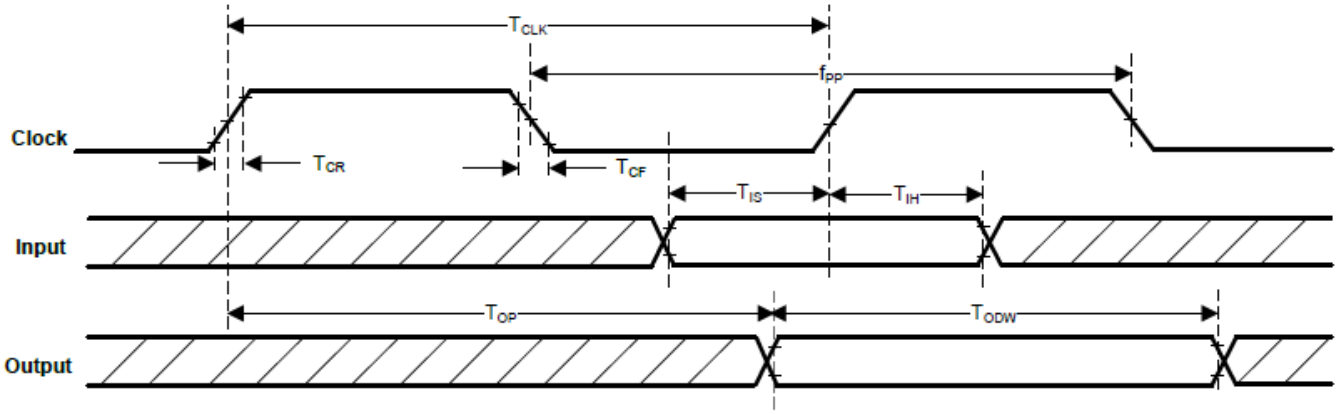


SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR ,TCF <2ns(max) at 100MHz CCARD =10pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output Delay Time CL ≦ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL =15pF	SDR12/25/50	1.5	-	-	ns

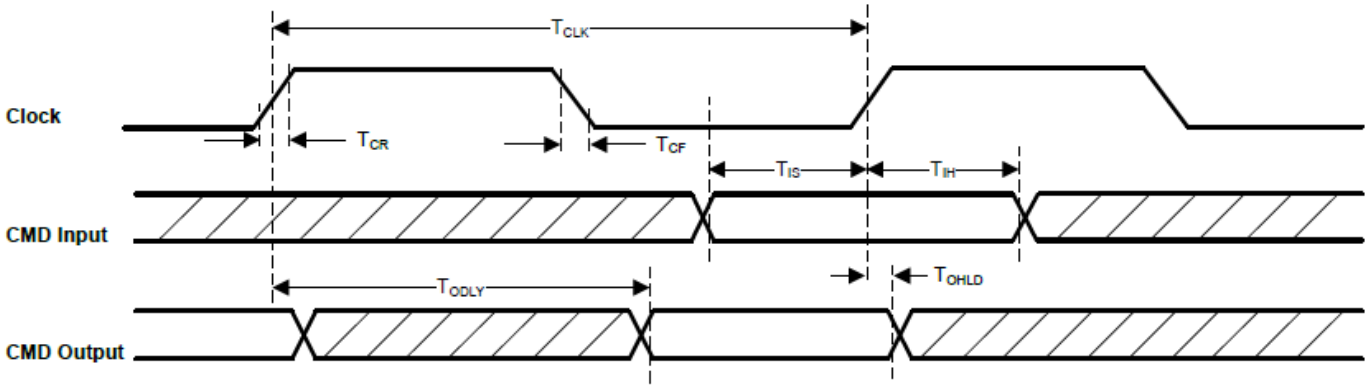
SDIO Timing Data - SDR12/25/50 modes. (1.8V)

3.4.2.3 SDR104 mode (208MHz) (1.8V)

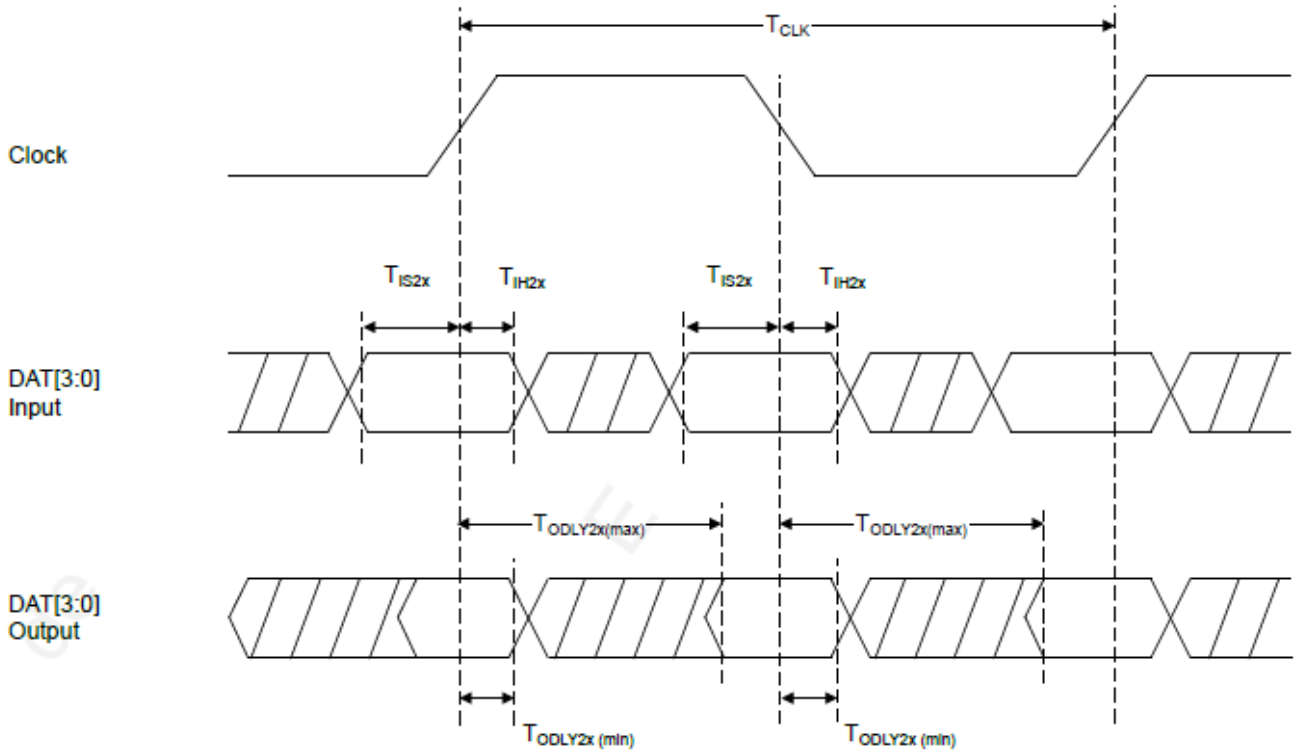


Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR104	0	-	208	MHz
T_{CLK}	Clock Time	SDR104	4.8	-	-	ns
T_{IS}	Input Setup Time	SDR104	1.4	-	-	ns
T_{IH}	Input Hold Time	SDR104	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR,TCF<0.96ns(max) at 208MHz CCARD =10pF	SDR104	-	-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	-	-	ns

3.4.2.4 DDR50 mode (50MHz) (1.8V)



SDIO CMD timing diagram—DDR50 mode (50 MHz)



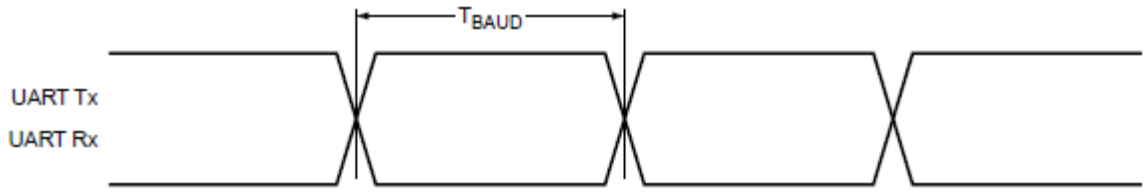
SDIO DAT[3:0] timing diagram—DDR50 mode(50 MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	-	-	ns
T_{CR} ,T_{CF}	Rise time, fall time TCR, TCF < 4.00 ns (max) at 50 MHz CCARD = 10 pF	DDR50	-	-	0.2* T_{CLK}	ns
Clock Duty	-	DDR50	45	-	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time CCARD ≤ 10 pF (1 card)	DDR50	6	-	-	ns
T_{IH}	Input hold time CCARD ≤ 10 pF (1 card)	DDR50	0.8	-	-	ns

CMD Output (referenced to clock rising edge)						
T_{ODLY}	Input Hold Time	DDR50	-	-	13.7	ns
T_{OHLD}	Output hold time CL ≥ 15 pF (1 card)	DDR50	1.5	-	-	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time CCARD ≤ 10 pF (1 card)	DDR50	3	-	-	ns
T_{IH2x}	Input hold time CCARD ≤ 10 pF (1 card)	DDR50	0.8	-	-	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x(max)}$	Output delay time during data transfer mode CL ≤ 25 pF (1 card)	DDR50	-	-	7.0	ns
$T_{ODLY2x(min)}$	Output hold time CL ≥ 15 pF (1 card)	DDR50	1.5	-	-	ns

3.4.3.High-Speed UART Interface

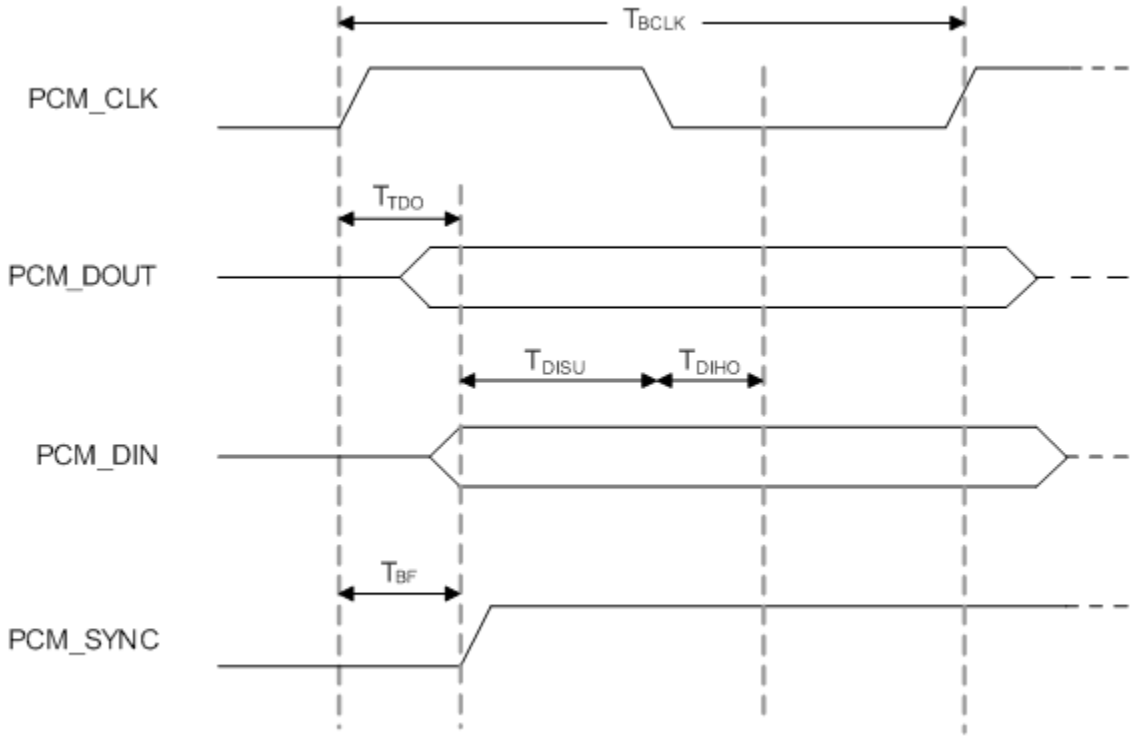
The AW-XM553 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	40MHz input clock	250	-	-	ns

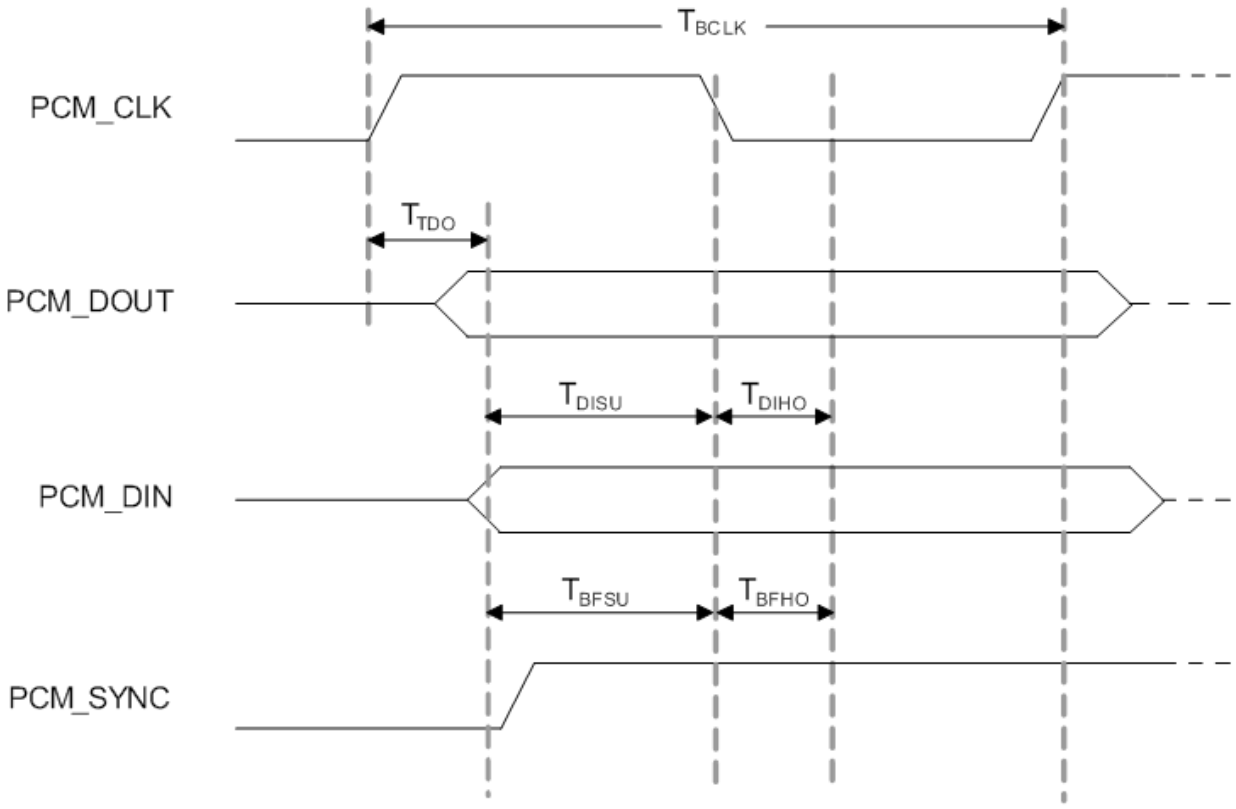
3.4.4 PCM Interface

3.4.4.1 PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

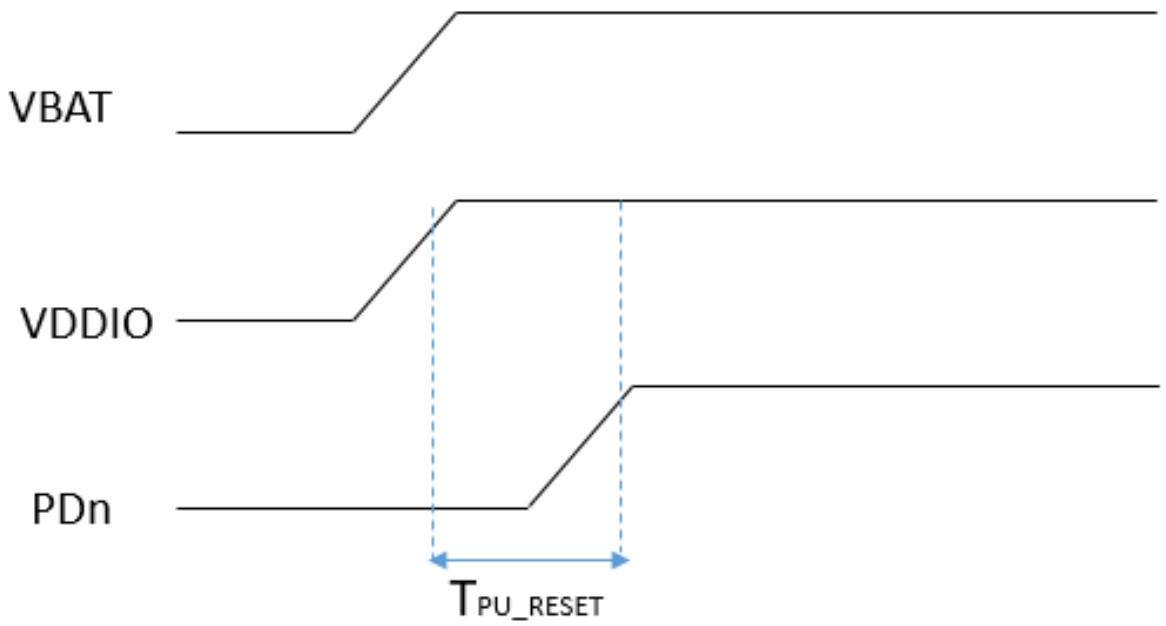
3.4.4.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}			10		--	ns

3.5 Timing Sequence

AW-XM553 power up timing sequence.



Symbol	Parameter	Min	Typ	Max	Units
TPU_RESET	Valid power to PDn deasserted	0	-	-	ms
VIH	Input high voltage	1.4	-	4.5	V
VIL	Input low voltage	-0.4	-	0.5	V

3.6 Power Consumption*

3.6.1 WLAN

No.	Item			VBAT_3.3V		
				Transmit		
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Max. (mA)	Avg. (mA)	Duty Mean (%)
2.4	11b@1Mbps	20	15	290	286	99
	11g@54Mbps	20	12	261	258	87
	11n@MCS0	40	10	255	251	96
	11n@MCS7	40	10	250	240	78
	11ax@MCS0 NSS1	40	8	246	244	95
	11ax@MCS11 NSS1	40	8	225	223	75
5	11a@6Mbps	20	16	414	409	98
	11n@MCS0	40	15	409	396	96
	11n@MCS7	40	15	358	355	81
	11ac@MSC0 NSS1	20	14	373	372	98
	11ac@MSC8 NSS1	20	14	350	349	87
	11ac@MSC0 NSS1	40	14	375	372	96
	11ac@MSC9 NSS1	40	14	339	338	79
	11ac@MSC0 NSS1	80	14	378	376	93
	11ac@MSC9 NSS1	80	14	334	333	73
	11ax@MSC0 NSS1	20	11	327	324	97
	11ax@MSC11 NSS1	20	11	303	302	83
	11ax@MSC0 NSS1	40	11	330	329	96
	11ax@MSC11 NSS1	40	11	298	297	78
	11ax@MSC0 NSS1	80	11	334	332	92
	11ax@MSC11 NSS1	80	11	302	301	76

Band (GHz)	Mode	BW(MHz)	Receive	
			Max. (mA)	Avg. (mA)
2.4	11b@11Mbps	20	67	66
	11n@MCS7	40	79	78
	11ax@MCS11 NSS1	40	79	78
5	11a@54Mbps	20	84	83
	11n@MCS7	40	92	91
	11ac@MCS9 NSS1	80	106	105
	11ax@MCS11 NSS1	80	104	103

	Item			VIO_3.3V	
				Transmit	
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Max. (uA)	Avg. (uA)
2.4	11b@1Mbps	20	15	341	340

	11ax@MCS11 NSS1	40	8	344	342
5	11a@6Mbps	20	16	341	339
	11ax@MSC11 NSS1	80	11	343	342
Band (GHz)	Mode	BW(MHz)		Receive	
				Max. (uA)	Avg. (uA)
2.4	11b@11Mbps	20		349	348
	11ax@MCS11 NSS1	80		348	347

	Item			VIO_1.8V	
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit	
				Max. (uA)	Avg. (uA)
2.4	11b@1Mbps	20	15	116	115
	11ax@MCS11 NSS1	40	8	116	115
5	11a@6Mbps	20	16	116	115
	11ax@MSC11 NSS1	80	11	116	115
Band (GHz)	Mode	BW(MHz)		Receive	
				Max. (uA)	Avg. (uA)
2.4	11b@11Mbps	20		116	115
	11ax@MCS11 NSS1	80		116	115

3.6.2 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	VBAT_IN=3.3V(mA)	
				Max.	Avg.
1	Transmit*(2)	DH5	2	40	38
2	Receive*(2)	3-DH5	n/a	32	26

No.	Mode	Packet Type	RF Power (dBm)	VDDIO=3.3V(uA)	
				Max.	Avg.
1	Transmit*(2)	DH5	2	401	400
2	Receive*(2)	3-DH5	n/a	401	400

No.	Mode	Packet Type	RF Power (dBm)	VDDIO=1.8V(uA)	
				Max.	Avg.
1	Transmit*(2)	DH5	2	75	74
2	Receive*(2)	3-DH5	n/a	75	74

3.7 Sleep Clock(Optional)

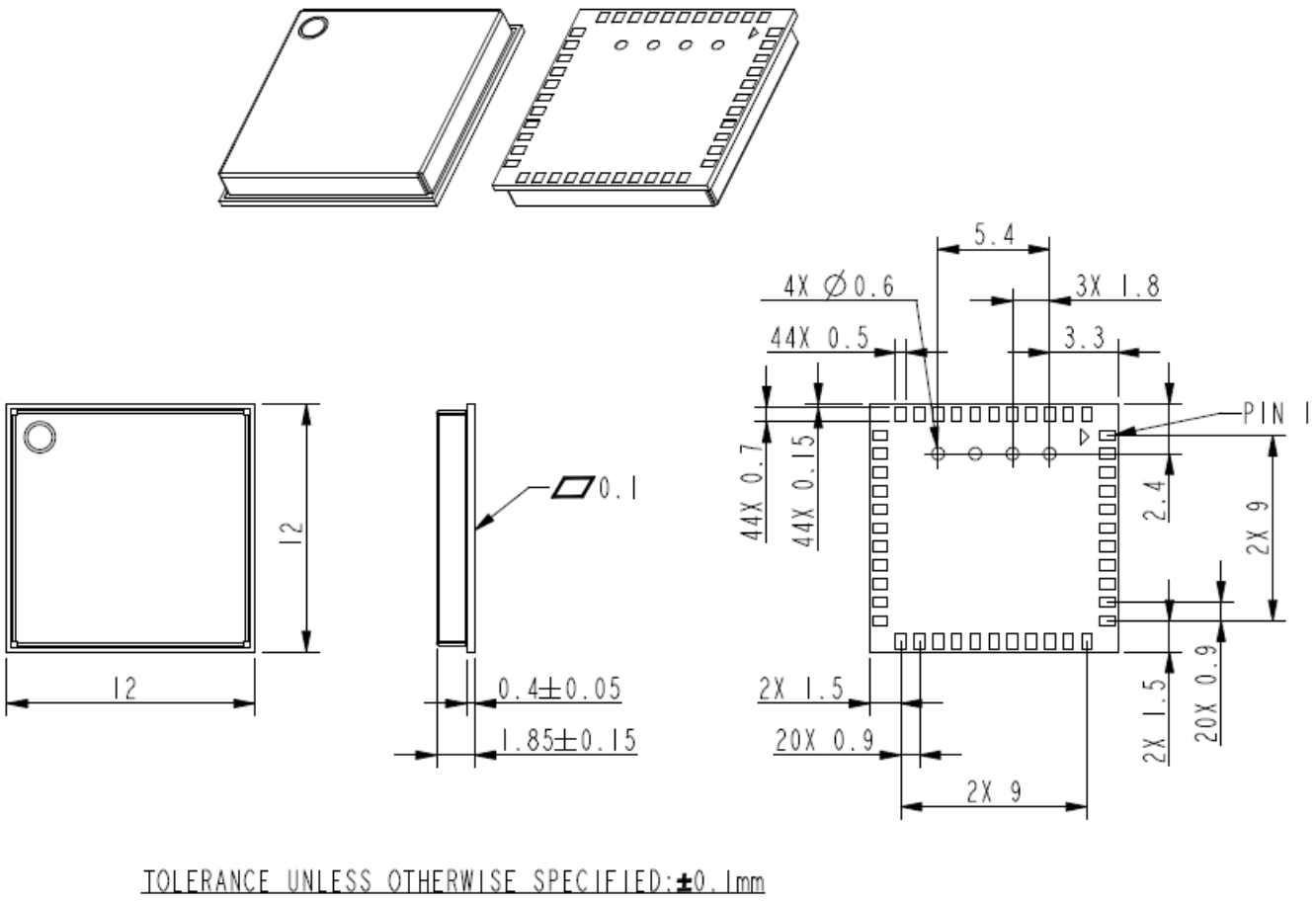
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock frequency range/ accuracy ■ CMOS input clock signal type ■ ±250 ppm (initial, aging, temperature)	-	32.768	-	kHz
PN	Phase noise requirement (@ 100KHz)	-	-125	-	dBc/Hz
J_C	Cycle jitter	-	1.5	-	ns (RMS)
SR	Slew rate limit (10-90%)	-	-	100	ns
DC	Duty cycle tolerance	20	-	80	%

4. Mechanical Information

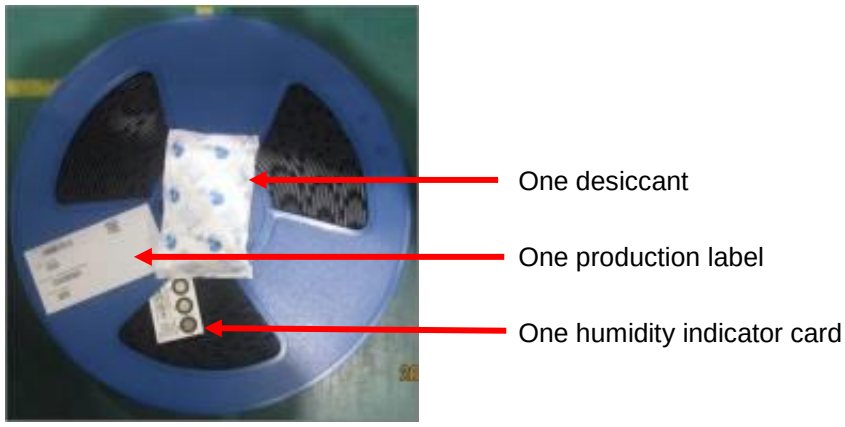
4.1 Mechanical Drawing



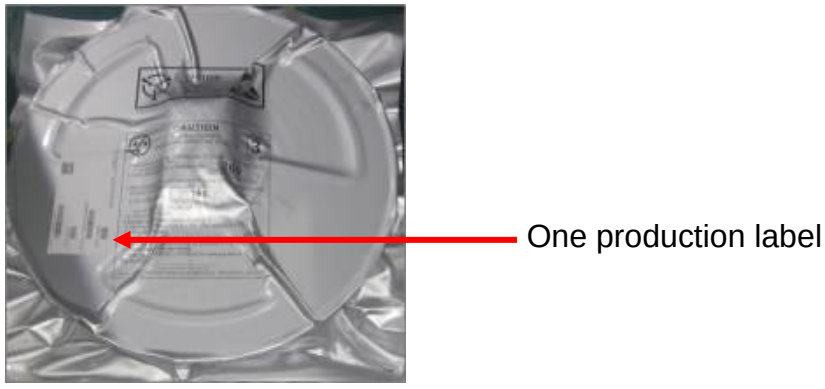
TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

5. Packing Information

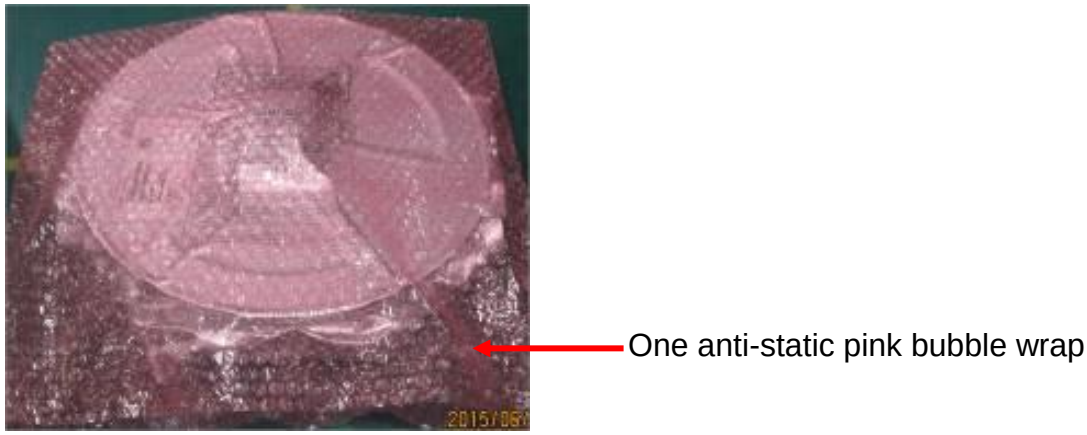
1. One reel can pack 1,500pcs 12x12 LGA modules
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



4. A bag is put into the anti-static pink bubble wrap



5. A bubble wrap is put into the inner box and then one label is pasted on the inner box

6. 5 inner boxes could be put into one carton

7. Sealing the carton by AzureWave tape

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton

One carton label

One box label