AzureWave Technologies, Inc.

AW-XM549

IEEE 802.11 1X1 a/b/g/n/ac/ax Wireless LAN + Bluetooth 5.4 + 802.15.4 Tri-radio 12 x 12 LGA Module

Datasheet

Rev. C

DF

For Standard

Features

WLAN

- IEEE 802.11a/b/g/n/ac/ax, 1x1 SISO 2.4 GHz and 5 GHz, up to 80 MHz channel
- Integrated high power PA up to +21 dBm transmit power
- Integrated LNA and T/R switches
- UL/DL OFDMA, UL/DL MU-MIMO
- 802.11ax ER, DCM, TWT
- 802.11az accurate ranging
- Security: WPA3 security with hardware encryption engines

Bluetooth

- Supports Bluetooth 5.4 Class 2 and Bluetooth Low Energy
- BDR/EDR packet types—1 Mbps (GFSK), 2 Mbps (/4-DQPSK), 3 Mbps (8DPSK)
- Bluetooth LE long range (125/500 kbps) support improving range by 4x
- Bluetooth LE 2 Mbps
- Bluetooth LE advertising extensions for improved capacity
- Isochronous channels (ISOC) supporting Bluetooth Low Energy (LE) audio
- Security: AES

802.15.4

- IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
- Shared transmitter and antenna pin with Bluetooth
- Simultaneous receive with Wi-Fi and Bluetooth
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers

Revision History

Document NO: R2-2549-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2022/07/01	DCN026641	● Draft version	Roger Liu	N.C Chen
B	2023/08/05	DCN029872	● Update BT feature to 5.3 ● Update RF specification Update power consumption	Roger Liu	N.C Chen
C	2024/12/06	DCN032958	● Update BT feature to BT5.4	Roger Liu	N.C Chen

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n/ac/ax 1x1 dual band WLAN, BT, and 802.15.4 tri-radio module – **AW-XM549.** With full-feature Wi-Fi subsystem integrated into a module, **AW-XM549** provides the best and most convenient SMT process. The module is targeted to smart entertainment, gateways, hubs, bridges, smart home, industrial, point of sale (POS) terminal, smart appliances which need convenient SMT process.

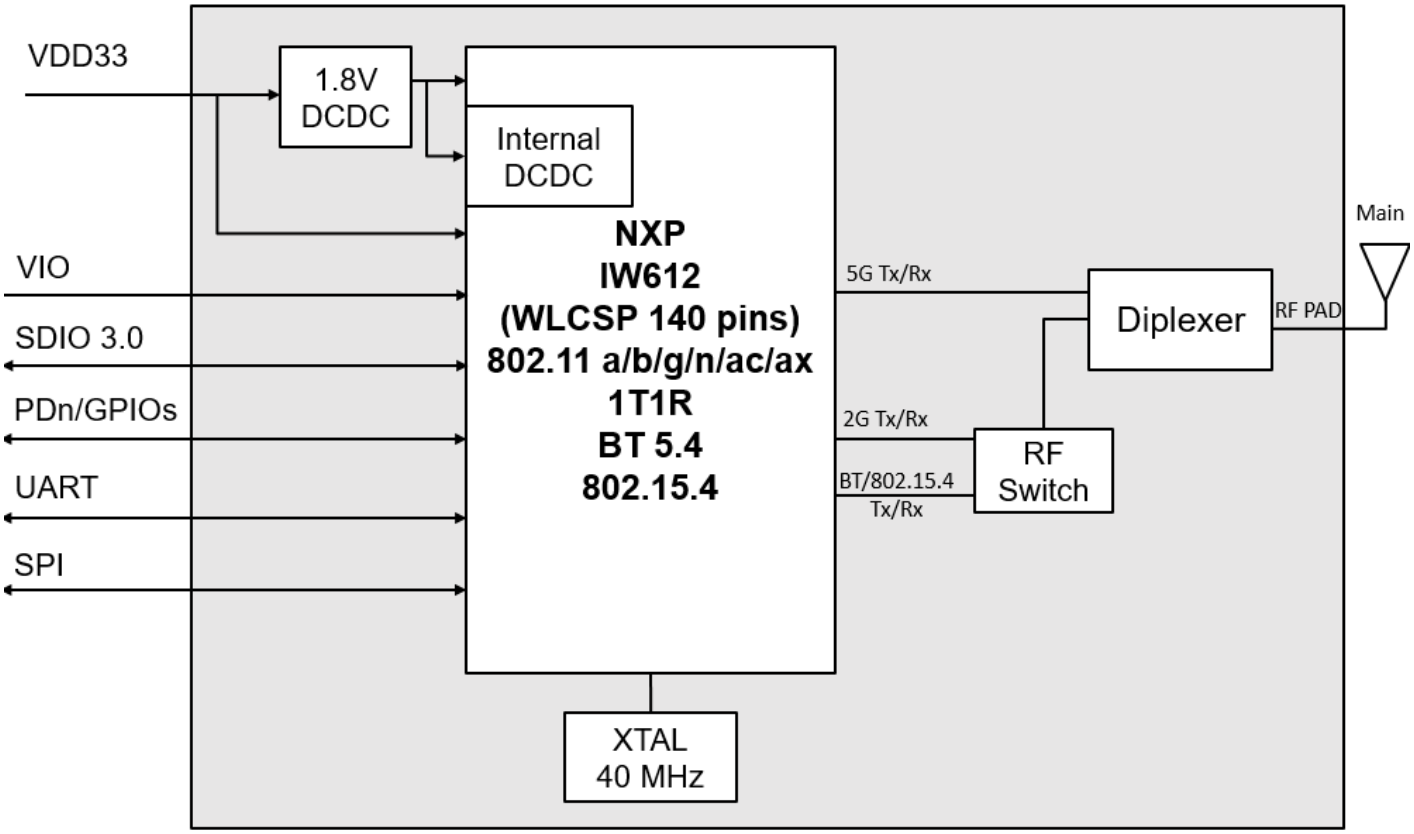
By using **AW-XM549**, the customers can easily integrate the Wi-Fi, BT, 802.15.4 by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11 a/b/g/n/ac/ax standard, the **AW-XM549** uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using **AW-XM549**.

The **AW-XM549** supports standard interface **SDIO3.0 for WLAN**, **UART for BT and SPI for 802.15.4**. AW-XM549 is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the **AW-XM549** is the best solution for the consumer electronics and smart applications.

1.2 Block Diagram

A simplified block diagram of the AW-XM549 module is depicted in the figure below.



AW-XM549 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi with Bluetooth 5.4 and 802.15.4 tri-radio Module
Major Chipset	NXP IW612 WLCSP (140pins)
Host Interface	WiFi + BT + 802.15.4 ● SDIO + UART + SPI
Dimension	12 mm X 12 mm x 2 mm(Max)
Form Factor	LGA module, 48 pins
Antenna	For LGA, “1T1R, external” ANT(Main)：Wi-Fi / Bluetooth/802.15.4→ TX / RX
Weight	0.6 g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6
WLAN VID/PID	NA
WLAN SVID/SPID	NA
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-QAM, 1024-QAM, OFDMA

<table>
<tr><td>Number of Channels</td><td>2.4GHz:
■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11
■ China, Australia, Most European Countries - 1 ~ 13
■ Japan, 1 ~ 13

5GHz:
■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140
■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power (Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps) @EVM<35%</td><td>15</td><td>17</td><td>19</td><td>dBm</td></tr>
<tr><td>11g (54Mbps) @EVM≦-27 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11) @EVM≦-35 dB</td><td>10.5</td><td>12</td><td>13.5</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11) @EVM≦-35 dB</td><td>10.5</td><td>12</td><td>13.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps) @EVM≦-27 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8) @EVM≦-31 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9) @EVM≦-32 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9) @EVM≦-32 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11) @EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>11ax(HE40 MCS11)
@EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11)
@EVM≦-35 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-85</td><td>-82</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-67</td><td>-64</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS11)</td><td>-</td><td>-57</td><td>-54</td><td>dBm</td></tr>
<tr><td>11ax (HE40 MCS11)</td><td>-</td><td>-57</td><td>-54</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-68</td><td>-65</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-63</td><td>-60</td><td>dBm</td></tr>
<tr><td>11ac(VHT20 MCS8)</td><td>-</td><td>-62</td><td>-59</td><td>dBm</td></tr>
<tr><td>11ac(VHT40 MCS9)</td><td>-</td><td>-58</td><td>-55</td><td>dBm</td></tr>
<tr><td>11ac(VHT80 MCS9)</td><td>-</td><td>-56</td><td>-53</td><td>dBm</td></tr>
<tr><td>11ax(HE20 MCS11)</td><td>-</td><td>-56</td><td>-53</td><td>dBm</td></tr>
<tr><td>11ax(HE40 MCS11)</td><td>-</td><td>-54</td><td>-51</td><td>dBm</td></tr>
<tr><td>11ax(HE80 MCS11)</td><td>-</td><td>-53</td><td>-50</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n : Maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)
802.11ac: Maximum data rates up to 433 Mbps (80 MHz channel)
802.11ax: Maximum data rates up to 600 Mbps (80 MHz channel)</td></tr>
<tr><td>Security</td><td>■ WiFi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP
■ BT: AES
■ 802.15.4 :AES</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Full Bluetooth 5.4 features</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK
Payload 2M: π/4-DQPSK
Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>BDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>BDR(DH1)</td><td>-</td><td>-89</td><td>-86</td><td>dBm</td></tr>
<tr><td>EDR(2DH5)</td><td>-</td><td>-87</td><td>-84</td><td>dBm</td></tr>
<tr><td>EDR(3DH5)</td><td>-</td><td>-81</td><td>-78</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>-</td><td>-91</td><td>-88</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

1.3.4 Thread

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Thread Standard</td><td>IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band</td></tr>
<tr><td>Frequency Rage</td><td>2400MHz~2483.5MHz</td></tr>
<tr><td>Modulation</td><td>O-QPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>Thread</td><td>2</td><td>4</td><td>6</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

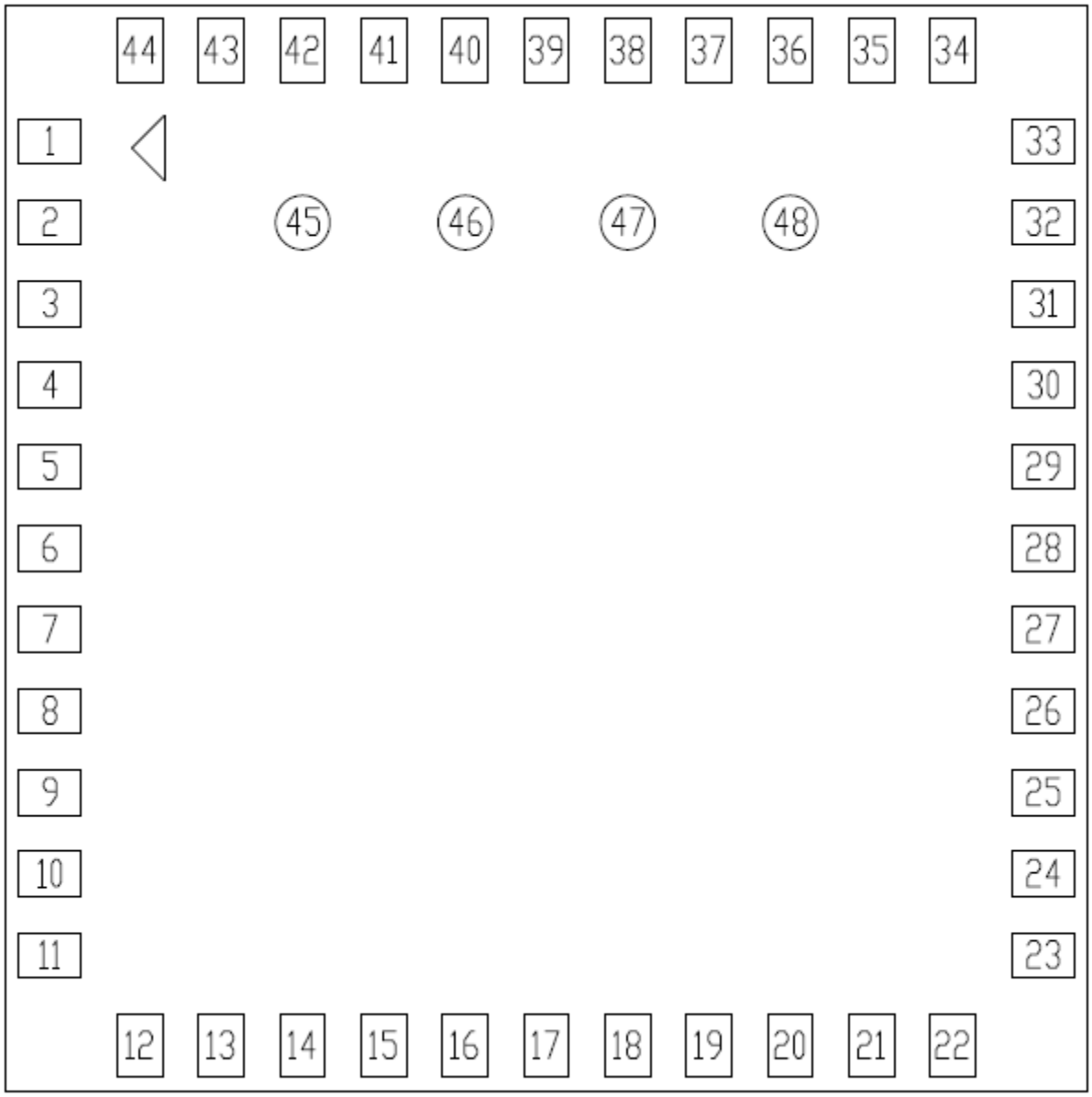
<table>
<tr>
<td>Receiver Sensitivity</td>
<td>Thread Sensitivity (PER<1%)
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>Thread</td><td>-</td><td>-95</td><td>-92</td><td>dBm</td></tr>
</table>
</td>
</tr>
</table>

1.3.5 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	0 ºC to +70 ºC
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 ºC to +85 ºC
Storage Humidity	Less than 60% R.H.
ESD Protection	
Human Body Model	+-2kV
Changed Device Model	+-500V

2. Pin Definition

2.1 Pin Map



AW-XM549 Pin Map (top view)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND1	Ground	---	---
2	RF_ANT	RF pin out	---	I/O
3	GND3	Ground	---	---
4	SPI_TXD	SPI receive output signal	VDDIO	I/O
5	SPI_RXD	SPI receive input signal	VDDIO	I/O
6	HOST_WAKE_ BT	GPIO Mode : GPIO[18]. BT Device Wake	VDDIO	I/O
7	BT_WAKE_HOST	GPIO Mode : GPIO[19]. BT Host Wake	VDDIO	I/O
8	SPI_FRM	SPI_FRM - SPI frame signal	VDDIO	I/O
9	VBAT	3.3V power voltage source input	3.3V	P
10	JTAG_TMS	JTAG test mode select input signal. GPIO[29]	VDDIO	I/O
11	SPI_CLK	SPI_CLK - SPI clock signal	VDDIO	I/O
12	PDn	Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode (Need external pull high 51k resistor to VDDIO)	1.8V/3.3V	I
13	WL_WAKE_HOST	GPIO Mode : GPIO[17]. Wi-Fi radio wake-up output signal	VDDIO	O
14	SDIO_DATA2	SDIO Data line Bit[2]	VDDIO	I/O
15	SDIO_DATA3	SDIO Data line Bit[3]	VDDIO	I/O
16	SDIO_CMD	SDIO Command	VDDIO	I/O
17	SDIO_CLK	SDIO Clock input	VDDIO	I
18	SDIO_DATA0	SDIO Data line Bit[0]	VDDIO	I/O
19	SDIO_DATA1	SDIO Data line Bit[1]	VDDIO	I/O
20	GND20	Ground	---	---
21	DCDC_1V8_OUT	Internal DC-DC output (Need external 1uH power inductor)	1.8V	P
22	VDDIO	1.8V/3.3V Digital I/O Power Supply	1.8V/3.3V	P
23	1V8_IN	1.8V power voltage source input	1.8V	P
24	NC24	Floating Pin, No connect to anything.	---	Floating
25	BT_PCM_OUT	PCM Data output / GPIO[5]	VDDIO	O
26	BT_PCM_CLK	PCM Clock / GPIO[4]	VDDIO	I/O
27	BT_PCM_IN	PCM data input / GPIO[6]	VDDIO	I
28	BT_PCM_SYNC	PCM sync signal / GPIO[7]	VDDIO	I/O
29	JTAG_TDO	JTAG test data output signal. GPIO[31]	VDDIO	O
30	JTAG_TDI	JTAG test data input signal. GPIO[30]	VDDIO	I
31	GND31	Ground	---	---
32	NC32	Floating Pin, No connect to anything.	---	Floating
33	GND33	Ground	---	---
34	BT_DIS	Host-to-BT reset /IND_RST_BT - Independent	VDDIO	I

		software reset for Bluetooth / GPIO[2]		
35	JTAG_TCK	JTAG test clock input signal. GPIO[28]	VDDIO	I
36	GND36	Ground	---	---
37	Host-to-Wi-Fi reset	GPIO Mode : GPIO[1]. Independent software reset for Wi-Fi	VDDIO	I
38	MWS_SOUT	WCI-2 MWS coexistence serial transport interface(TX) / GPIO[26]	VDDIO	I/O
39	MWS_SIN	WCI-2 MWS coexistence serial transport interface(RX) / GPIO[25]	VDDIO	I/O
40	HOST_WAKE_WL	GPIO Mode : GPIO[16]. Host-to-WLAN wake / Wi-Fi radio wake-up input signal	VDDIO	I
41	UART_RTS_N	UART_RTSn (active low)	VDDIO	O
42	UART_TXD	UART_SOUT	VDDIO	O
43	UART_RXD	UART_SIN(active high)	VDDIO	I
44	UART_CTS	UART_CTS(active high)	VDDIO	I
45	GND45	Ground	---	---
46	IND_RST_15.4	Independent software reset for 802.15.4 / GPIO[24]	VDDIO	I/O
47	RST_IND	Independent software reset indicator output signal to host / GPIO[22]	VDDIO	I/O
48	SPI_INT	SPI interrupt signal / GPIO[20]	VDDIO	I/O

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	-	3.3	3.96	V
VDDIO	I/O power supply	-	3.3	3.96	V
		-	1.8	2.16	

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	3.14	3.3	3.46	V
VDDIO	1.8V/3.3V digital I/O power supply	3.14	3.3	3.46	V
		1.71	1.8	1.98	

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.4 Host Interface

3.4.1 SDIO Interface

The AW-XM549 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-XM549 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

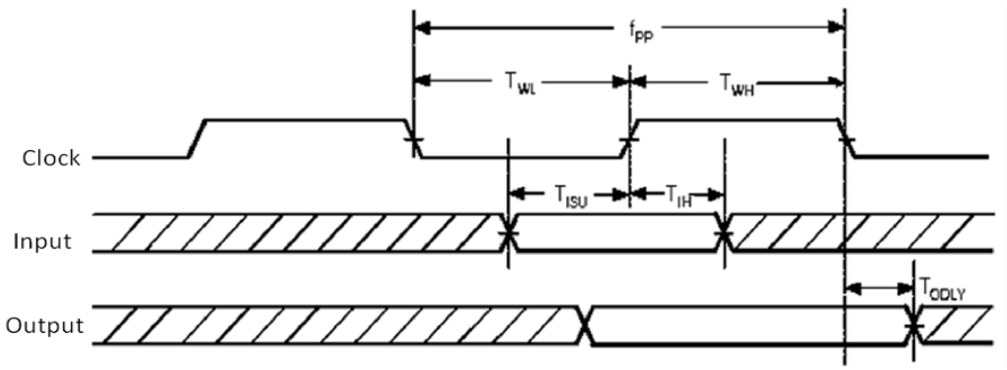
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

SDIO Interface Signals

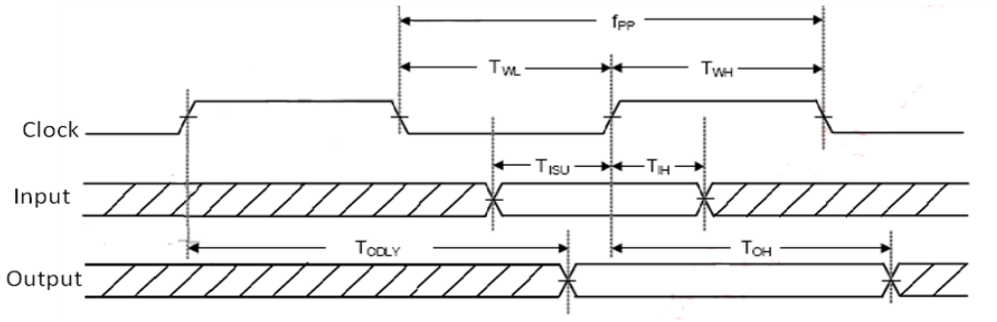
AW-XM549 SDIO Pin Name	Type	Description
SDIO_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

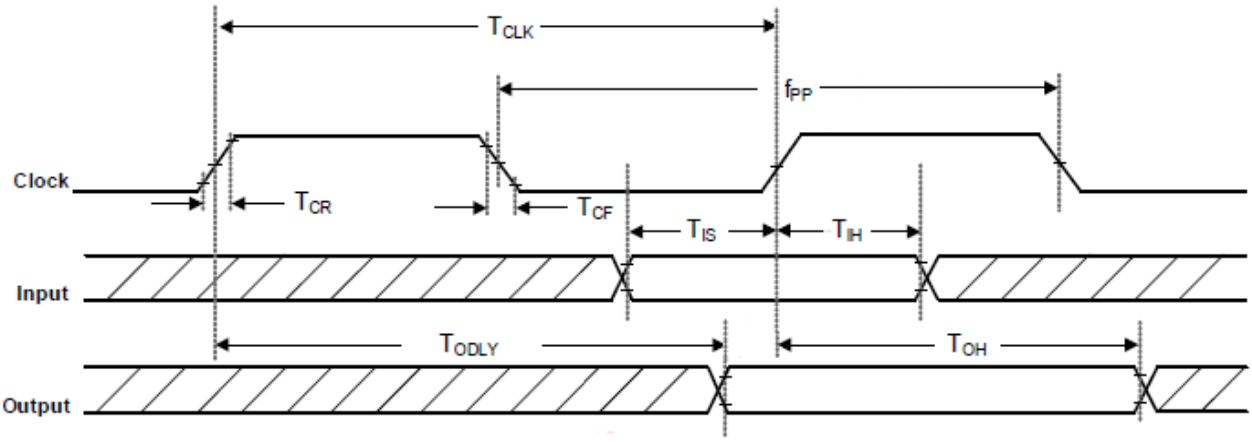


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≦ 40pF (1 card)	High Speed	--	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

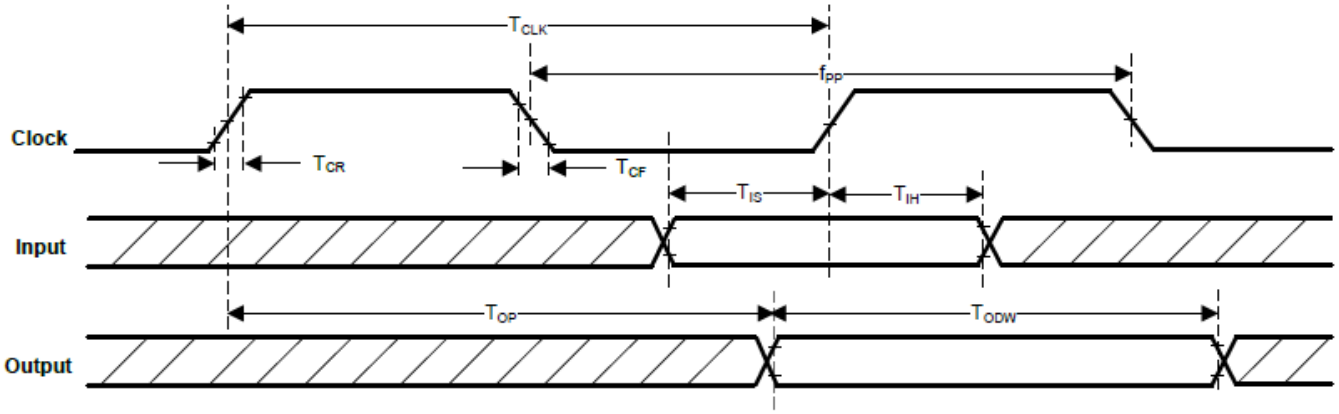


SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR ,TCF <2ns(max) at 100MHz CCARD =10pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output Delay Time CL ≦ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL =15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

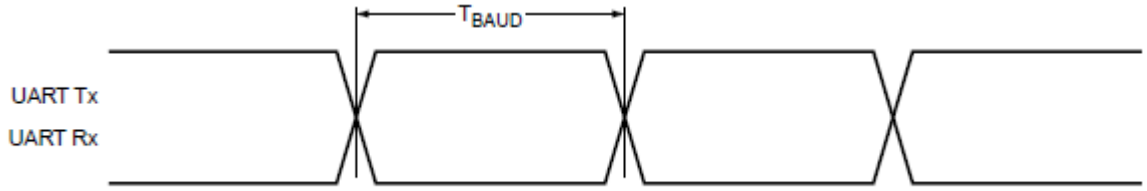
3.4.2.3 SDR104 mode (208MHz) (1.8V)



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR104	0	-	208	MHz
T_{CLK}	Clock Time	SDR104	4.8	-	-	ns
T_{IS}	Input Setup Time	SDR104	1.4	-	-	ns
T_{IH}	Input Hold Time	SDR104	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR,TCF<0.96ns(max) at 208MHz CCARD =10pF	SDR104	-	-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	-	-	ns

3.4.3.High-Speed UART Interface

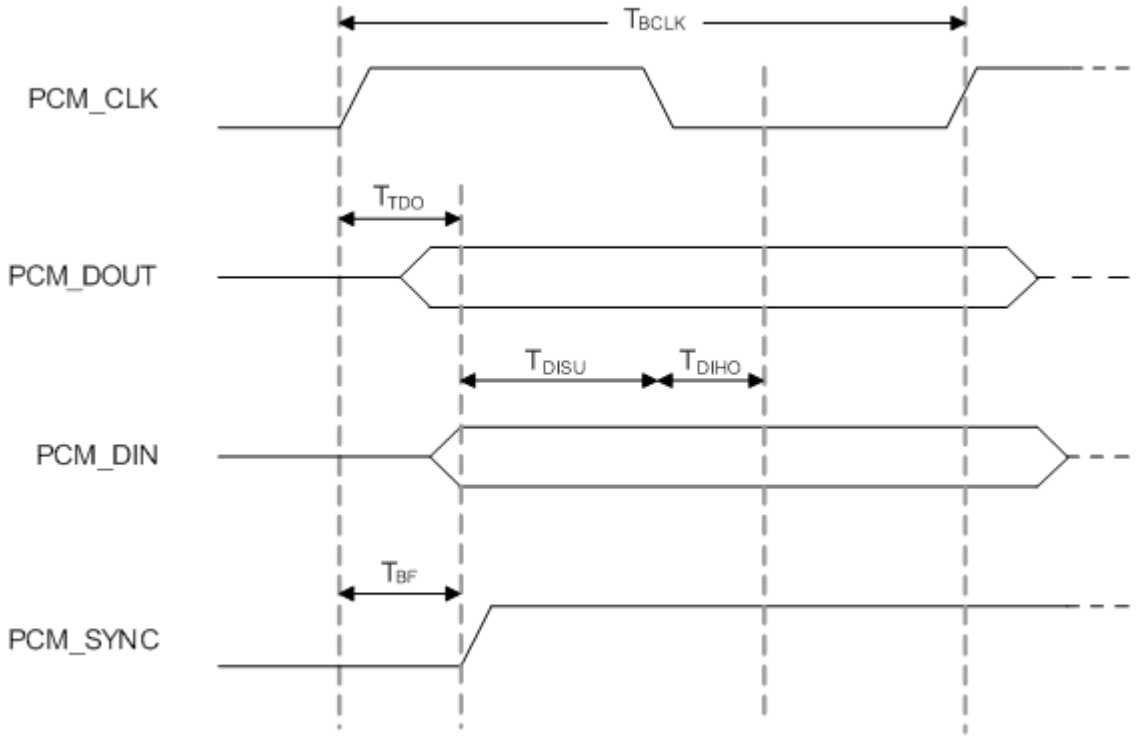
The AW-XM549 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz or 40MHz input clock	250	-	-	ns

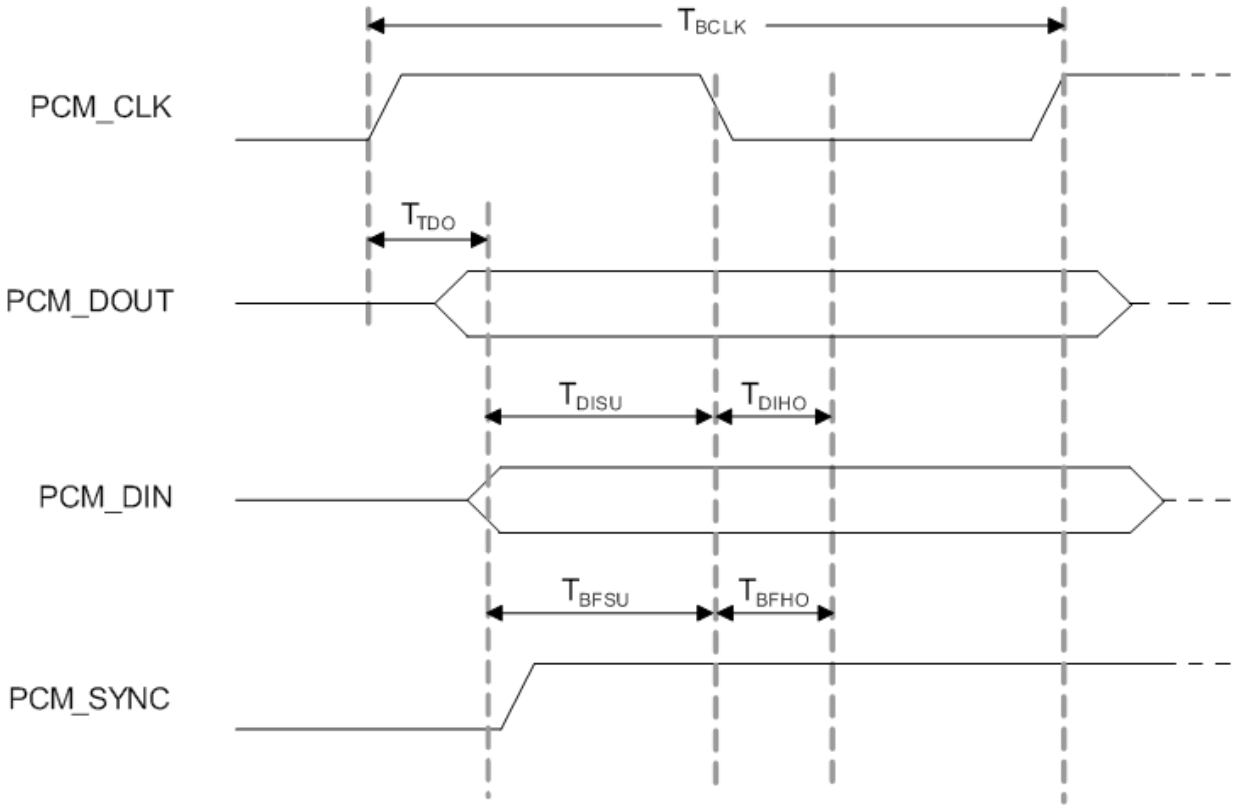
3.4.4 PCM Interface

3.4.4.1 PCM Timing Specification – Master Mode



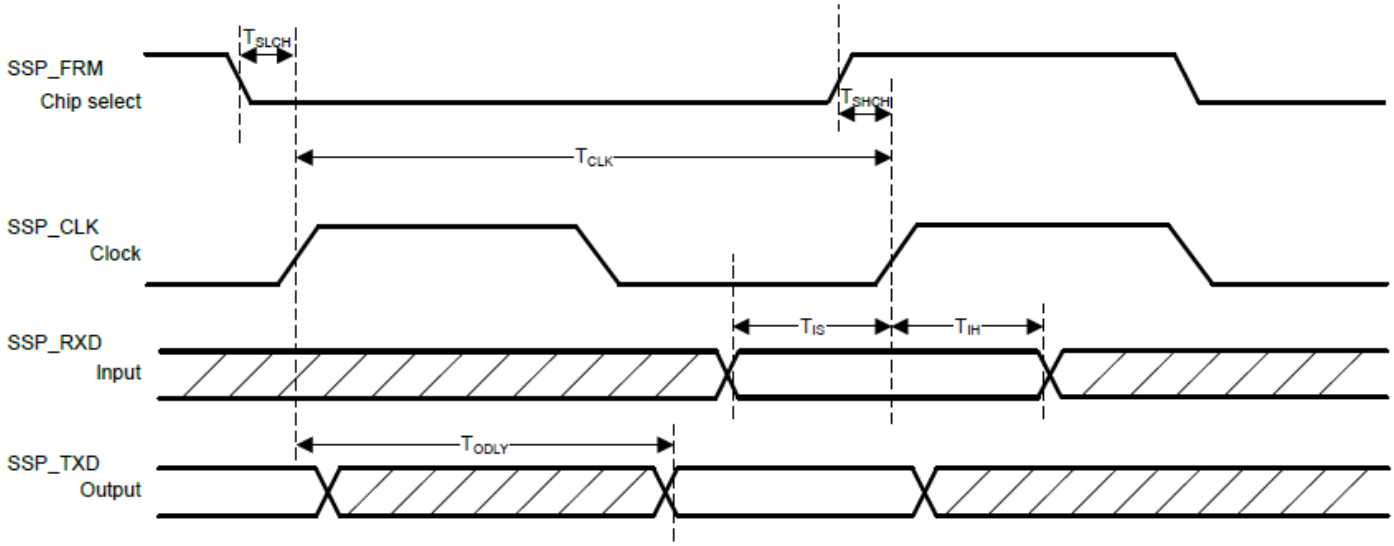
Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

3.4.4.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}			10		--	ns

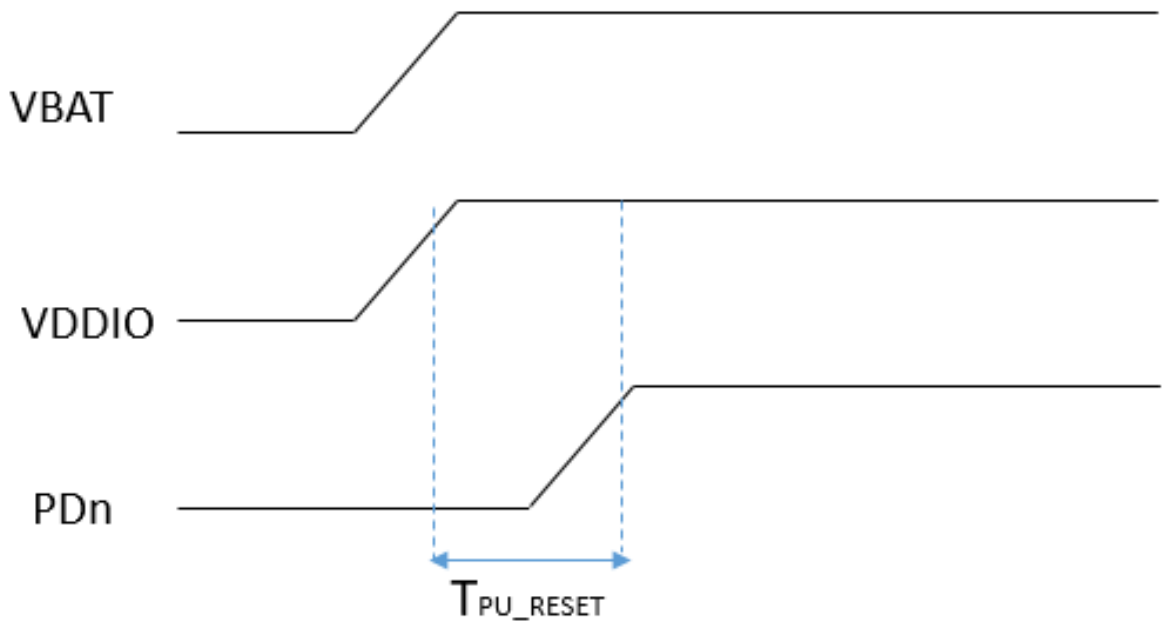
3.4.5 SPI Interface



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SLCH}	Chip select setup time	--	12	--	--	ns
T_{SHCH}	Chip select hold time	--	12	--	--	ns
T_{CLK}	Clock period	--	40	--	--	ns
T_{IS}	Input setup time	--	12	--	--	ns
T_{IH}	Input hold time	--	0	--	--	ns
T_{ODLY}	Output delay	--	--	--	12	ns

3.5 Timing Sequence

AW-XM549 power up timing sequence.



Symbol	Parameter	Min	Typ	Max	Units
TPU_RESET	Valid power to PDn deasserted	0	-	-	ms
VIH	Input high voltage	1.4	-	4.5	V
VIL	Input low voltage	-0.4	-	0.5	V

3.6 Power Consumption*

3.6.1 WLAN

No.	Item			JP1_PIN2 VBAT_3.3V (mA)		
				Max.	Avg.	
1	Pdn *(1)(2)			0.18	0.02	
2	Deepsleep*(2)(3)			0.4	0.3	
3	Power Save 2.4GHz (DTIM-1)*(2)(3)(4)			62	1.7	
4	Power Save 5GHz (DTIM-1)*(2)(3)(4)			69	1.1	
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit (mA)		
				Max.	Avg.	Duty Cycle Avg. (%)
2.4	11b@1Mbps	20	17	295	294	99
	11g@54Mbps	20	16	278	276	88
	11n@MCS0	40	14	271	269	96
	11n@MCS7	40	14	251	248	81
	11ax@MCS0 NSS1	40	12	258	255	96
	11ax@MCS11 NSS1	40	12	232	231	77
5	11a@6Mbps	20	16	410	404	98
	11n@MCS0	40	16	415	410	96
	11n@MCS7	40	16	375	369	80
	11ac@MSC0 NSS1	80	14	378	372	93
	11ac@MSC9 NSS1	80	14	332	328	72
	11ax@MSC0 NSS1	80	11	327	324	92
	11ax@MSC11 NSS1	80	11	296	294	76
Band (GHz)	Mode	BW(MHz)		Receive (mA)		
				Max.	Avg.	
2.4	11b@11Mbps	20		61	58	
	11n@MCS7	40		73	71	
	11ax@MCS11 NSS1	40		73	69	
5	11a@54Mbps	20		73	72	
	11n@MCS7	40		83	82	
	11ac@MCS9 NSS1	80		101	100	
	11ax@MCS11 NSS1	80		100	98	

No.	Item			JP4_PIN2 VIO_3.3V (uA)	
				Max.	Avg.
1	Pdn *(1)(2)			23	23
2	Deepsleep*(2)(3)			181	181
3	Power Save 2.4GHz (DTIM-1)*(2)(3)(4)			327	189
4	Power Save 5GHz (DTIM-1)*(2)(3)(4)			327	187
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit (uA)	
				Max.	Avg.
2.4	11b@1Mbps	20	17	480	479
	11ax@MCS11 NSS1	40	12	473	472
5	11a@6Mbps	20	16	498	496
	11ax@MSC11 NSS1	80	11	484	484
Band (GHz)	Mode	BW(MHz)		Receive (uA)	
				Max.	Avg.
2.4	11b@11Mbps	20		448	447
5	11ax@MCS11 NSS1	80		453	453

No.	Item			JP4_PIN2 VIO_1.8V (uA)	
				Max.	Avg.
1	Pdn *(1)(2)			2	2
2	Deepsleep*(2)(3)			61	61
3	Power Save 2.4GHz (DTIM-1)*(2)(3)(4)(5)			61	61
4	Power Save 5GHz (DTIM-1)*(2)(3)(4)(5)			61	61
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit (uA)	
				Max.	Avg.
2.4	11b@1Mbps	20	17	44	44
	11ax@MCS11 NSS1	40	12	44	44
5	11a@6Mbps	20	16	45	44
	11ax@MSC11 NSS1	80	11	45	44
Band (GHz)	Mode	BW(MHz)		Receive (uA)	
				Max.	Avg.
2.4	11b@11Mbps	20		44	44
5	11ax@MCS11 NSS1	80		44	44

3.6.2 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	JP1_PIN2 VBAT_3.3V (mA)	
				Max.	Avg.
1	Deepsleep*(1)	N/A		0.6	0.4
2	Transmit*(2)	DH5	2	53	36
3	Receive*(2)	DH5	N/A	53	31

No.	Mode	Packet Type	RF Power (dBm)	JP4_PIN2 VIO_3.3V (uA)	
				Max.	Avg.
1	Deepsleep*(1)	N/A		180	179
2	Transmit*(2)	DH5	2	437	436
3	Receive*(2)	DH5	N/A	437	436

No.	Mode	Packet Type	RF Power (dBm)	JP4_PIN2 VIO_1.8V (uA)	
				Max.	Avg.
1	Deepsleep*(1)	N/A		61	61
2	Transmit*(2)	DH5	2	43	42
3	Receive*(2)	DH5	N/A	43	42

3.6.3 802.15.4

No.	Mode	Modulation Type	RF Power (dBm)	JP1_PIN2 VBAT_3.3V (mA)	
				Max.	Avg.
1	Deepsleep*(1)(2)	N/A		0.3	0.13
2	Transmit*(3)(4)	O-QPSK	4	81	53
3	Receive*(3)(5)	O-QPSK	N/A	43	42

No.	Mode	Packet Type	RF Power (dBm)	JP4_PIN2 VIO_3.3V (uA)	
				Max.	Avg.
1	Deepsleep*(1)(2)	N/A		457	457
2	Transmit*(3)(4)	O-QPSK	4	571	570
3	Receive*(3)(5)	O-QPSK	N/A	571	570

No.	Mode	Packet Type	RF Power (dBm)	JP4_PIN2 VIO_1.8V (uA)	
				Max.	Avg.
1	Deepsleep*(1)(2)	N/A		118	118
2	Transmit*(3)(4)	O-QPSK	4	194	193
3	Receive*(3)(5)	O-QPSK	N/A	194	193

3.7 Sleep Clock (Optional)

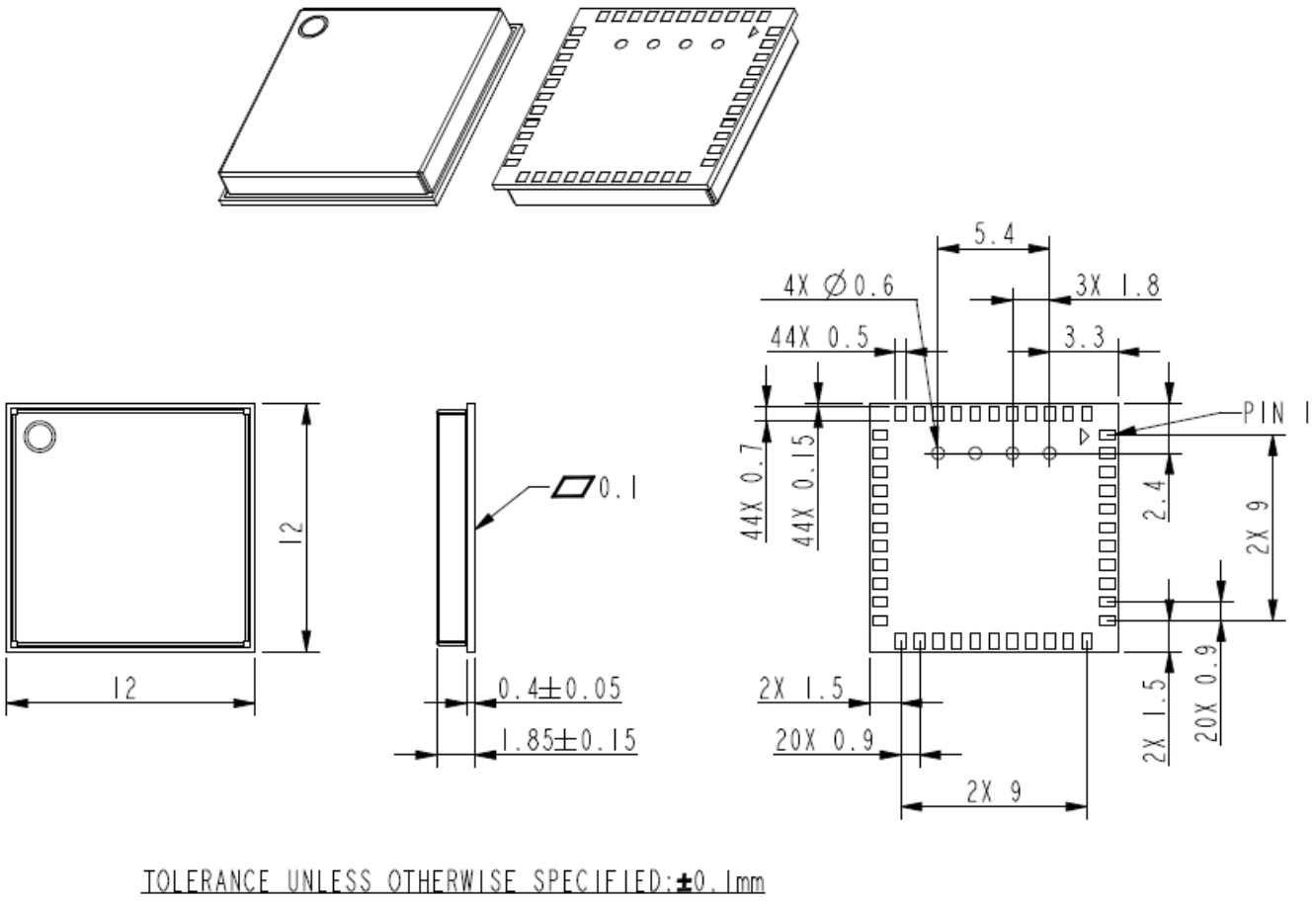
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock frequency range/ accuracy ■ CMOS input clock signal type ■ ±250 ppm (initial, aging, temperature)	-	32.768	-	kHz
PN	Phase noise requirement (@ 100KHz)	-	-125	-	dBc/Hz
J_C	Cycle jitter	-	1.5	-	ns (RMS)
SR	Slew rate limit (10-90%)	-	-	100	ns
DC	Duty cycle tolerance	20	-	80	%

4. Mechanical Information

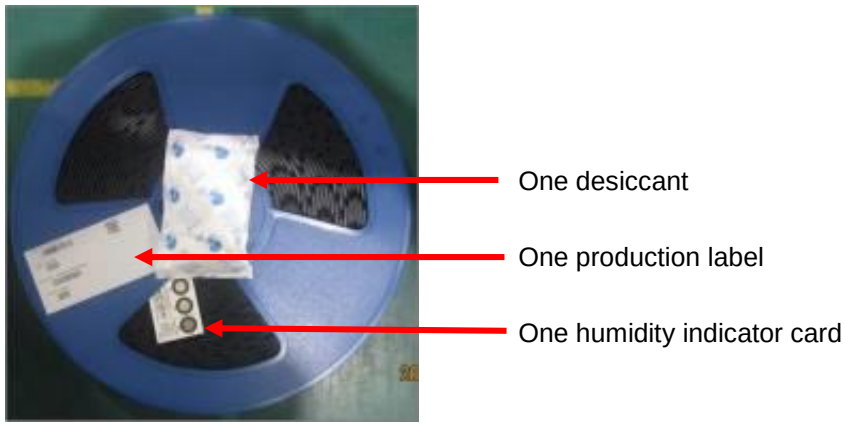
4.1 Mechanical Drawing



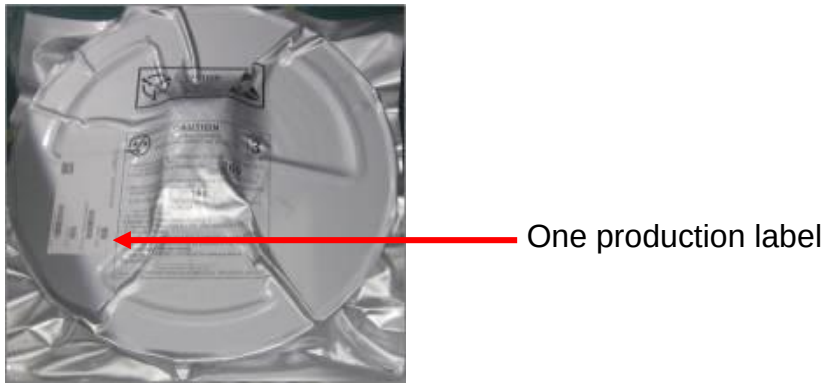
TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

5. Packing Information

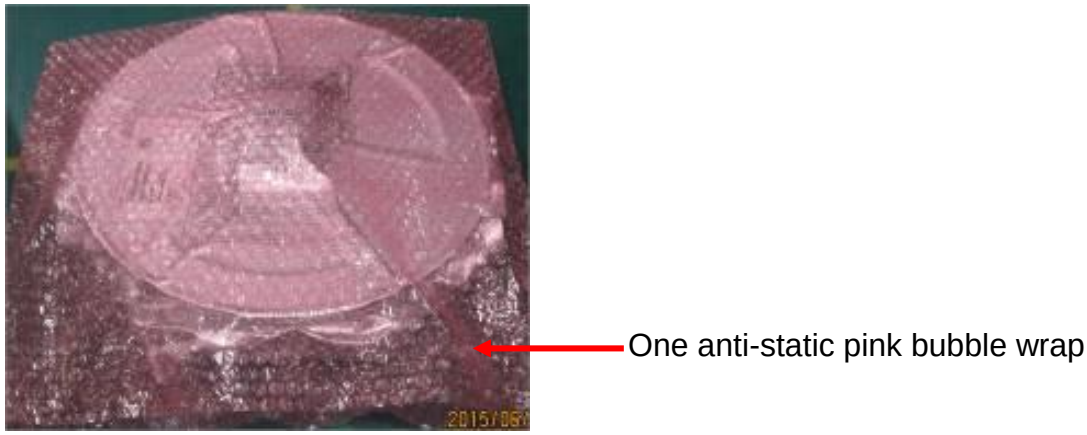
1. One reel can pack 1,500pcs 12x12 LGA modules
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



4. A bag is put into the anti-static pink bubble wrap



5. A bubble wrap is put into the inner box and then one label is pasted on the inner box

One production label

6. 5 inner boxes could be put into one carton

7. Sealing the carton by AzureWave tape

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton

One carton label
出貨標籤

One box label
箱號標籤