

AW-XM455

IEEE 802.11 2X2 WiFi 6 MIMO Wireless LAN + Bluetooth 5.1 Combo LGA Module

Datasheet

Rev. B

DF

For Standard

 1

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Features

WLAN

- Support 2x2 802.11 a/b/g/n/ac/ax
- Dual bands: 2.4 GHz and 5 GHz
- Support 20/40/80 MHz channel Bandwidths.
- 5GHz PHY data rates up to 1.2 Gbps
- 2.4 GHz PHY data rates up to 458 Mbps
- Uplink and downlink OFDMA and MU-MIMO
- Support DFS

Bluetooth

- Bluetooth 5.1
- Bluetooth class 2
- PCM interface for voice applications
- ♦ 2Mbit/s LE
- Long range
- LTE/MWS coexistence
- 2 x wide band speech (WBS) calls
- Security: AES



Revision History

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Version	Revision Date	DCN NO.	Description	Initials	Approved
Α	2020/05/26	DCN017597	Draft version	Renton Tao	N.C Chen
В	2021/02/08		 Update format Update features Update operating temperature Update pin map Update Host configuration table 	Renton Tao	N.C Chen



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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n/ac/ax Concurrent Dual WiFi(CDW) and BT, combo module – **AW-XM455.** With High Efficiency Wireless (HEW) and backward compatible with 802.11ac technologies integrated into a module, AW-XM455 provides the best and most convenient SMT process. The module is targeted to mobile devices including, Tablet PC, Portable Media Players (PMPs), Portable Navigation Devices (PNDs), Personal Digital Assistants (PDAs), Tracking Devices, Gaming Devices which need convenient SMT process, low power consumption.

By using AW-XM455, the customers can easily integrate the Wi-Fi, BT, by a combo module with the benefits of high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.

Compliance with the IEEE 802.11a/b/g/n/ac/ax standard, the AW-XM455 uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-XM455.

The AW-XM455 supports standard interface **PCIe for WLAN** interface connection, High-Speed **UART for BT** interface connection. AW-XM455 is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the AW-XM455 is the best solution for the consumer electronics and the tablet PC.



1.2 Block Diagram

A simplified block diagram of the AW-XM455 module is depicted in the figure below.



AW-XM455 Block Diagram



1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 2X2 WiFi 6 MIMO Wireless LAN + Bluetooth 5.1 Combo LGA Module
Major Chipset	NXP IW620P
Host Interface	 WiFi + BT PCIe + UART (For Host configuration interface, please refer to section 2.3)
Dimension	20 mm X 18 mm x 2.85 mm(Max) (Tolerance remarked in mechanical drawing)
Form factor	LGA module, 98 pins
Antenna	2T2R for WiFi, standalone antenna for BT ANT1(Main) : WiFi_A \rightarrow TX/RX ANT2(Aux) : WiFi_B \rightarrow TX/RX ANT3(BT): BT
Weight	TBD

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax 2T2R
WLAN VID/PID	
WLAN SVID/SPID	TBD
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-QAM
Number of Channels	 2.4GHz: USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11 China, Australia, Most European Countries - 1 ~ 13 Japan, 1 ~ 13 5GHz: USA, Canada, Most European Countries -

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	 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,13 6,140,149,153,157,161,165 Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,13 6,140 China - 36,40,44,48,52,56,60,64, 149,153,157,161,165 				
	2.4G	-			
		Min	Тур	Max	Unit
	11b (11Mbps) @EVM<35%		TBD		dBm
	11g (54Mbps) @EVM≦-27 dB		TBD		dBm
	11n (HT20 MCS7) @EVM≦-28 dB		TBD		dBm
	11n (HT40 MCS7) @EVM≦-28 dB		TBD		dBm
	11n (HE20 MCS11) @EVM≦-35 dB		TBD		dBm
	11n (HE40 MCS11) @EVM≦-35 dB		TBD		dBm
	5G				
		Min	Тур	Max	Unit
Output Power	11a (54Mbps) @EVM≦-27 dB		TBD		dBm
	11n (HT20 MCS7) @EVM≦-28 dB		TBD		dBm
	11n (HT40 MCS7) @EVM≦-28 dB		TBD		dBm
	11ac(VHT20 MCS8) @EVM≦-31 dB		TBD		dBm
	11ac(VHT40 MCS9) @EVM≤-32 dB		TBD		dBm
	11ac(VHT80 MCS9) @EVM≦-32 dB		TBD		dBm
	11ax(HE20 MCS11) @EVM≦-35 dB		TBD		dBm
	11ax(HE40 MCS11) @EVM≦-35 dB		TBD		dBm
	11ax(HE80 MCS11) @EVM≦-35 dB		TBD		dBm



	2.4G				
		Min	Тур	Max	Unit
	11b (11Mbps)	-	TBD		dBm
	11g (54Mbps)	-	TBD		dBm
	11n (HT20 MCS7)	-	TBD		dBm
	11n (HT40 MCS7)	-	TBD		dBm
	11ax(HE20 MCS11)		TBD		dBm
	11ax(HE40 MCS11)		TBD		dBm
Pacaivar Sansitivity	5G		-		
Receiver Sensitivity		Min	Тур	Max	Unit
	11a (54Mbps)	-	TBD		dBm
	11n (HT20 MCS7)	-	TBD		dBm
	11n (HT40 MCS7)	-	TBD		dBm
	11ac(VHT20 MCS8)	-	TBD		dBm
	11ac(VHT40 MCS9)		TBD		dBm
	11ac(VHT80 MCS9)		TBD		dBm
	11ax(HE20 MCS11)		TBD		dBm
	11ax(HE40 MCS11)		TBD		dBm
	11ax(HE80 MCS11)		TBD		dBm
Data Rate	 802.11b: 1, 2, 5.5, 11Mbps 802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: up to 150Mbps-single 802.11n: up to 300Mbps-2x2 MIMO 802.11ac:up to 192.6Mbps (20MHz channel) 802.11ac:up to 400Mbps (40MHz channel) 802.11ac:up to 866.7Mbps (80MHz channel) 802.11ax:2.4GHz up to 458Mbps, 5GHz up to 1.2Gbps 				
Security	WiFi: WPA/WPA3				

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth 5.1
Bluetooth VID/PID	N/A
Frequency Rage	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: π/4-DQPSK Payload 3M: 8DPSK

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		Min	Тур	Max	Unit
Output Bower	BDR		2		dBm
Output Power	EDR		2		dBm
	Low Energy (2MHz)		2		dBm
		Min	Тур	Max	Unit
Bossiver Sensitivity	BDR	Min	Тур	Max	Unit dBm
Receiver Sensitivity	BDR EDR	Min	Тур	Max	Unit dBm dBm
Receiver Sensitivity	BDR EDR Low Energy (2MHz)	Min	Тур	Max	Unit dBm dBm dBm

1.3.4 Operating Conditions

Features	Description			
Operating Conditions				
Voltage	3.3V+-5%			
Operating Temperature	-10 °C~ 85°C			
Operating Humidity	less than 85% R.H.			
Storage Temperature	-40 °C~ 85°C			
Storage Humidity	less than 60% R.H.			
ESD Protection				
Human Body Model	TBD			
Changed Device Model	TBD			



2.1 Pin Map

97	69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48	96
70		47
71		46
72		45
73		44
74		43
75		42
76		41
77		40
78	G1 G2 G3 G4 G5 G6	39
79		38
80	G7 G8 G9 G10 G11 G12	37
81	G13 G14 G15 G16 G17 G18	36
82		35
83		34
84	G25 G26 G27 G28 G29 G30	33
85	G31 G32 G33 G34 G35 G36	32
98		31
87		30
88	\bigcirc	29
89	<u> </u>	28
90		27
6		26
- 3		25
6		3 24
6	\bigtriangledown	2
98	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22	95

AW-XM455 Pin Map (Top View)



2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Туре
1	GPIO[5]	GPIO Mode: GPIO[5]	VDDIO	I/O
2	GPIO[4]	GPIO Mode: GPIO[4]	VDDIO	I/O
3	GPIO[3]	GPIO Mode: GPIO[3]	VDDIO	I/O
4	GND	Ground		
5	PCIE_RCLK_P	PCI Express Differential Clock Input—Positive	1V8	I
6	PCIE_RCLK_N	PCI Express Differential Clock Input—Negative	1V8	I
7	GND	Ground		
8	PCIE_TX_P	PCI Express Transmit Data—Positive	1V8	0
9	PCIE_TX_N	PCI Express Transmit Data—Negative	1V8	0
10	GND	Ground		
11	PCIE_RX_N	PCI Express Receive Data—Negative	1V8	I
12	PCIE_RX_P	PCI Express Receive Data—Positive	1V8	I
13	GND	Ground		
14	USB_DM	USB Serial Differential Data Minus	3V3	I/O
15	USB_DP	USB Serial Differential Data Plus	3V3	I/O
16	GND	Ground		
17	NC	NC		floating
18	NC	NC		floating
19	NC	NC		floating
20	NC	NC		floating
21	NC	NC		floating
22	NC	NC		floating
23	NC	NC		floating
24	GND	Ground		
25	PCIE_PERSTn	PCIe host indication to reset the device (active low)	VIO	
26	PCIE_CLKREQn	PCIe clock request (active low)	VIO	I/O
27	PCIE_WAKEn	PCIe wake signal (active low)	VIO	I/O
28	NC	NC		floating
29	GND	Ground		
30	UART_RTSn	UART Mode: UART_RTSn (active low)	VDDIO	0
31	UART_CTSn	UART Mode: UART_CTSn (active low)	VDDIO	
32	UART_RX	UART SIN pin	VDDIO	
33	UART_TX	UART SOUT.pin	VDDIO	0
34	NC	NC		floating
35	NC	NC		floating
36	NC	NC		floating
37	NC	NC		floating
38	NC	NC		floating
39	NC	NC		floating
40	NC	NC		floating
41	NC	NC		floating

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42	NC	NC		floating
43	NC	NC		floating
44	NC	NC		floating
45	NC	NC		floating
46	NC	NC		floating
47	NC	NC		floating
48	BT_ANT	RF I/O pad for BT		I/O
49	GND	Ground		
50	GND	Ground		
51	GND	Ground		
52	WLAN_ANT_2	RF I/O pad for WLAN ANT 2		I/O
53	GND	Ground		
54	GND	Ground		
55	GND	Ground		
56	GND	Ground		
57	GND	Ground		
58	GND	Ground		
59	GND	Ground		
60	GND	Ground		
61	GND	Ground		
62	GND	Ground		
63	GND	Ground		
64	GND	Ground		
65	GND	Ground		
66	GND	Ground		
67	GND	Ground		
68	GND	Ground		
69	WLAN_ANT_1	RF I/O pad for WLAN ANT 1		I/O
70	3V3	3.3V DC power supply	3.3V	
71	3V3	3.3V DC power supply	3.3V	
72	GND	Ground		
73	CON[0]	Firmware Boot Options. See below table*	VIO	
74	CON[1]	Firmware Boot Options. See below table*	VIO	I
75	CON[2]	Firmware Boot Options. See below table*	VIO	I
76	NC	NC		floating
77	NC	NC		floating
78	NC	NC		floating
79	NC	NC		floating
80	NC	NC		floating
81	NC	NC		floating
82	NC	NC		floating
83	GND	Ground		
84	PDn	Full Power-down input pin (active low) 0 = full power-down mode	3V3	I
L				

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		1 = normal mode		
85	GPIO[2]	GPIO Mode: GPIO[2]	VDDIO	I/O
86	GPIO[21]	GPIO Mode: GPIO[21]	VDDIO	I/O
87	GPIO[13]	GPIO Mode: GPIO[13]	VDDIO	I/O
88	GPIO[5]	GPIO Mode: GPIO[5]	VDDIO	I/O
89	GPIO[7]	GPIO Mode: GPIO[7]	VDDIO	I/O
90	VIO	Digital I/O power supply	1.8 or 3.3V	I
91	GND	Ground		
92	1V8	1.8V DC power supply	1.8V	I
93	1V8	1.8V DC power supply	1.8V	I
94	GPIO[6]	GPIO Mode: GPIO[6]	VDDIO	I/O
95	GND	Ground		
96	GND	Ground		
97	GND	Ground		
98	GND	Ground		
G1~36	GND	Ground		

2.3 Host Configuration Interface Table

Strap Value	WLAN	Bluetooth/LE
011	PCle	UART
others	reserved	reserved
	-	

*Firmware Boot options



3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3V3	DC supply for the 3.3V input	-	3.3	3.63	V
VIO	I/O power supply	-	3.3	3.63	V
		-	1.8	1.98	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3V3	DC supply for the 3.3V input	3.14	3.3	3.46	V
VIO	I/O power supply	3.14	3.3	3.46	V
		1.71	1.8	1.89	V

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8/3.3V Operation (VIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Vін	Input high voltage	0.7*VIO	-	VIO+0.4	
VIL	Input low voltage	-0.4	-	0.3*VIO	
Vон	Output high voltage	VIO-0.4	-	-	V
Vol	Output low voltage	-	-	0.4	
VHYS	Input Hysteresis	100			



3.4 Host Interface

3.4.1 PCI Express Interface

3.4.1.1 Differential Tx Output Electricals

Sy mbol	Paramete r		Тур	Max	Unit s
UI	Unit interval Each UI is 400 ps ±300 PPM. UI does not account for SSC dictated variations.		400	400.12	ps
V _{Tx_DIFFpp}	Differential peak-to-peak output voltage V _{Tx_DIFFpp} = 2* V _{TX-D+} - V _{TX-D} -	0.800		1.2	V
VTx_DE_RATIO	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	db
T _{Rx_EYE}	Minimum Tx eye wid th	0.75			UI
T _{RX_EYE_MEDIAN_} MAX_JIT	Maximum time between jitter median and maximum deviation from median			0.125	UI
T _{Tx_RISE} , T _{Tx_FALL}	D+/D- Tx output rise/fall time	0.125			UI
V _{Tx_CM_DC_ACTIV} E_IDLE_DELTA	Absolute delta of DC common mode voltage during L0 and electrical idle	0-	-	100	mV
VTX_CM_DC_LINE_ DE LTA	Absolute delta of DC common mode voltage between D+ and D-	0-	-	25	mV
VTx_IDLE_D IFF p	Electrical idle differential peak output voltage	0		20	mV
VTx_RCV_DETECT	Voltage change allowed during receiver detection			600	mV
V _{Tx_DC_CM}	TxDC common mode voltage			3.6	V
ITx_SHORT	Tx short circuit current limit			90	mA
T _{Tx_IDLE_MIN}	Minimum time spent in electrical idle	50			UI
T _{Tx_IDLE_SET_TO_}	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI
T _{Tx_IDLE_TO_DIFF_} DATA	Maximum time to transition to valid Tx specifications after leaving an electrical idle condition			20	UI
RL _{Tx_DIFF}	Differential return loss	10			dB
RL _{Tx_CM}	Common mode return loss	6			dB
C _{Tx}	AC coupling capacitor	75		200	nF
T _{Crosstalk}	Crosstalk random timeout	0		1	ms



3.4.1.2 Differential Rx input Electricals

Sy m bol	Paramet er		Тур	Max	Unit s
UI	Unit interval Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.		400	400.12	ps
V _{Rx_DIFFpp}	Differential peak-to-peak voltage V _{Rx_DIFFpp} = 2* V _{RX-D+} - V _{RX-D-}			1.2	V
T _{Rx_EYE}	Minimum receiver eye width	0.4			UI
T _{Rx_EYE_MEDIAN_MAX_} JIT	Maximum time between jitter median and maximum deviation from median			0.3	UI
V _{Rx_CM_ACp}	AC peak common mode input voltage			150	mV
RL _{Rx_DIFF}	Differential return loss	10			dB
RL _{Rx_CM}	Common mode return loss	6			dB
Z _{Rx_DIFF_DC}	DC differential input impedance	80	100	120	Ω
Z _{Rx_DC}	DC input impedance	40	50	60	Ω
Z _{Rx_HIGH_IMP_DC_POS}	Powered down DC input impedance positive	50			k
Z _{Rx_HIGH_IMP_DC_NEG}	Powered down DC input impedance negative	1			kΩ
V _{Rx_IDLE_DET_} DIFFpp	Electrical idle detect threshold	65		175	mV
T _{Rx_IDLE_DET_} DIFF_ENTERTIME	Unexpected electrical idle enter detect threshold integration time			10	ms
L _{Rx_SKEW}	Total skew		-2	0	ns



3.4.2 USB Interface



3.4.2.1 USB LS Driver and Receiver Parameters

BRBaud rate-1.5-MbpsBRppmBaud rate tolerance-15000-15000ppmDriver specificationsVoHOutput single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.2.8-3.6VVoLOutput single ended low Defined with 1.425 kΩ pull-down resistor to ground.0-0.3VVcRsOutput single crossover voltage1.3-2.0VTLRData rise time to fall time.75-300nsTLRFData fall time for fall time.75-300nsTLRFMRise and fall time matching to Juli80-125%TUDJ1Source jitter total: to next transition including frequency tolerance. Timing difference between-95-95ns
BRppmBaud rate tolerance-15000-15000ppmDriver specificationsVoHOutput single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.2.8-3.6VVoLOutput single ended low Defined with 1.425 kΩ pull-down resistor to ground.0-0.3VVcRsOutput single crossover voltage1.3-2.0VTLRData rise time for fall time.75-300nsTLFData fall time for fall time.75-300nsTLRFMRise and fall time matching v Including frequency tolerance. Timing difference between-125%
Driver specificationsVOHOutput single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.2.8-3.6VVoLOutput single ended low Defined with 1.425 kΩ pull-down resistor to ground.0-0.3VVcRsOutput single crossover voltage1.3-2.0VTLRData rise time for fall time.75-300nsTLFData fall time for fall time.75-300nsTLRFMRise and fall time matching for fall time.80-125%TUDJ1Source jitter total: to next transition including frequency tolerance. Timing difference between-95ns
VoHOutput single ended high Defined with 1.425 k Ω pull-up resistor to 3.6V.2.8-3.6VVoLOutput single ended low Defined with 1.425 k Ω pull-down resistor to ground.0-0.3VVcRsOutput single crossover voltage1.3-2.0VTLRData rise time for fall time.75-300nsTLFData fall time for fall time.75-300nsTLRMRise and fall time matching for fall time.80-125%TUDJ1Source jitter total: to next transition including frequency tolerance. Timing difference between-95ns
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3.6V.0-0.3VVoLOutput single ended low Defined with 1.425 k Ω pull-down resistor to ground.0-0.3VVcRsOutput single crossover voltage1.3-2.0VTLRData rise time for fall time.75-300nsTLFData fall time for fall time.75-300nsTLRFMRise and fall time matching for fall time.80-125%TUDJ1Source jitter total: to next transition including frequency tolerance. Timing difference between-95ns
VoLOutput single ended low Defined with 1.425 k Ω pull-down resistor to ground.0-0.3VVcrsOutput single crossover voltage1.3-2.0VTLRData rise time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300nsTLFData fall time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300nsTLFData fall time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300nsTLRFMRise and fall time matching • Including frequency tolerance. Timing difference between-95ns
Defined with 1.425 kΩ pull-down resistor to ground.Image: constant of the second sec
ground.Image: construction of the second
VCRSOutput single crossover voltage1.3-2.0VTLRData rise time75-300ns• Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300nsTLFData fall time75-300ns• Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300nsTLRFMRise and fall time matching80-125%TUDJ1Source jitter total: to next transition • Including frequency tolerance. Timing difference between-95ns
TLRData rise time75-300ns• Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300nsTLFData fall time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300ns• Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300ns• Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300ns• Defined from 10% to 90% for rise time and 90% to 10% for fall time.80-125%TLRFMRise and fall time matching • Source jitter total: to next transition • Including frequency tolerance. Timing difference between-95-95ns
• Defined from 10% to 90% for rise time and 90% to 10% for fall time. -
for fall time.75-300nsTLFData fall time · Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300nsTLRFMRise and fall time matching · UDJ180-125%TUDJ1Source jitter total: to next transition · Including frequency tolerance. Timing difference between-95-95ns
TLFData fall time • Defined from 10% to 90% for rise time and 90% to 10% for fall time.75-300nsTLRFMRise and fall time matching80-125%TUDJ1Source jitter total: to next transition • Including frequency tolerance. Timing difference between-95-95ns
• Defined from 10% to 90% for rise time and 90% to 10% for fall time. -
for fall time. 80 125 % TLRFM Rise and fall time matching 80 - 125 % TUDJ1 Source jitter total: to next transition -95 - 95 ns • Including frequency tolerance. Timing difference between - 95 ns
I LRFMRise and fall time matching80-125%TUDJ1Source jitter total: to next transition • Including frequency tolerance. Timing difference between-95-95ns
I UDJ1 Source jitter total: to next transition -95 - 95 ns • Including frequency tolerance. Timing difference between • • 95 • 95 •
Including frequency tolerance. Timing difference between
the differential data signals.
Defined at crossover point of differential data signals.
TUDJ2 Source jitter total: for paired transitions -150 - 150 ns
Including frequency tolerance. Timing difference between
the differential data signals.
Denned at crossover point of differential data signals.
Receiver specifications Very
VIH Input single ended low
$V_{\rm L}$ Input single ended low0.8V $V_{\rm ex}$ Differential input consitivity0.2V

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3.4.4.2 USB FS Driver and Receiver Parameters

Symbol	Parameter	Min	Тур	Max	Units
BR	Baud rate	-	12	-	Mbps
BR _{ppm}	Baud rate tolerance	-2500	-	2500	ppm
Driver specif	ications				
Vон	Output single ended high	2.8	-	3.6	V
	Defined with 1.425 k Ω pull-up resistor to				
	3.6V.				
Vol	Output single ended low	0	-	0.3	V
	Defined with 1.425 k Ω pull-down resistor to				
	ground.				
VCRS	Output single crossover voltage	1.3	-	2.0	V
TFF	Data fall time	-4	-	20	ns
	• Defined from 10% to 90% for rise time and 90% to 10%				
	for fall time.				
T _{FR}	Data rise time	-4	-	20	ns
	Defined from 10% to 90% for rise time and 90% to 10%				
- -	for fall time.	0.5		0.5	
I DJ1	Source jitter total: to next transition	-3.5	-	3.5	ns
	Including frequency tolerance. Timing difference between				
	the differential data signals.				
Taua	Source jitter total: for paired transitions	1		1	20
T DJ2		-4	-	4	115
	Including frequency tolerance. Timing difference between the differential data signals				
	Defined at crossover point of differential data signals				
	Source litter for differential transition to SE0	-2		5	ns
TIDEOF	transition	-		Ŭ	110
	Defined at crossover point of differential data				
	signals.				
Receiver spe	cifications				
Vih	Input single ended high	2.0	-	-	V
VIL	Input single ended low	-	-	0.8	V
VDI	Differential input sensitivity	0.2	-	-	V
T _{JR1}	Receiver jitter: to next transition	-18.5	-	18.5	ns
	Defined at crossover point of differential data				
	signals.				
T _{JR2}	Receiver jitter: for paired transitions	-9	-	9	ns
	Defined at crossover point of differential data				
	signals.				



3.4.4.3 USB HS Driver and Receiver Parameters

Symbol	Parameter	Min	Тур	Max	Units	
BR	Baud rate	-	480	-	Mbps	
BR _{ppm}	Baud rate tolerance	-500	-	500	ppm	
Driver specifi	ications					
V _{HSOH}	Data signaling high	360	-	440	mV	
VHSOL	Data signaling low	-10	-	10	mV	
T _{HSR}	Data rise time	500	-	-	ns	
	• Defined from 10% to 90% for rise time and 90% to 10%					
	for fall time.					
THSF	Data fall time	-500	-	-	ns	
	Defined from 10% to 90% for rise time and 90% to 10%					
	for fall time.					
	Source jitter	-	-	-	-	
	See below figure					
Receiver specifications						
	Differential input signaling levels	-	-	-	-	
	See below figure					
VHSCM	Input single ended low	-50	-	500	mV	
	Receiver jitter tolerance	-	-	-	-	
	See below figure					



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USB HS Rx Eye Diagram Pattern Template Diagram

3.4.5. High-Speed UART Interface

The AW-XM455 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Тур	Max	Units
TBAUD	Baud rate	26MHz input clock	250	-	-	ns

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3.4.6 PCM Interface

3.4.6.1 PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Тур	Max	Units
FBCLK				2/2.048		MHz
Duty CycleBCLK			0.4	0.5	0.6	
TBCLK rise/fall				3		ns
T _{DO}					15	ns
TDISU			20			ns
Тыно			15			ns
T _{BF}					15	ns



3.4.6.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Тур	Max	Units
FBCLK				2/2.048		MHz
Duty Cycle _{BCLK}			0.4	0.5	0.6	
TBCLK rise/fall				3		ns
T _{DO}					30	ns
TDISU			15			ns
Тыно			10			ns
TBFSU			15			ns
Твғно			10			ns

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3.5 Timing Sequence

AW-XM455 power up timing sequence.

TBD

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3.6 Power Consumption*

3.6.1 WLAN

TBD

3.6.2 Bluetooth

TBD

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4. Mechanical Information

4.1 Mechanical Drawing





5. Packing Information

- 1. One reel can pack 650pcs AW-XM455 LGA modules
- 2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



4. A bag is put into the anti-static pink bubble wrap



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5. A bubble wrap is put into the inner box and then one label is pasted on the inner box



6. 4 inner boxes could be put into one carton



7. Sealing the carton by AzureWave tape



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8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton



Example of carton label (出貨標籤的範例)	AzureWave Technologies Inc.				
	AzureWave P/N				
	Customer	由業務提供			
	Customer P/N	由業務提供			
	Customer PO	由業務提供			
	Description	AW-XXXXXX			
	ΩΤΥ	1200 pcs			
	C/N				
	N.W.	G.W.			
	RoHs				
Example of box label (箱號標籤)	BOX0012018				
Example of production label (生產標籤)	P/N:				
	BAG SEAL DATE:				

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