AW-PU580

Wireless SMARC2.1 SoM

Datasheet

Rev. D

DF

(For Standard)

Features

Arm Cortex-A53 MPCore platform

- 32 KB L1 Instruction Cache
- 32 KB L1 Data Cache
- 512 KB unified L2 cache
- Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture
- Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
- Support of 64-bit Armv8-A architecture

Arm Cortex-M7 core platform

- Low power operation
- Real-time processing
- 32 KB L1 Instruction Cache
- 32 KB L1 Data Cache
- 256 KB tightly coupled memory (TCM)

Image Sensor Processor (ISP)

- 375 Mpixel/s HDR ISP supporting configurations, such as 12MP@30fps, 4kp45, or 2x 1080p80

On board memory

- Ram : up to 6GB(48Gb) 32bit LPDDR4-4000 (support Inline ECC)
- Flash :16GB(128Gb) eMMC 5.1 (Optional)

Graphic Processing Unit

- GC7000UL with OpenCL and Vulkan support
- 2 shader
- 166 million triangles/sec
- 1.0 giga pixel/sec
- 16 GFLOPs 32-bit
- Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL 1.2, Vulkan
- Core clock frequency of 1000 MHz
- Shader clock frequency of 1000 MHz
- GC520L for 2D acceleration

Video Processing Unit

- 1080p60 VP9 Profile 0, 2 (10-bit)
- 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) decoder
- 1080p60 AVC/H.264 Baseline, Main, High decoder
- 1080p60 VP8 decoder
- 1080p60 AVC/H.264 encoder
- 1080p60 HEVC/H.265 encoder

Neutral Processing Unit (NPU)

- 2.3 TOP/s Neural Network performance

HDMI 2.0a Tx

- Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30
- Pixel clock up to 297 MHz

LCDIF Display Controller

- Support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 1x 1080p60 + 2x 720p60 if all 3 instances used simultaneously (one LCDIF drives MIPI DSI, one LCDIF drives LVDS Tx and one LCDIF drives HDMI Tx)

MIPI Interface

- 4-lane MIPI CSI interface
- 4-lane MIPI DSI interface

Audio

- S/PDIF input and output, including a new Raw Capture input mode
- Support I2S interface

Connectivity

- 1x USB 3.0(or 1x USB 2.0 OTG) and 4x USB 2.0 One Ultra Secure Digital Host Controller (uSDHC) interface.
- SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100MB/sec. Also support for SDXC (extended capacity)
- Two Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588.
- Three Universal Asynchronous Receiver / Transmitter (UART) modules.
- Four I2C modules.
- One ECSPI modules
- Two Controller Area Network (FlexCAN) modules, each optionally supporting flexible data-rate (FD)

Security

- Resource Domain Controller (RDC)
- Cortex®-A53 MPCore TrustZone® support
- On-chip RAM (OCRAM) secure region protection using OCRAM controller
- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance Module (CAAM)
- Secure Non-Volatile Storage (SNVS)
- Optional Trust Platform Module (TPM 2.0)

WLAN + Bluetooth

- Wi-Fi 802.11 a/b/g/n/ac 2x2 (Wi-Fi 5)
- 2.4GHz and 5GHz Dual-Band
- Up to 866Mbps
- 20/40/80MHz channel bandwidth
- Bluetooth 5.3 (BR/ EDR/LE)

Revision History

Document NO: R2-3580-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/12/23	DCN019724	● Draft version	Steven Jian	Chihhao Liao
B	2021/04/15	DCN021212	● Removed SER0 & PCIE_A ● Updated 1.2 Block Diagram ● Updated 2.2.1 Module Pin Table ● Added 3.5 Boot mode configuration ● Changed document format ● Updated 1.3.1 General ● Updated 1.3.2 Operating Conditions ● Updated 4.1 Mechanical Drawing	Steven Jian	Chihhao Liao
C	2023/02/08	DCN028617	● Updated P134 P135 P140 P141 S4 P62 P67 P71 P74 P76 pin description ● Updated 2.2.2 CSI Feature Connector Pin Table (optional) ● Updated 1.2 Block Diagram ● Support Bluetooth 5.3 ● Added I2C pull-ups info in 2.2.1 Module Pin Table ● Remove Wi-Fi BT Specs in 1.3 Specifications Table ● Updated 3.6 Power Consumption, 2.1 Pin Map, 4. Mechanical Information ● Added 1.1.1 Ordering Information	Steven Jian	Chihhao Liao
D	2023/04/18	DCN029047	● Updated 1.1.1 Ordering Information ● Updated 1.2 Block Diagram ● Updated Ethernet and weight in 1.3.1 General ● Updated CSI description in 2.1 Pin Map and 2.2.2 CSI Feature Connector Pin Table (optional) ● Updated footnotes of Table 10 Master mode SAI timing (50 MHz)Table 12 Slave mode SAI timing (50 MHz)	Steven Jian	Chihhao Liao

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the System on Module with SMARC (“Smart Mobility ARChitecture”) 2.1 short size form factor & pin definition--- AW-PU580. By using AW-PU580, the customers can easily enable smart city, smart home, smart world and industrial IoT applications with the benefits of high design flexibility, short development cycle, and quick time-to-market.

The main system CPU shines in machine learning, vision, advanced multimedia and industrial IoT applications. The Neural Processing Unit (NPU) with 2.3 TOPS computing performance delivers substantially higher performance for Machine Learning tasks at nodes that removes cloud dependency and preserves individual privacy while providing a superior user experience. The integrated Image Signal Processor (ISP) brings real-time image processing to high-definition video and performs algorithms that extract the maximum image details in high-contrast scenes. The state-of-the-art Video Processing Unit (VPU), Graphics Processing Unit (GPU) and HIFi4 DSP enhance the multimedia experience. A dual gigabit Ethernet, one supporting Time-sensitive networking (TSN) provides control loops with highly precise timing. The CPU includes error correction code (ECC) in critical points of the system, including the DDR interface, for high system and security reliability and the required safety industrial level certification (SIL). Security protection features such as secure boot, encrypted boot, hardware firewall and run-time integrity checker (RTIC) support the prevention of multiple security attacks.

AW-PU580 adopts NXP’s latest highly-integrated dual-band WLAN & Bluetooth SoC---88W8997. It supports IEEE 802.11ac/a/b/g/n 2X2 MU-MIMO WLAN and Bluetooth 5.3 (Core Standard) + Bluetooth 2.1+Enhanced Data Rate (EDR). With multiple wired and wireless interfaces, the AW-PU580 enables ubiquitous connectivity effortlessly.

1.1.1 Ordering Information

Planned versions:

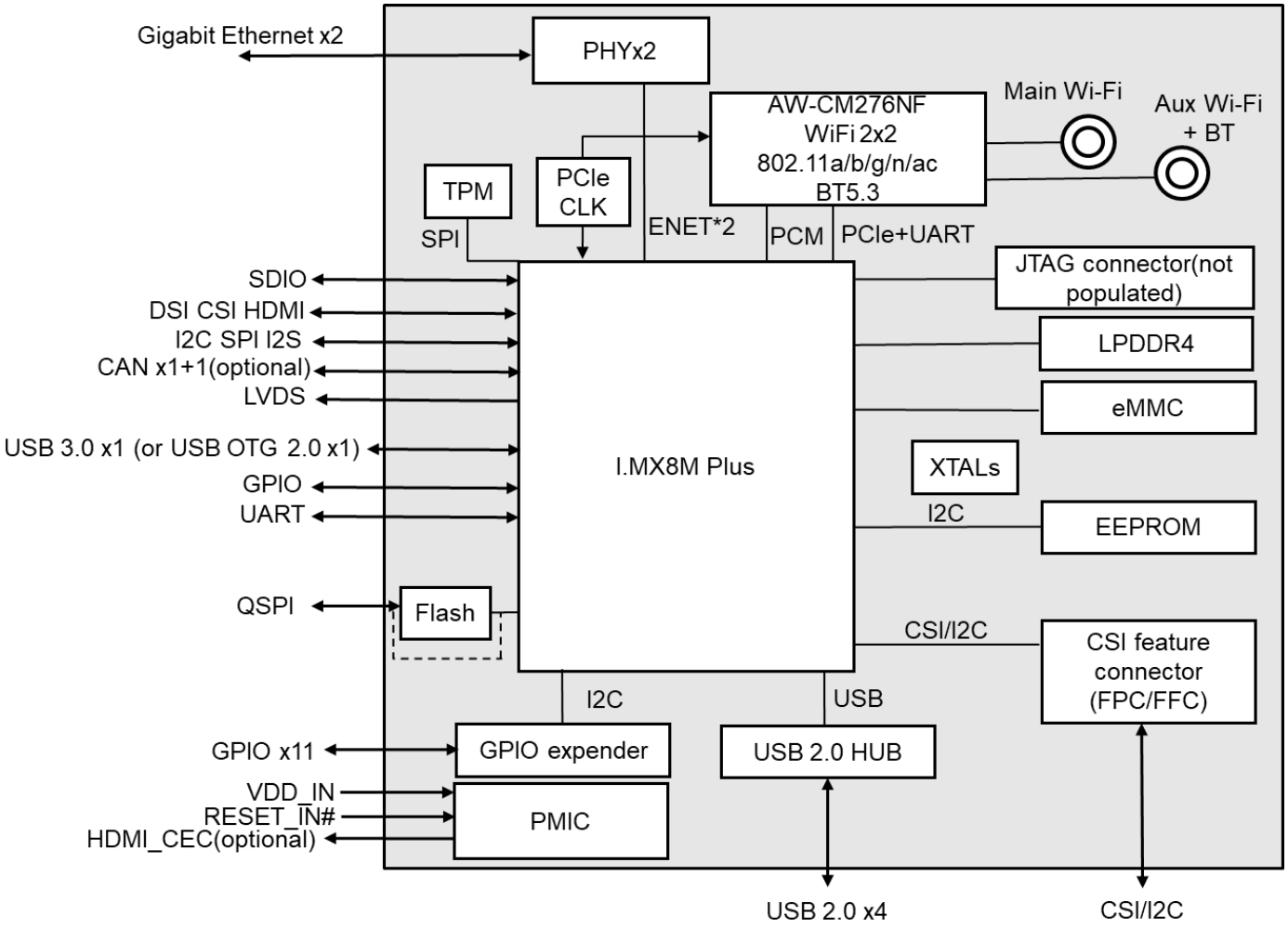
Model Name	Part Number of Main Chip	RAM Size	eMMC Size	Part Differentiator
AW-PU580-8CA-416AA2WWI	MIMX8ML8CVNKZAB 1.6GHz Industrial	LPDDR4 4GB	16GB	32MB NOR Flash, w/ WIFI, Ethernet x2, w/ TPM, w/ USB HUB, -40° ~85°
AW-PU580-8CA-4NAXX1XXC	MIMX8ML8CVNKZAB 1.6GHz Industrial	LPDDR4 4GB	N/A	w/o NOR Flash, w/o WIFI, Ethernet x1, w/o TPM, w/o USB HUB, 0° ~60°

AW-PU580 Option P/N

AW	-	PU580	-	8CA	-	4	16	A	A	2	W	W	I
AW	-	PU580	-	8CA	-	4	NA	X	X	1	X	X	C

AzureWave Module
Model Name
Chip Version 8CA(8ML8CVNKZAB)
DDR Memory : 4(4GB)
EMMC Memory: NA, 16(16GB)
NOR Flash X(n/a), A(32MB),
WIFI: X(n/a), A(2276NF)
Ethernet: X(n/a), 1(x1), 2(x2)
TPM: X(n/a), W(w/TPM)
USB Hub: X(n/a), W (w/usb hub)
Temperature: C(0~60), I(-40~85)

1.2 Block Diagram



**Support different HW configurations. Please contact Azurewave for the details.*

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	Wireless SMARC2.1 SoM
Major Chipset	NXP i.MX 8M Plus
CPU Speed (frequency)	Up to 1.8GHz
Wireless Connectivity	● Use the AW-CM267NF module* ● IEEE 802.11a/b/g/n/ac Wireless LAN 2T2R and Bluetooth 5.3 ● RF Connector: I-PEX MHF4 Connector Receptacle (20449)
USB	USB 3.0 x1(or USB 2.0 OTG x1) + USB2.0 x4
uSDHC	x1 Ultra Secure Digital Host Controller (uSDHC) interfaces
Ethernet	x2 Gigabit Ethernet controller: - GBE1 support Energy Efficient Ethernet (EEE),Ethernet AVB, and IEEE 1588 - GBE0 support TSN in addition to EEE, Ethernet AVB, and IEEE 1588
MIPI Interface	● 4-lane MIPI CSI interface ● 4-lane MIPI DSI interface
UART	UART 4wire up to 1x + UART 2wire*2
ECSPI	x1 ECSPI modules
I²C	x5 I²C modules
Audio Interface	● HDMI eARC ● x2 I2S interfaces
Ram	Up to 6GB(48Gb) 32bit LPDDR4-4000(support Inline ECC)
Flash	16GB(128Gb) eMMC 5.1 (Option)
Dimension	82mm x 50mm x 5.1mm
Form factor	SMARC 2.1 short size
Weight	18.7 g

*Note: For the detail, please refer to the data sheet of AW-CM276NF

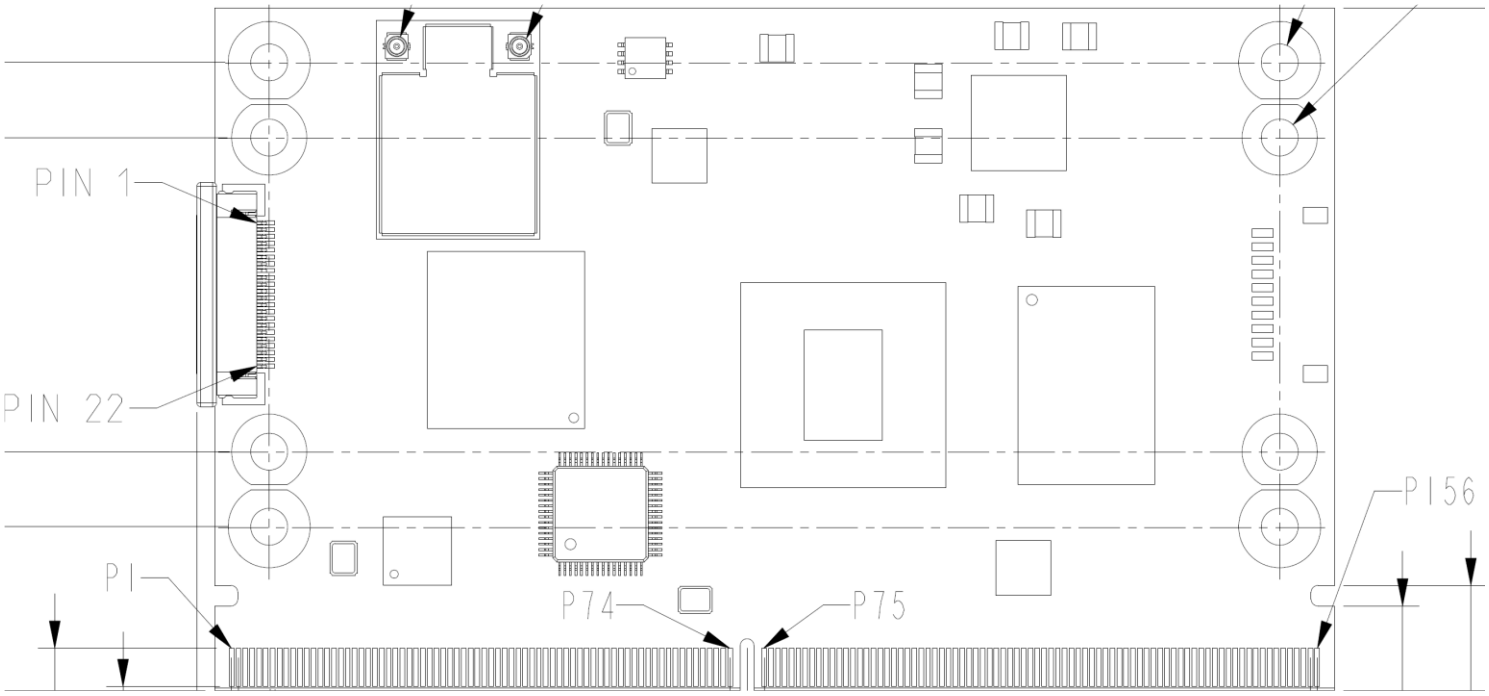
1.3.2 Operating Conditions

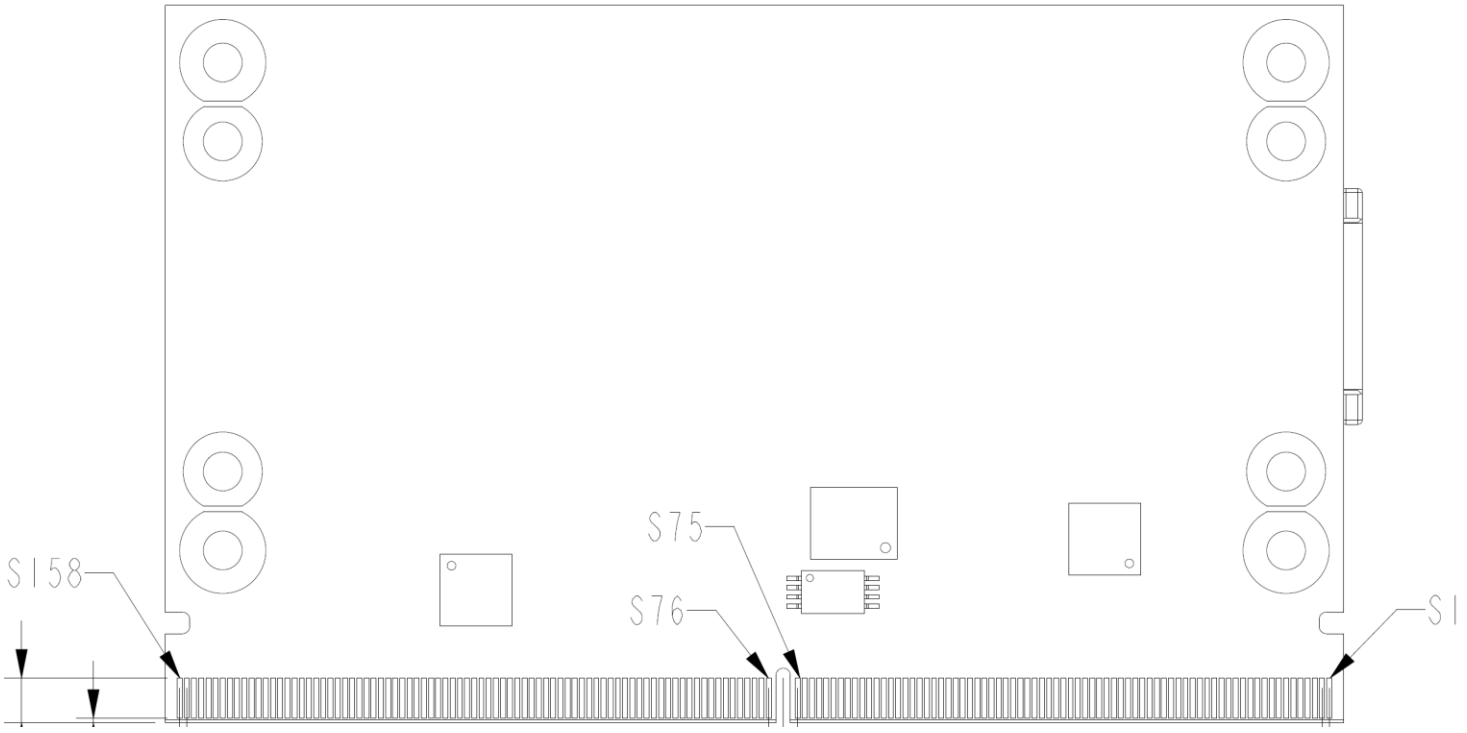
Features	Description
Operating Conditions	
Voltage	VBAT: 3V to 5.25V (5V typical)
Operating Temperature	Commercial grade: 0°C to 70°C[1] Industrial grade: -40°C to 85°C[1] [2]
Operating Humidity	less than 85%R.H.
Storage Temperature	-40°C to 85°C
Storage Humidity	less than 60%R.H.
ESD Protection	
Human Body Model	N/A
Changed Device Model	N/A

[1] Based on the operating temperature grade of the SMARC components and the cooling performance.
[2] The Wi-Fi module operating temperature is only -30°C to 85°C.

2. Pin Definition

2.1 Pin Map





2.2 Pin Table

2.2.1 Module Pin Table

Pin No	Definition	Basic Description	Voltage	Type
S38	AUDIO_MCK	Master Clock Output to I2S Codec(s)	1.8V	O CMOS
S156	BATLOW#	Battery low indication to Module. Carrier to float the line in inactive state.	1.8-5V	I
P123	BOOT_SEL0#	IMX8MP BOOT mode select BOOT_MODE0. 10 K ohms internal pull up	1.8V	I
P124	BOOT_SEL1#	IMX8MP BOOT mode select BOOT_MODE1. 10 K ohms internal pull up	1.8V	I
P125	BOOT_SEL2#	IMX8MP BOOT mode select BOOT_MODE2. 100 K ohms internal pull down	1.8V	I
S6	CAM_MCK	Master clock output. Connect to SMARC MIPI-CSI Feature Connector Pin 22 internally.	1.8V	O
P144	CAN0_RX	CAN Port 0 Receive Input (optional)	1.8V	I CMOS
P143	CAN0_TX	CAN Port 0 Transmit Output (optional)	1.8V	O CMOS
P146	CAN1_RX	CAN Port 1 Receive Input	1.8V	I CMOS
P145	CAN1_TX	CAN Port 1 Transmit Output	1.8V	O CMOS
S154	CARRIER_PWR_ON	Carrier Board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	1.8V	O
S153	CARRIER_STBY#	The Module shall drive this signal low when the system is in a standby power state.	1.8V	O
S152	CHARGER_PRSNT#	Held low by Carrier if DC input for battery charger is present.	1.8-5V	I
S151	CHARGING#	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	1.8-5V	I
S9	CSI0_CK-	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
S8	CSI0_CK+	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
S12	CSI0_RX0-	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
S11	CSI0_RX0+	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
S15	CSI0_RX1-	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I

S14	CSI0_RX1+	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
P4	CSI1_CK-	CSI1 differential clock input (point to point)		I
P3	CSI1_CK+	CSI1 differential clock input (point to point)		I
P8	CSI1_RX0-	CSI1 differential input (point to point)		I
P7	CSI1_RX0+	CSI1 differential input (point to point)		I
P11	CSI1_RX1-	CSI1 differential input (point to point)		I
P10	CSI1_RX1+	CSI1 differential input (point to point)		I
P14	CSI1_RX2-	CSI1 differential input (point to point)		I
P13	CSI1_RX2+	CSI1 differential input (point to point)		I
P17	CSI1_RX3-	CSI1 differential input (point to point)		I
P16	CSI1_RX3+	CSI1 differential input (point to point)		I
S135	DSI0_CLK-	Primary DSI Panel Differential Pair Clock Lines		O
S134	DSI0_CLK+	Primary DSI Panel Differential Pair Clock Lines		O
S126	DSI0_D0-	Primary DSI Panel Differential Pair Data Lines		I/O
S125	DSI0_D0+	Primary DSI Panel Differential Pair Data Lines		I/O
S129	DSI0_D1-	Primary DSI Panel Differential Pair Data Lines		O
S128	DSI0_D1+	Primary DSI Panel Differential Pair Data Lines		O
S132	DSI0_D2-	Primary DSI Panel Differential Pair Data Lines		O
S131	DSI0_D2+	Primary DSI Panel Differential Pair Data Lines		O
S138	DSI0_D3-	Primary DSI Panel Differential Pair Data Lines		O
S137	DSI0_D3+	Primary DSI Panel Differential Pair Data Lines		O
S155	FORCE_RECOV#	Low on this pin allows nonprotected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module.	1.8V	I
P25	GBE0_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	3.3V	O
P21	GBE0_LINK100#	Link Speed Indication LED for GBE0 100Mbps	3.3V	O

P22	GBE0_LINK1000#	Link Speed Indication LED for GBE0 1000Mbps	3.3V	O
P29	GBE0_MDI0-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P30	GBE0_MDI0+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P26	GBE0_MDI1-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P27	GBE0_MDI1+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P23	GBE0_MDI2-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P24	GBE0_MDI2+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P19	GBE0_MDI3-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P20	GBE0_MDI3+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
S31	GBE1_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	3.3V	O
S19	GBE1_LINK100#	Link Speed Indication LED for GBE0 100Mbps	3.3V	O
S22	GBE1_LINK1000#	Link Speed Indication LED for GBE0 1000Mbps	3.3V	O
S18	GBE1_MDI0-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O

S17	GBE1_MDI0+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
S21	GBE1_MDI1-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
S20	GBE1_MDI1+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
S24	GBE1_MDI2-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
S23	GBE1_MDI2+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
S27	GBE1_MDI3-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
S26	GBE1_MDI3+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P100	GND_P100	Ground		Ground
P103	GND_P103	Ground		Ground
P12	GND_P12	Ground		Ground
P120	GND_P120	Ground		Ground
P133	GND_P133	Ground		Ground
P142	GND_P142	Ground		Ground
P15	GND_P15	Ground		Ground
P18	GND_P18	Ground		Ground
P2	GND_P2	Ground		Ground

P32	GND_P32	Ground		Ground
P38	GND_P38	Ground		Ground
P47	GND_P47	Ground		Ground
P50	GND_P50	Ground		Ground
P53	GND_P53	Ground		Ground
P59	GND_P59	Ground		Ground
P68	GND_P68	Ground		Ground
P79	GND_P79	Ground		Ground
P82	GND_P82	Ground		Ground
P85	GND_P85	Ground		Ground
P88	GND_P88	Ground		Ground
P9	GND_P9	Ground		Ground
P91	GND_P91	Ground		Ground
P94	GND_P94	Ground		Ground
P97	GND_P97	Ground		Ground
S10	GND_S10	Ground		Ground
S101	GND_S101	Ground		Ground
S110	GND_S110	Ground		Ground
S119	GND_S119	Ground		Ground
S124	GND_S124	Ground		Ground
S13	GND_S13	Ground		Ground
S130	GND_S130	Ground		Ground
S136	GND_S136	Ground		Ground
S143	GND_S143	Ground		Ground
S158	GND_S158	Ground		Ground
S16	GND_S16	Ground		Ground

S25	GND_S25	Ground		Ground
S3	GND_S3	Ground		Ground
S34	GND_S34	Ground		Ground
S47	GND_S47	Ground		Ground
S61	GND_S61	Ground		Ground
S64	GND_S64	Ground		Ground
S67	GND_S67	Ground		Ground
S70	GND_S70	Ground		Ground
S73	GND_S73	Ground		Ground
S80	GND_S80	Ground		Ground
S83	GND_S83	Ground		Ground
S86	GND_S86	Ground		Ground
S89	GND_S89	Ground		Ground
S92	GND_S92	Ground		Ground
P108	GPIO0 / CAM0_PWR#	GPIO	1.8V	I/O
P109	GPIO1 / CAM1_PWR#	GPIO	1.8V	I/O
P118	GPIO10	GPIO	1.8V	I/O
P119	GPIO11	GPIO	1.8V	I/O
S142	GPIO12	GPIO	1.8V	I/O
S123	GPIO13	GPIO	1.8V	I/O
P110	GPIO2 / CAM0_RST#	GPIO	1.8V	I/O
P111	GPIO3 / CAM1_RST#	GPIO	1.8V	I/O
P112	GPIO4 / HDA_RST#	GPIO	1.8V	I/O
P113	GPIO5 / PWM_OUT	GPIO5 PWM capability	1.8V	I/O
P114	GPIO6 / TACHIN	GPIO6 Tachin capability	1.8V	I/O
P115	GPIO7	GPIO	1.8V	I/O

P116	GPIO8	GPIO	1.8V	I/O
P117	GPIO9	GPIO	1.8V	I/O
S53	HDA_CK / I2S2_CK	I2S2 Digital Audio Clock. Floating if CAN0_RX is used	1.8V	I/O CMOS
S52	HDA_SDI / I2S2_SDIN	I2S2 Digital Audio Input	1.8V	I CMOS
S51	HDA_SDO / I2S2_SDOUT	I2S2 Digital Audio Output	1.8V	O CMOS
S50	HDA_SYNC / I2S2_LRCK	I2S2 Left & Right Synchronization Clock. Floating if CAN0_TX is used	1.8V	I/O CMOS
P102	HDMI_CK-	HDMI Port, Differential Pair Clock Lines		O
P101	HDMI_CK+	HDMI Port, Differential Pair Clock Lines		O
P105	HDMI_CTRL_CK	I2C_CLK Line Dedicated to HDMI	1.8V	I/O
P106	HDMI_CTRL_DAT	I2C_DAT Line Dedicated to HDMI	1.8V	I/O
P99	HDMI_D0-	HDMI Port, Differential Pair Data Lines		O
P98	HDMI_D0+	HDMI Port, Differential Pair Data Lines		O
P96	HDMI_D1-	HDMI Port, Differential Pair Data Lines		O
P95	HDMI_D1+	HDMI Port, Differential Pair Data Lines		O
P93	HDMI_D2-	HDMI Port, Differential Pair Data Lines		O
P92	HDMI_D2+	HDMI Port, Differential Pair Data Lines		O
P104	HDMI_HPD	HDMI Hot Plug Active High Detection Signal that Serves as an Interrupt Request	1.8V	I
S5	I2C_CAM0_CK	CAM0 I2C clock for serial camera data support link. Connect to SMARC MIPI-CSI Feature Connector Pin 19 internally. With PU 4.7k ohms on module.	1.8V	I/O
S7	I2C_CAM0_DAT	CAM0 I2C data for serial camera data support link. Connect to SMARC MIPI-CSI Feature Connector Pin 20 internally. With PU 4.7k ohms on module.	1.8V	I/O
S1	I2C_CAM1_CK	CAM1 I2C clock for serial camera data support link. I2C address 0x68(1101000x) is used by internal PCIe clock source With PU 4.7k ohms on module.	1.8V	I/O
S2	I2C_CAM1_DAT	CAM1 I2C data for serial camera data support link. I2C address 0x68(1101000x) is used by internal PCIe clock source With PU 4.7k ohms on module.	1.8V	I/O
S48	I2C_GP_CK	General Purpose I2C Clock Signal. I2C address 0x50(1010000x) is used by internal EEPROM With PU 4.7k ohms on module.	1.8V	I/O
S49	I2C_GP_DAT	General Purpose I2C Data Signal. I2C address 0x50(1010000x) is used by internal EEPROM With PU 4.7k ohms on module.	1.8V	I/O

S139	I2C_LCD_CK	DDC Clock Line Used for Flat Panel Detection and Control. I2C address 0x25(0100101x) is used by internal PMIC With PU 4.7k ohms on module.	1.8V	I/O
S140	I2C_LCD_DAT	DDC Data Line Used for Flat Panel Detection and Control. I2C address 0x25(0100101x) is used by internal PMIC With PU 4.7k ohms on module.	1.8V	I/O
P121	I2C_PM_CK	Power management I2C bus CLK. With PU 2.2k ohms on module.	1.8V	I/O
P122	I2C_PM_DAT	Power management I2C bus DATA With PU 2.2k ohms on module.	1.8V	I/O
S42	I2S0_CK	I2S0 Digital Audio Clock	1.8V	I/O CMOS
S39	I2S0_LRCK	I2S0 Left & Right Synchronization Clock	1.8V	I/O CMOS
S41	I2S0_SDIN	I2S0 Digital Audio Input	1.8V	I CMOS
S40	I2S0_SDOUT	I2S0 Digital Audio Output	1.8V	O CMOS
S127	LCD0_BKLT_EN	Primary Panel Backlight Enable	1.8V	O
S141	LCD0_BKLT_PWM	Primary Panel Brightness Control	1.8V	O
S133	LCD0_VDD_EN	Primary Panel Power Enable	1.8V	O
S148	LID#	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the Module.	1.8-5V	I
S112	LVDS1_0-	Secondary LVDS Channel Differential Pair Data Lines		O
S111	LVDS1_0+	Secondary LVDS Channel Differential Pair Data Lines		O
S115	LVDS1_1-	Secondary LVDS Channel Differential Pair Data Lines		O
S114	LVDS1_1+	Secondary LVDS Channel Differential Pair Data Lines		O
S118	LVDS1_2-	Secondary LVDS Channel Differential Pair Data Lines		O
S117	LVDS1_2+	Secondary LVDS Channel Differential Pair Data Lines		O
S121	LVDS1_3-	Secondary LVDS Channel Differential Pair Data Lines		O
S120	LVDS1_3+	Secondary LVDS Channel Differential Pair Data Lines		O
S109	LVDS1_CK-	Secondary LVDS Channel Differential Pair Clock Lines		O
S108	LVDS1_CK+	Secondary LVDS Channel Differential Pair Clock Lines		O
S106	NC_DP0_AUX-	Floating Pin, No connect to anything.		Floating
S95	NC_DP0_AUX_SEL	Floating Pin, No connect to anything.		Floating

S105	NC_DP0_AUX+	Floating Pin, No connect to anything.		Floating
S98	NC_DP0_HPD	Floating Pin, No connect to anything.		Floating
S94	NC_DP0_LANE0-	Floating Pin, No connect to anything.		Floating
S93	NC_DP0_LANE0+	Floating Pin, No connect to anything.		Floating
S97	NC_DP0_LANE1-	Floating Pin, No connect to anything.		Floating
S96	NC_DP0_LANE1+	Floating Pin, No connect to anything.		Floating
S100	NC_DP0_LANE2-	Floating Pin, No connect to anything.		Floating
S99	NC_DP0_LANE2+	Floating Pin, No connect to anything.		Floating
S103	NC_DP0_LANE3-	Floating Pin, No connect to anything.		Floating
S102	NC_DP0_LANE3+	Floating Pin, No connect to anything.		Floating
P107	NC_DP1_AUX_SEL	Floating Pin, No connect to anything.		Floating
S144	NC_eDP0_HPD	Floating Pin, No connect to anything.		Floating
S113	NC_eDP1_HPD	Floating Pin, No connect to anything.		Floating
S43	NC_ESPI_ALERT0#	Floating Pin, No connect to anything.		Floating
S44	NC_ESPI_ALERT1#	Floating Pin, No connect to anything.		Floating
S58	NC_ESPI_RESET#	Floating Pin, No connect to anything.		Floating
P28	NC_GBE0_CTREF	Floating Pin, No connect to anything.		Floating
P6	NC_GBE0_SDP	Floating Pin, No connect to anything.		Floating
S28	NC_GBE1_CTREF	Floating Pin, No connect to anything.		Floating
P5	NC_GBE1_SDP	Floating Pin, No connect to anything.		Floating
S107	NC_LCD1_BKLT_EN	Floating Pin, No connect to anything.		Floating
S122	NC_LCD1_BKLT_PWM	Floating Pin, No connect to anything.		Floating
S116	NC_LCD1_VDD_EN	Floating Pin, No connect to anything.		Floating
S45	NC_MDIO_CLK	Floating Pin, No connect to anything.		Floating
S46	NC_MDIO_DAT	Floating Pin, No connect to anything.		Floating
P78	NC_PCIE_A_CKREQ#	Floating Pin, No connect to anything.		Floating

P84	NC_PCIE_A_REFCK-	Floating Pin, No connect to anything.		Floating
P83	NC_PCIE_A_REFCK+	Floating Pin, No connect to anything.		Floating
P75	NC_PCIE_A_RST#	Floating Pin, No connect to anything.		Floating
P87	NC_PCIE_A_RX-	Floating Pin, No connect to anything.		Floating
P86	NC_PCIE_A_RX+	Floating Pin, No connect to anything.		Floating
P90	NC_PCIE_A_TX-	Floating Pin, No connect to anything.		Floating
P89	NC_PCIE_A_TX+	Floating Pin, No connect to anything.		Floating
P77	NC_PCIE_B_CKREQ#	Floating Pin, No connect to anything.		Floating
S85	NC_PCIE_B_REFCK-	Floating Pin, No connect to anything.		Floating
S84	NC_PCIE_B_REFCK+	Floating Pin, No connect to anything.		Floating
S76	NC_PCIE_B_RST#	Floating Pin, No connect to anything.		Floating
S88	NC_PCIE_B_RX-	Floating Pin, No connect to anything.		Floating
S87	NC_PCIE_B_RX+	Floating Pin, No connect to anything.		Floating
S91	NC_PCIE_B_TX-	Floating Pin, No connect to anything.		Floating
S90	NC_PCIE_B_TX+	Floating Pin, No connect to anything.		Floating
P81	NC_PCIE_C_REFCK-	Floating Pin, No connect to anything.		Floating
P80	NC_PCIE_C_REFCK+	Floating Pin, No connect to anything.		Floating
S77	NC_PCIE_C_RST#	Floating Pin, No connect to anything.		Floating
S79	NC_PCIE_C_RX-	Floating Pin, No connect to anything.		Floating
S78	NC_PCIE_C_RX+	Floating Pin, No connect to anything.		Floating
S82	NC_PCIE_C_TX-	Floating Pin, No connect to anything.		Floating
S81	NC_PCIE_C_TX+	Floating Pin, No connect to anything.		Floating
S33	NC_PCIE_D_RX-	Floating Pin, No connect to anything.		Floating
S32	NC_PCIE_D_RX+	Floating Pin, No connect to anything.		Floating
S30	NC_PCIE_D_TX-	Floating Pin, No connect to anything.		Floating
S29	NC_PCIE_D_TX+	Floating Pin, No connect to anything.		Floating

S146	NC_PCIE_WAKE#	Floating Pin, No connect to anything.		Floating
S54	NC_SATA_ACT#	Floating Pin, No connect to anything.		Floating
P52	NC_SATA_RX-	Floating Pin, No connect to anything.		Floating
P51	NC_SATA_RX+	Floating Pin, No connect to anything.		Floating
P49	NC_SATA_TX-	Floating Pin, No connect to anything.		Floating
P48	NC_SATA_TX+	Floating Pin, No connect to anything.		Floating
P132	NC_SER0_CTS#	Floating Pin, No connect to anything.		Floating
P131	NC_SER0_RTS#	Floating Pin, No connect to anything.		Floating
P130	NC_SER0_RX	Floating Pin, No connect to anything.		Floating
P129	NC_SER0_TX	Floating Pin, No connect to anything.		Floating
P31	NC_SPI0_CS1#	Floating Pin, No connect to anything.		Floating
P55	NC_SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	Floating Pin, No connect to anything.		Floating
P64	NC_USB0_OTG_ID	Floating Pin, No connect to anything.		Floating
S75	NC_USB2_SSRX-	Floating Pin, No connect to anything.		Floating
S74	NC_USB2_SSRX+	Floating Pin, No connect to anything.		Floating
S72	NC_USB2_SSTX-	Floating Pin, No connect to anything.		Floating
S71	NC_USB2_SSTX+	Floating Pin, No connect to anything.		Floating
S60	NC_USB5-	Floating Pin, No connect to anything.		Floating
S55	NC_USB5_EN_OC#	Floating Pin, No connect to anything.		Floating
S59	NC_USB5+	Floating Pin, No connect to anything.		Floating
S147	NC_VDD_RTC	Floating Pin, No connect to anything.		Floating
P128	POWER_BTN#	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module	1.8-5V	I
P56	QSPI_CK	floating, if internal QSPI flash is used	1.8V	O CMOS
P54	QSPI_CS0#	floating, if internal QSPI flash is used	1.8V	O CMOS
P58	QSPI_IO_0	floating, if internal QSPI flash is used	1.8V	I/O CMOS

P57	QSPI_IO_1	floating, if internal QSPI flash is used	1.8V	I/O CMOS
S56	QSPI_IO_2	floating, if internal QSPI flash is used	1.8V	I/O CMOS
S57	QSPI_IO_3	floating, if internal QSPI flash is used	1.8V	I/O CMOS
P127	RESET_IN#	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise.	1.8-5V	I
P126	RESET_OUT#	General purpose reset output to Carrier Board.	1.8V	O
P73	RSVD_EARC_N_HPD	EARC N HPD Out		O
P72	RSVD_EARC_P_UTIL	EARC P UTIL Out		O
S4	RSVD_PMIC_32K_OUT_1V8_CEC	32.768 CLK output from internal PMIC. Can be used for HDMI CEC pin (different HW option)	1.8V	O
P35	SDIO_CD#	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	1.8/3.3V	I
P36	SDIO_CK	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	1.8/3.3V	O
P34	SDIO_CMD	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	1.8/3.3V	I/O
P39	SDIO_D0	SDIO Data lines. These signals operate in push-pull mode.	1.8/3.3V	I/O
P40	SDIO_D1	SDIO Data lines. These signals operate in push-pull mode.	1.8/3.3V	I/O
P41	SDIO_D2	SDIO Data lines. These signals operate in push-pull mode.	1.8/3.3V	I/O
P42	SDIO_D3	SDIO Data lines. These signals operate in push-pull mode.	1.8/3.3V	I/O
P37	SDIO_PWR_EN	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	3.3V	O
P33	SDIO_WP	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	1.8/3.3V	I
P135	SER1_RX	Asynchronous Serial Data Input Port 1. For A53 debug use by default	1.8V	I
P134	SER1_TX	Asynchronous Serial Data Output Port 1. For A53 debug use by default	1.8V	O
P139	SER2_CTS#	Clear to Send Handshake Line for Port 1	1.8V	I
P138	SER2_RTS#	Request to Send Handshake Line for Port 1	1.8V	O
P137	SER2_RX	Asynchronous Serial Data Input Port 2	1.8V	I
P136	SER2_TX	Asynchronous Serial Data Output Port 2	1.8V	O
P141	SER3_RX	Asynchronous Serial Data Input Port 3. For M7 debug use by default	1.8V	I
P140	SER3_TX	Asynchronous Serial Data Output Port 3. For M7 debug use by default	1.8V	O

S149	SLEEP#	Sleep indicator from Carrier Board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	1.8-5V	I
P1	SMB_ALERT	SMBus Alert# (Interrupt) Signal	1.8-5V	I OD CMOS
P44	SPI0_CK	SPI0 Clock	1.8V	O
P43	SPI0_CS0#	SPI0 Master Chip Select 0	1.8V	O
P45	SPI0_DIN	SPI0 Master input / Slave output	1.8V	I
P46	SPI0_DO	SPI0 Master output / Slave input	1.8V	O
S157	TEST#	IMX8MP BOOT mode select BOOT_MODE3. 100 K ohms internal pull down	1.8-5V	I
P61	USB0-	USB Differential Data Pairs for Port 0		I/O
P62	USB0_EN_OC#	USB Over-Current Sense for Port 1 (10K PU on Module). 500mA Max	3.3V	I/O OD CMOS
P63	USB0_VBUS_DET	Isolated with a 30K resistor inside the module	USB VBUS 5V	USB VBUS 5V
P60	USB0+	USB Differential Data Pairs for Port 0		I/O
P66	USB1-	USB Differential Data Pairs for Port 1		I/O
P67	USB1_EN_OC#	USB Over-Current Sense for Port 1 (10K PU on Module). 500mA Max	3.3V	I/O OD CMOS
P65	USB1+	USB Differential Data Pairs for Port 1		I/O
P70	USB2-	USB Differential Data Pairs for Port 2		I/O
P71	USB2_EN_OC#	USB Over-Current Sense for Port 2 (10K PU on Module). 500mA Max	3.3V	I/O OD CMOS
P69	USB2+	USB Differential Data Pairs for Port 2		I/O
S69	USB3-	USB Differential Data Pairs for Port 3		I/O
P74	USB3_EN_OC#	USB Over-Current Sense for Port 3 (10K PU on Module)	3.3V	I/O OD CMOS
S104	USB3_OTG_ID	Input Pin to Announce OTG Device Insertion on USB 3.x Port	3.3V	I CMOS
S66	USB3_SSRX-	Receive Signal Differential Pairs for SuperSpeed on Port 3		I
S65	USB3_SSRX+	Receive Signal Differential Pairs for SuperSpeed on Port 3		I
S63	USB3_SSTX-	Transmit Signal Differential Pairs for SuperSpeed on Port 3		O
S62	USB3_SSTX+	Transmit Signal Differential Pairs for SuperSpeed on Port 3		O
S37	USB3_VBUS_DET	Isolated with a 30K resistor inside the module	USB VBUS 5V	USB VBUS 5V

S68	USB3+	USB Differential Data Pairs for Port 3		I/O
S36	USB4-	USB Differential Data Pairs for Port 4		I/O
P76	USB4_EN_OC#	USB Over-Current Sense for Port 4 (10K PU on Module). 500mA Max	3.3V	I/O OD CMOS
S35	USB4+	USB Differential Data Pairs for Port 4		I/O
P147	VDD_IN_P147	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P148	VDD_IN_P148	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P149	VDD_IN_P149	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P150	VDD_IN_P150	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P151	VDD_IN_P151	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P152	VDD_IN_P152	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P153	VDD_IN_P153	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P154	VDD_IN_P154	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P155	VDD_IN_P155	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P156	VDD_IN_P156	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
S150	VIN_PWR_BAD#	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.	VDD_IN	I
S145	WDT_TIME_OUT#	Watch-Dog-Timer Output, low active	1.8V	O

2.2.2 CSI Feature Connector Pin Table (optional)

Pin No	Definition	Basic Description	Voltage	Type
1	CAM2_VCC_1	Camera power. Recommended Max. output current is 800mA(pin1+pin2)	3.3V	Power Out
2	CAM2_VCC_2	Camera power. Recommended Max. output current is 800mA(pin1+pin2)	3.3V	Power Out
3	GND_3	Ground		Ground
4	CSI2_RX0+	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
5	CSI2_RX0-	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
6	GND_6	Ground		Ground
7	CSI2_RX1+	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
8	CSI2_RX1-	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
9	GND_9	Ground		Ground
10	CSI2_RX2+	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
11	CSI2_RX2-	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
12	CAM2_RST#	Camera 2 reset, active low output. Connect to SMARC Pin P110 internally.	1.8V	O
13	CSI2_RX3+	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
14	CSI2_RX3-	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
15	GND_15	Ground		Ground
16	CSI2_CK+	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
17	CSI2_CK	Differential input (point to point). Use MIPI-CSI Feature Connector instead of the SMARC 2.0 CSI0 pin for 4 lane operation		I
18	GND_18	Ground		Ground
19	I2C_CAM2_CK	CAM0 I2C clock for serial camera data support link. Connect to SMARC Pin S5 internally.	1.8V	I/O
20	I2C_CAM2_DAT	CAM0 I2C data for serial camera data support link. Connect to SMARC Pin S7 internally.	1.8V	I/O
21	CAM2_PWR#	Camera 2 Power Enable, active low output. Connect to SMARC Pin P108 internally.	1.8V	O
22	CAM2_MCK	Master clock output. Connect to SMARC Pin S6 internally.	1.8V	O

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_IN	DC supply input	-0.5	-	+6	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_IN	DC supply input	3.0[1]	5	5.25	V

[1] Use 3.3V or higher voltage for optimal performance

3.3 GPIO DC Characteristics

For VDD = 1.8V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VOH	Output High Voltage	0.8 x VDD[2]	-	VDD	V
VOL	Output low level	0[3]	-	0.2 x VDD	V
VIH	Input High level	0.7 x VDD	-	VDD + 0.3	V
VIL	Input low level	-0.3	-	0.3 x VDD	V
	Pull-up resistor[4]	12	22	49	kOhms
	Pull-down resistor[5]	13	23	48	kOhms

For VDD = 3.3V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VOH	Output High Voltage	0.8 x VDD[6]	-	VDD	V
VOL	Output low level	0[7]	-	0.2 x VDD	V
VIH	Input High level	0.7 x VDD	-	VDD + 0.3	V
VIL	Input low level	-0.3	-	0.3 x VDD	V
	Pull-up resistor[8]	18	37	72	kOhms
	Pull-down resistor[9]	24	43	87	kOhms

[2] IOH = 1.6/3.2/6.4/9.6 mA
[3] IOL = 1.6/3.2/6.4/9.6 mA
[4] For IMX8MP GPIO port only
[5] For IMX8MP GPIO port only
[6] IOH = 2/4/8/12 mA
[7] IOL = 2/4/8/12 mA
[8] For IMX8MP GPIO port only
[9] For IMX8MP GPIO port only

3.4 Interface

3.4.1 ECSPI timing parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

3.4.1.1 ECSPI Master mode timing

Figure 1 depicts the timing of ECSPI in master mode. Table 1 ECSPI Master mode timing parameters lists the ECSPI master mode timing characteristics.

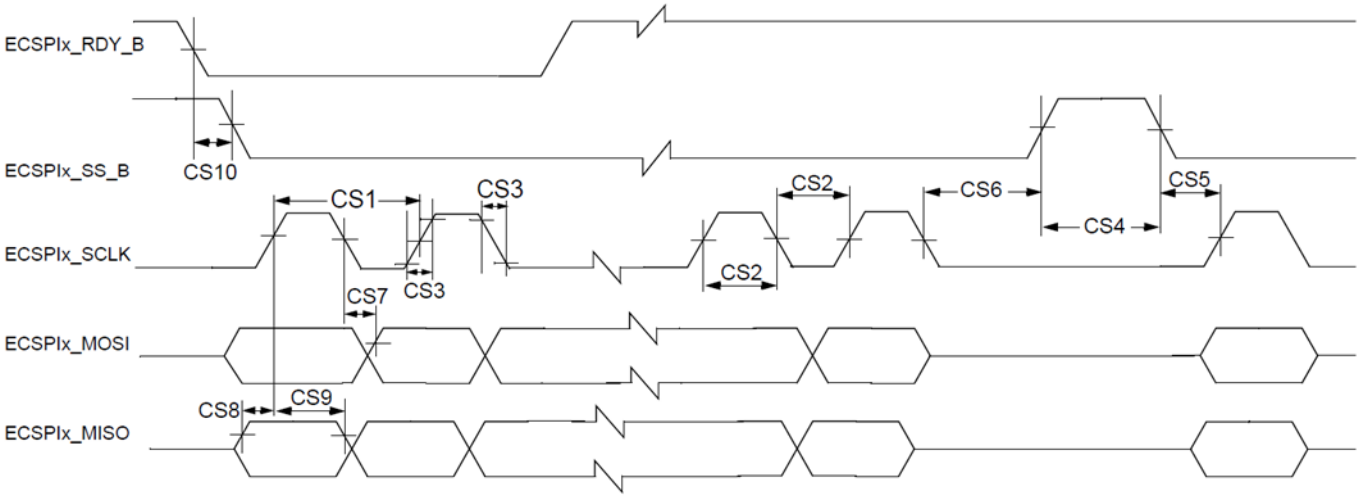


Figure 1

Table 1 ECSPI Master mode timing parameters

ID	Parameter	Symbol	Minimum	Maximum	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	tclk	See Table 2	-	ns
CS2	ECSPIx_SCLK High or Low Time–Read	tSW	21.5 7	-	ns
CS3	ECSPIx_SCLK Rise or Fall	tRISE/FALL	-	-	ns
CS4	ECSPIx_SS_B pulse width	tCSLH	Half ECSPIx_SCLK period	-	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	tSCS	Half ECSPIx_SCLK period - 4	-	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	tHCS	Half ECSPIx_SCLK period - 2	-	ns

CS7	ECSPIx_MOSI Propagation Delay (CLOAD = 20 pF)	tPDmosi	-1	1	ns
CS8	ECSPIx_MISO Setup Time	tSmiso	1.23	-	ns
CS9	ECSPIx_MISO Hold Time	tHmiso	3.09	-	ns
CS10	RDY to ECSPIx_SS_B Time	tSDRY	5	-	ns

Table 2 ECSPI Master Read and Write frequency

Instance	Mux mode	Master Read frequency	Master Write frequency	Unit
ECSPI1	Mux behind I2C1/I2C2	25	50	MHz
ECSPI1	Mux behind ECSPI1	30	60	MHz
ECSPI2	Mux behind SD2	30	60	MHz
ECSPI2	Mux behind ECSPI2	25	50	MHz
ECSPI3	Mux behind UART1/UART2	25	50	MHz

3.4.1.2 ECSPI Slave mode timing

Figure 2 depicts the timing of ECSPI in Slave mode. Table 3 ECSPI Slave mode timing parameters lists the ECSPI Slave mode timing characteristics.

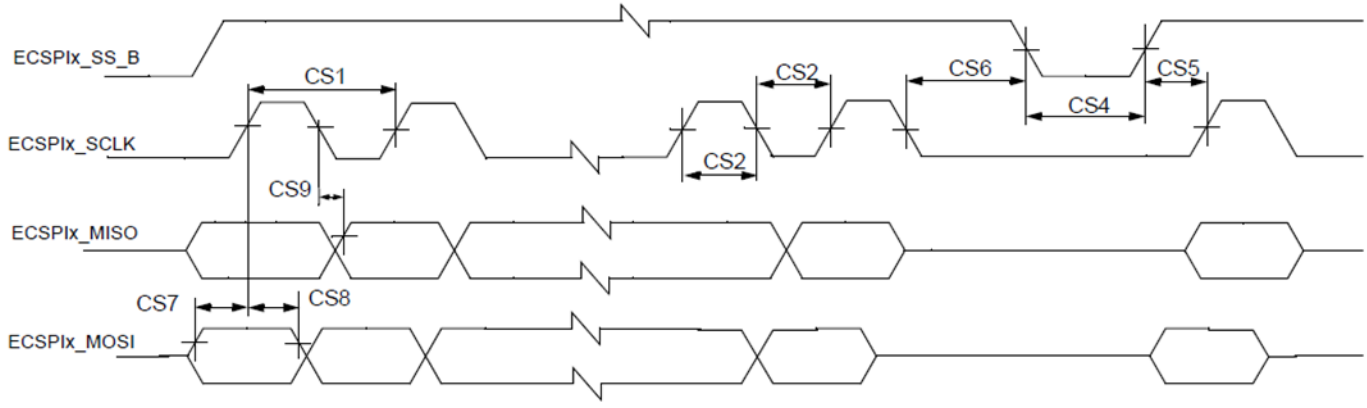


Figure 2

Table 3 ECSPI Slave mode timing parameters

ID	Parameter	Symbol	Minimum	Maximum	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	tclk	15 43	-	ns
CS2	ECSPIx_SCLK High or Low Time–Read	tSW	7 21.5	-	ns
CS4	ECSPIx_SS_B pulse width	tCSLH	Half ECSPIx_SCLK period	-	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	tSCS	5	-	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	tHCS	5	-	ns
CS7	ECSPIx_MOSI Setup Time	tSmiso	4	-	ns
CS8	ECSPIx_MISO Hold Time	tHmiso	4	-	ns
CS9	ECSPIx_MISO Propagation Delay (CLOAD = 20 pF)	tPDmiso	4	19	ns

3.4.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

3.4.2.1 SD3.0/eMMC5.1 (single data rate) AC timing

Figure 3 depicts the timing of SD3.0/eMMC5.1, and Table 4 SD3.0/eMMC5.1 (SDR) interface timing specification lists the SD3.0/eMMC5.1 timing characteristics.

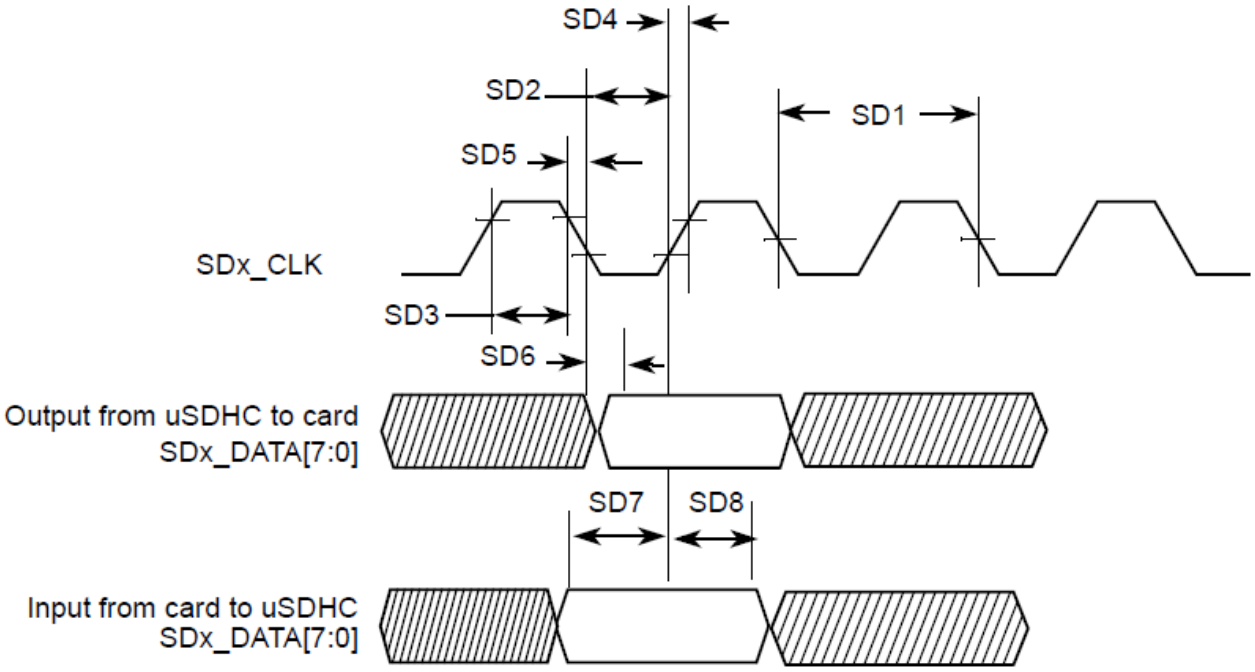


Figure 3

Table 4 SD3.0/eMMC5.1 (SDR) interface timing specification

ID	Parameter	Symbol	Minimum	Maximum	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	fPP[10]	0	400	KHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	fPP[11]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	fPP[12]	0	20/52	MHz
	Clock Frequency (Identification Mode)	fOD	100	400	KHz
SD2	Clock Low Time	tWL	7	-	ns
SD3	Clock High Time	tWH	7	-	ns
SD4	Clock Rise Time	tTLH	-	3	ns
SD5	Clock Fall Time	tTHL		3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	tOD	6.6	3.6	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	tISU	2.5	-	ns
SD8	uSDHC Input Hold Time[13]	tIH	1.5	-	ns

[10] In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
[11] In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0 – 25 MHz. In High-speed mode, clock frequency can be any value between 0 – 50 MHz.
[12] In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0 – 20 MHz. In High-speed mode, clock frequency can be any value between 0 – 52 MHz.
[13] To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.4.2.2 eMMC5.1/SD3.0 (dual data rate) AC timing

Figure 4 depicts the timing of eMMC5.1/SD3.0 (DDR). Table 5 eMMC5.1/SD3.0 (DDR) interface timing specification lists the eMMC5.1/SD3.0 (DDR) timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

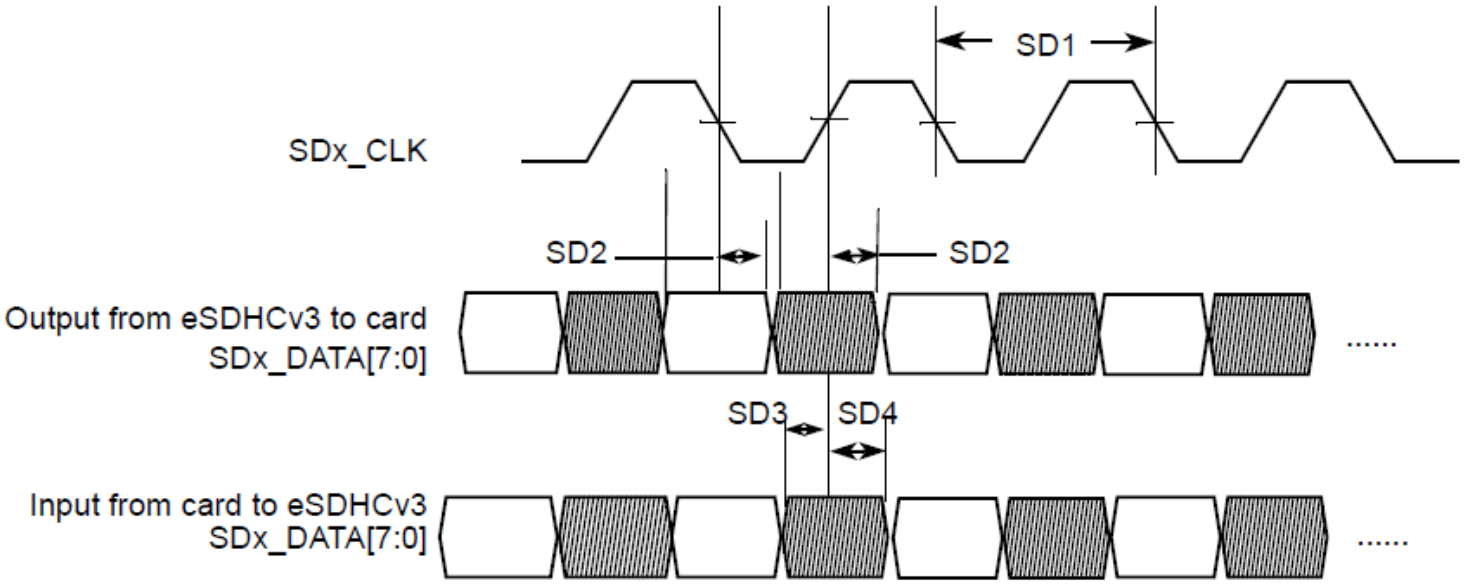


Figure 4

Table 5 eMMC5.1/SD3.0 (DDR) interface timing specification

ID	Parameter	Symbol	Minimum	Maximum	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC5.1 DDR)	fPP	0	52	MHz
	Clock Frequency (SD3.0 DDR)	fPP	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	tOD	2.7	6.9	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	tISU	2.4	-	ns
SD4	uSDHC Input Hold Time	tTLH	-	3	ns

3.4.2.3 HS400 DDR AC timing

Figure 5 depicts the timing of HS400 mode, and Table 6 HS400 interface timing specification lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in Table 43 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

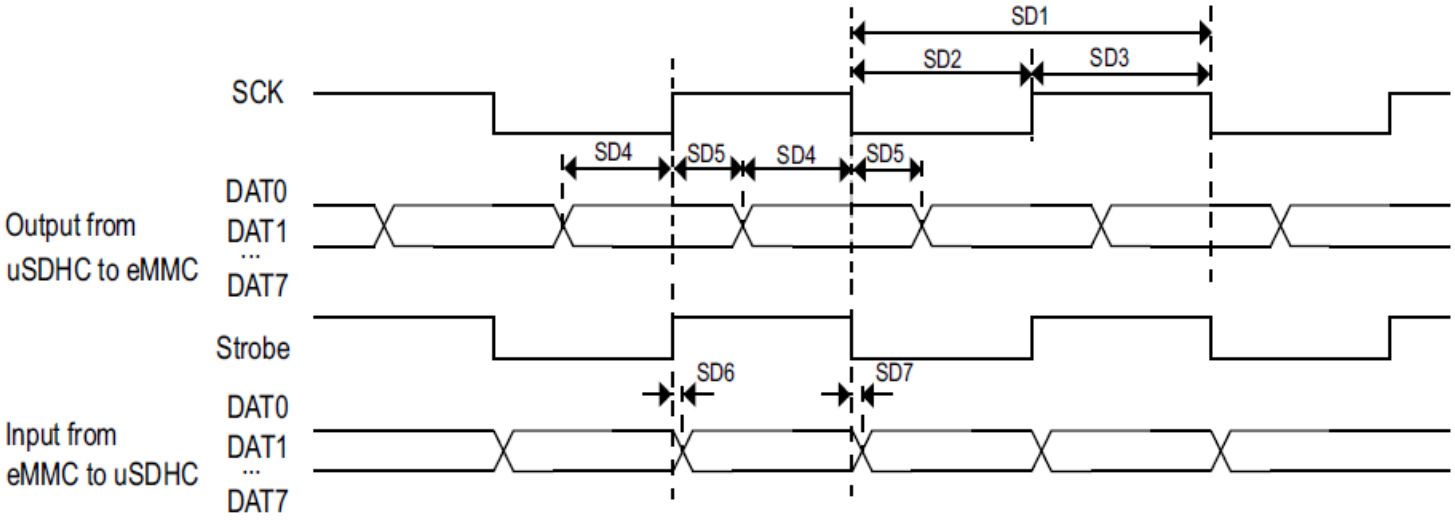


Figure 5

Table 6 HS400 interface timing specification

ID	Parameter	Symbol	Minimum	Maximum	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC5.1 DDR)	fPP	0	200	MHz
SD2	Clock low time	tCL	0.46 x tCLK	0.54 x tCLK	ns
SD3	Clock high time	tCH	0.46 x tCLK	0.54 x tCLK	ns
uSDHC Output/Card Inputs DAT (Reference to SCK)					
SD4	Output skew from data of edge of SCK	tOSkew1	0.45	-	ns
SD5	Output skew from edge of SCk to data	tOSkew2	0.45	-	ns
uSDHC Input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	tRQ	-	0.45	ns

SD7	uSDHC hold skew	tRQH	-	0.45	ns

3.4.2.4 HS200 DDR AC timing

Figure 6 depicts the timing of HS200 mode, and Table 7 HS200 interface timing specification lists the HS200 timing characteristics.

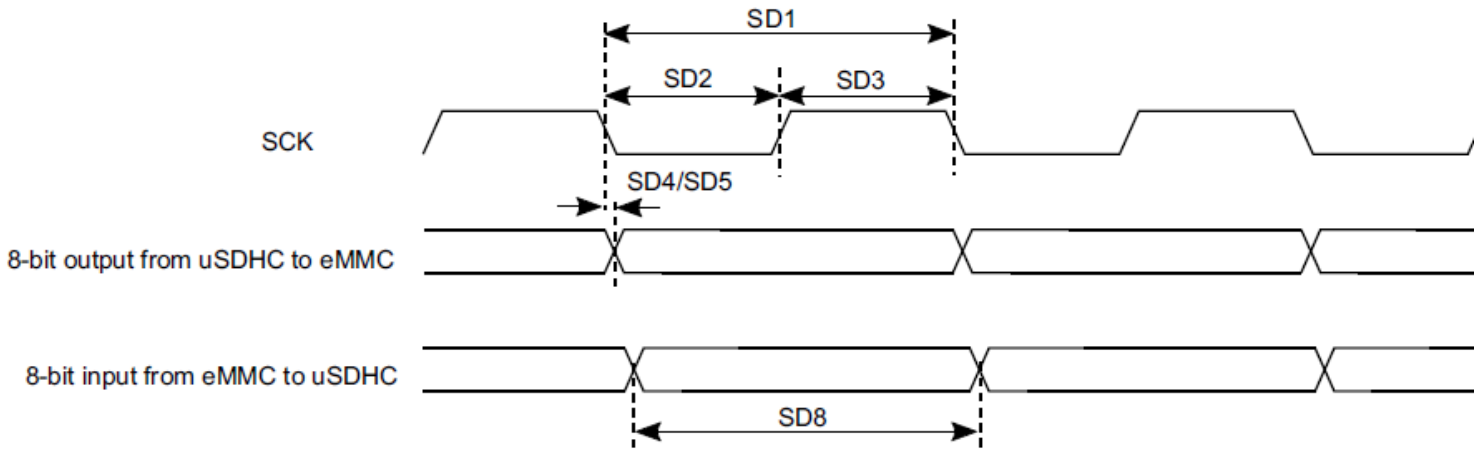


Figure 6

Table 7 HS200 interface timing specification

ID	Parameter	Symbol	Minimum	Maximum	Unit
Card Input Clock					
SD1	Clock Frequency Period	tCLK	5	-	ns
SD2	Clock low time	tCL	0.3 x tCLK	0.7 x tCLK	ns
SD3	Clock high time	tCH	0.3 x tCLK	0.7 x tCLK	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	tOD	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	tODW	0.5 x tCLK	-	ns

[1] HS200 is for 8 bits while SDR104 is for 4 bits.

3.4.2.5 SDR50/SDR104 AC timing

Figure 7 depicts the timing of SDR50/SDR104, and Table 43 lists the SDR50/SDR104 timing characteristics.

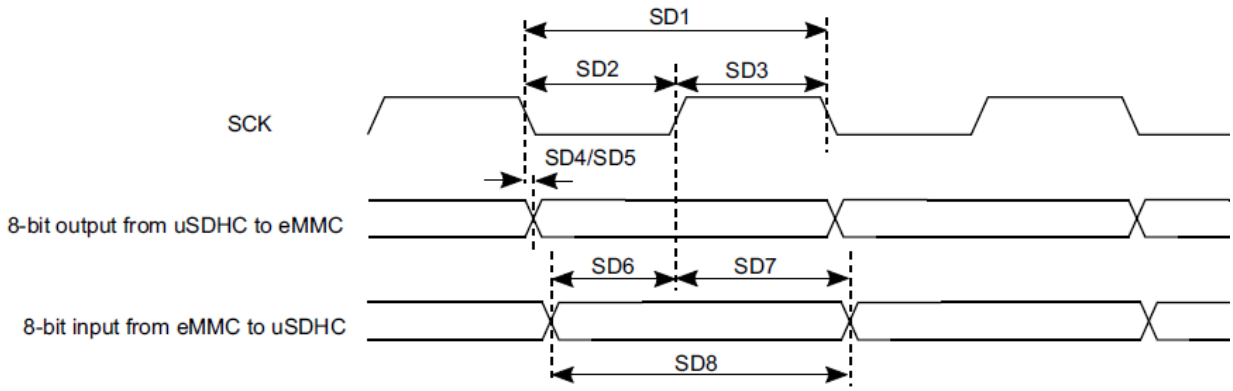


Figure 7

Table 8 SDR50/SDR104 interface timing specification

ID	Parameter	Symbol	Minimum	Maximum	Unit
Card Input Clock					
SD1	Clock Frequency Period	tCLK	5	-	ns
SD2	Clock low time	tCL	0.46 x tCLK	0.54 x tCLK	ns
SD3	Clock high time	tCH	0.46 x tCLK	0.54 x tCLK	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	tOD	-3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Data Window	tODW	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	tISU	2.4		ns
SD7	uSDHC Input Hold Time	tIH	1.4		ns

uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	tODW	0.5 x tCLK	-	ns

3.4.3 Pulse width modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Figure 8 depicts the timing of the PWM, and Table 9 PWM output timing parameters lists the PWM timing parameters.

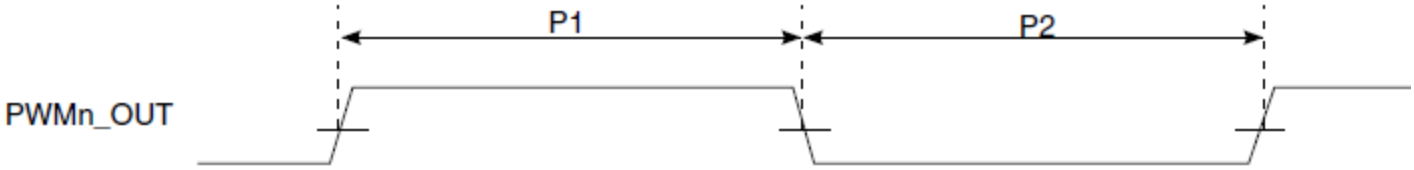


Figure 8

Table 9 PWM output timing parameters

ID	Parameter	Minimum	Maximum	Unit
	PWM Module Clock Frequency	0	66 (ipg_clk)	MHz
P1	PWM output pulse width high	12	-	ns
P2	PWM output pulse width low	12	-	ns

3.4.4 SAI/I2S switching specifications

This section provides the AC timings for the SAI in Master (clocks driven) and Slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0)

[1] Data window in SDR100 mode is variable.

and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

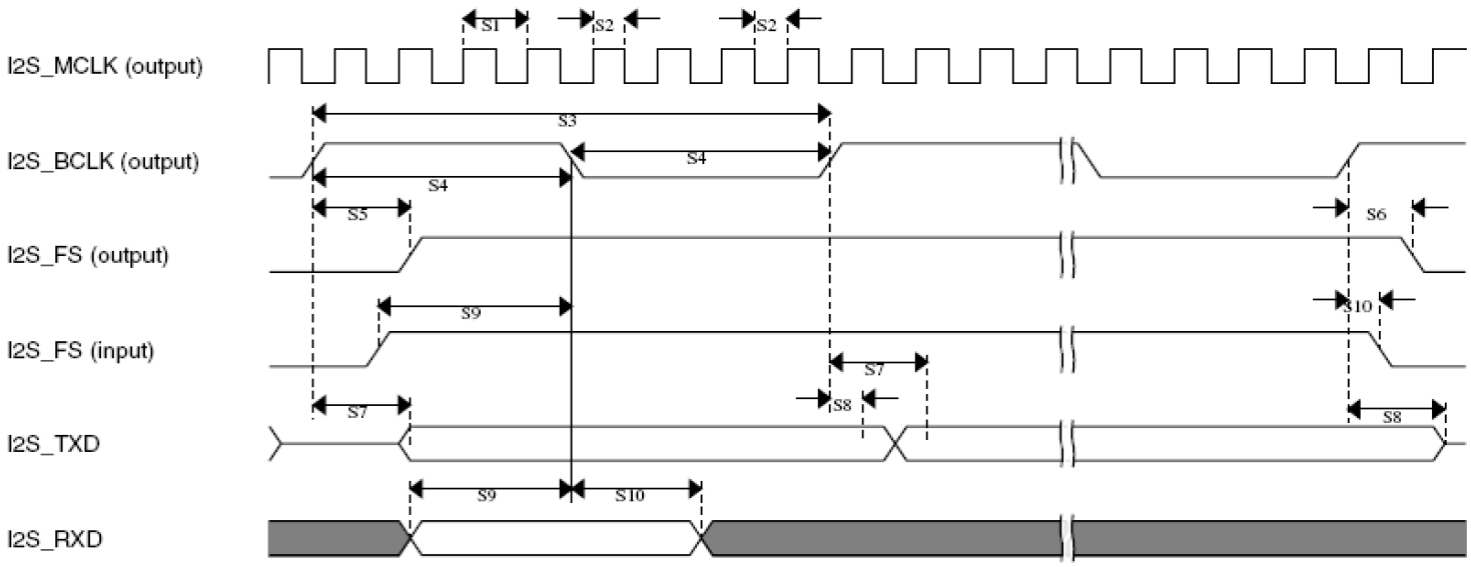


Figure 9 SAI timing—Master modes

Table 10 Master mode SAI timing (50 MHz)[1]

ID	Parameter	Minimum	Maximum	Unit
S1	SAI_MCLK cycle time	20	-	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	20	-	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	-	2	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	2	ns

[1] To achieve 50 MHz for BCLK operation, the following configuration must be used. In TX, configure BCI=0 in SAI TCR2 register and FSD=1 in SAI TCR4 register and in RX, configure BCI=1 in SAI TCR2 register and FSD=0 in SAI TCR4 register.

S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	2	-	ns
S9	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

Table 11 Master mode SAI timing (25 MHz)

ID	Parameter	Minimum	Maximum	Unit
S1	SAI_MCLK cycle time	40	-	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	-	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	-	2	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	2	ns
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	12	-	ns
S9	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

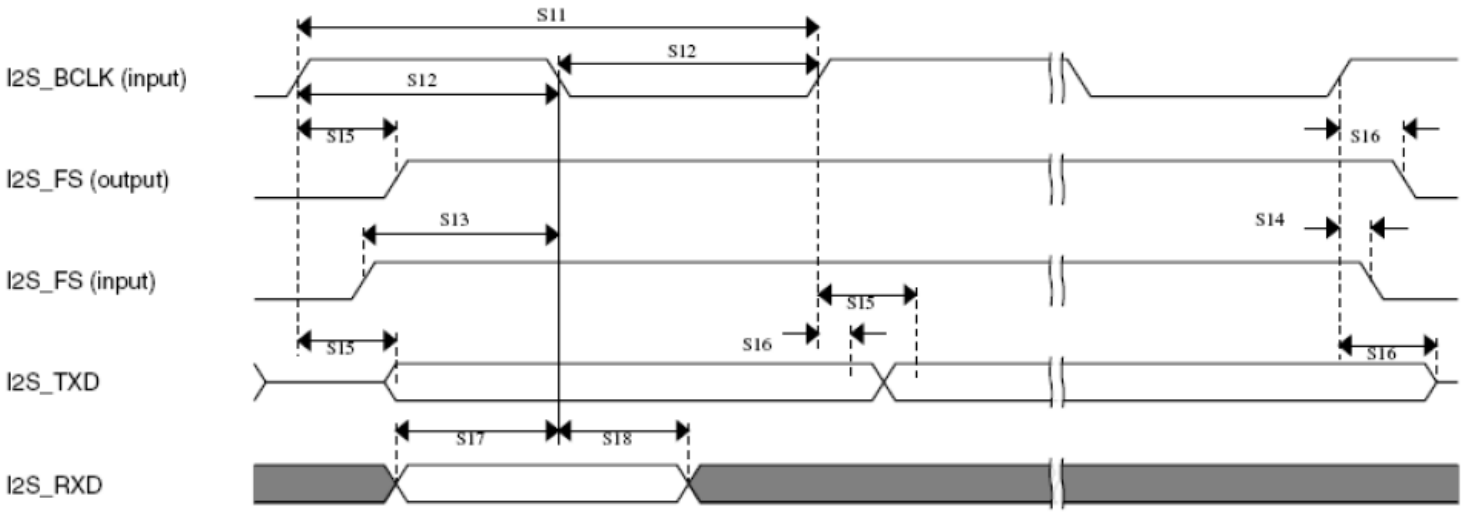


Figure 10 SAI Timing — Slave Modes

Table 12 Slave mode SAI timing (50 MHz)[1]

ID	Parameter	Minimum	Maximum	Unit
S11	SAI_BCLK cycle time (input)	20	-	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	2	-	ns
S14	SAI_FA input hold after SAI_BCLK	2	-	ns
S17	SAI_RXD setup before SAI_BCLK	2	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

Table 13 Slave mode SAI timing (25 MHz)

ID	Parameter	Minimum	Maximum	Unit
S11	SAI_BCLK cycle time (input)	40	-	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	12	-	ns
S14	SAI_FA input hold after SAI_BCLK	2	-	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	7	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	12	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

[1] TX does not support 50 MHz operation in Slave mode. To achieve 50 MHz BCLK in RX, configure BCI=1 in SAI TCR2 register and FSD=0 in SAI TCR4 register.

3.4.5 UART I/O configuration and timing parameters

3.4.5.1 UART RS-232 I/O configuration in different modes

The i.MX 8M Plus UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 14 UART I/O configuration vs. mode shows the UART I/O configuration based on the enabled mode.

Table 14 UART I/O configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	**Description**	**Direction**	**Description**
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

3.4.5.2 UART RS-232 Serial mode timing

This section describes the electrical information of the UART module in the RS-232 mode.

3.4.5.2.1 UART transmitter

Figure 11 depicts the transmit timing of UART in the RS-232 Serial mode, with 8 data bit/1 stop bit format. Table 15 RS-232 Serial mode transmit timing parameters lists the UART RS-232 Serial mode transmit timing characteristics.

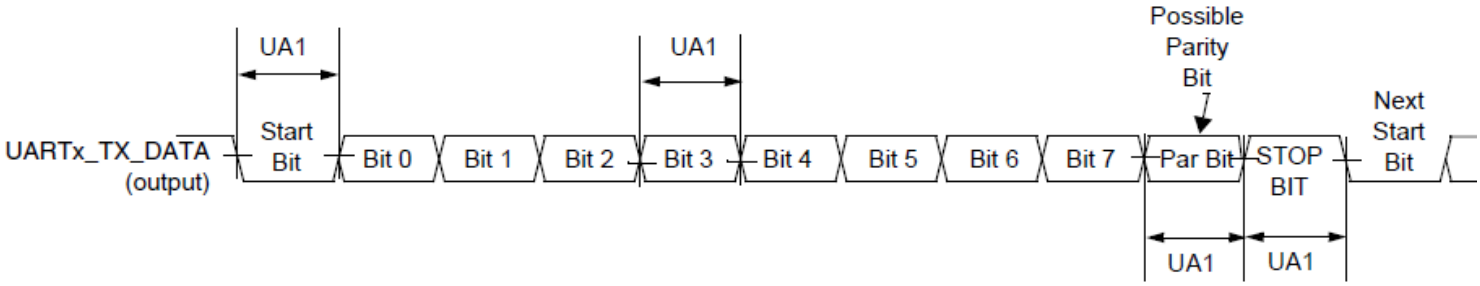


Figure 11

Table 15 RS-232 Serial mode transmit timing parameters

ID	Parameter	Symbol	Minimum	Maximum	Unit
UA1	Transmit Bit Time	tTbit	1/Fbaud_rate[1] - Tref_clk[2]	1/Fbaud_rate + Tref_clk	s

[1] Fbaud_rate: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.
[2] Tref_clk: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.4.5.2.2 UART receiver

Figure 12 depicts the RS-232 Serial mode receive timing with 8 data bit/1 stop bit format. Table 72 lists Serial mode receive timing characteristics.

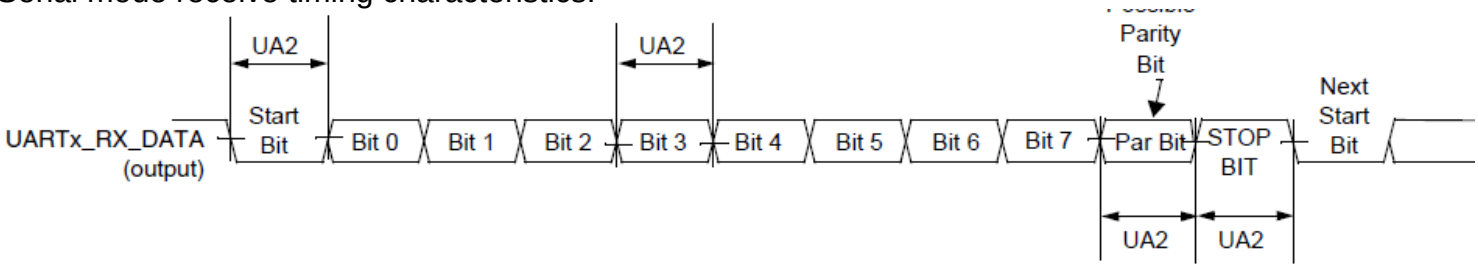


Figure 12

Table 16 RS-232 Serial mode receive timing parameters

ID	Parameter	Symbol	Minimum	Maximum	Unit
UA2	Receive Bit Time[1]	tRbit	1/Fbaud_rate[2] - 1/(16x Fbaud_rate)	1/Fbaud_rate +1/(16 x Fbaud_rate)	s

[1] The UART receiver can tolerate 1/(16 x Fbaud_rate) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x Fbaud_rate)

[2] Fbaud_rate: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

3.5 Boot mode configuration

Boot Mode	TEST#	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#
Boot from internal fuses	0	0	0	0
USB Serial Download	0	0	0	1
USDHC3 (eMMC)	0	0	1	0
USDHC2 (SD)	0	0	1	1
FlexSPI 3B Read	0	1	1	0
eCSPI Boot	1	0	0	0

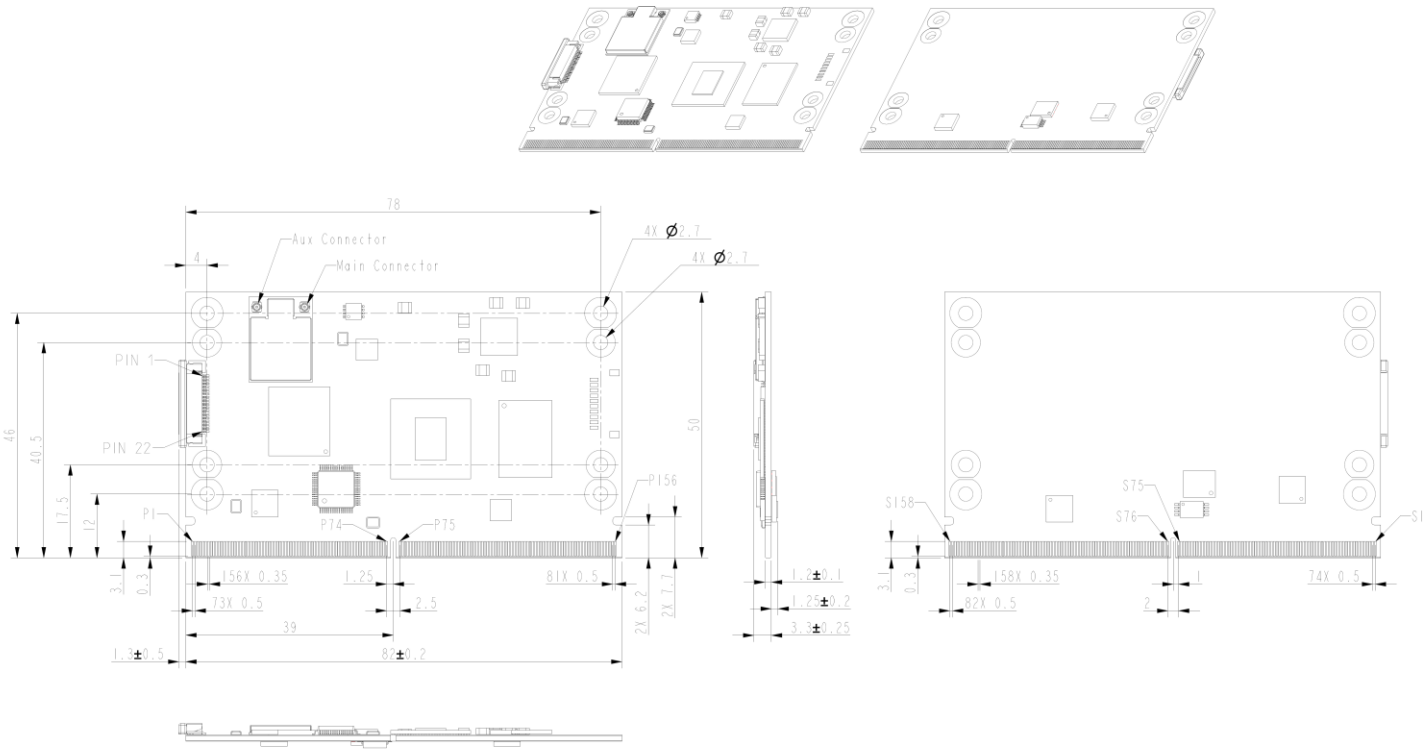
3.6 Power Consumption

Test Item[3]	VSYS_5V=5 V(mA)	
	Max.	Avg.
Power off mode	0.2	0.2
Suspend mode	50	50
IDLE_DEFAULT	434	346
IDLE_DEFAULT+WLAN Power Save Mode	475	353
Audio + Video_Playback(gplay)+WLAN_5GHz(iperf Tx50Mbit/s)	735	649
4-core Stream + GPU + VPU + WLAN_5G(iperf Tx 50Mbit/s)	1275	1116

[3] Please contact Azurewave for the details

4. Mechanical Information

4.1 Mechanical Drawing



Unit: mm

5. Packaging Information

TBD