AW-PU552

NXP i.MX 8M Mini SoM with Wi-Fi 1x1 Connectivity

Datasheet

Rev. A

DF

(For Standard)

Features

Arm Cortex-A53 MPCore platform

- Quad symmetric Cortex®-A53 processors
- 32 KB L1 Instruction Cache
- 32 KB L1 Data Cache
- Media Processing Engine (MPE) with Arm® NEONTM technology supporting the Advanced Single Instruction Multiple Data architecture.
- Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
- Support of 64-bit Arm®v8-A architecture
- 512 KB unified L2 cache

Arm Cortex-M7 core platform

- Low power standby mode
- IoT features including Weave
- Manage IR or Wireless Remote
- ML inference applications (Enhanced for AW-PU552)
- 32 KB L1 Instruction Cache
- 32 KB L1 Data Cache
- 256 KB tightly coupled memory (TCM)

Audio

- S/PDIF input and output, including a raw Capture input mode
- Five synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces.
- One SAI with 4 Tx and 4 Rx lanes, two SAI with 2 Tx and 2 Rx lanes, and two SAI with 1 Tx and 1 Rx lanes.
- ASRC supports processing 32 audio channels, 4 context groups, 8 kHz to 384 kHz sample rate and 1/16 to 8x sample rate conversion ratio.
- Pulse Density Modulation (PDM) input

Connectivity

- One USB 2.0 OTG controllers with integrated PHY interface.(Spread spectrum clock support)
- One Ultra Secure Digital Host Controller (uSDHC) interface. SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100MB/sec. Also support for SDXC (extended capacity)
- One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588.

Graphic Processing Unit

- GC7000UL with OpenCL and Vulkan support
- 2 shader
- 99.8 million triangles/sec
- 0.6 giga pixel/sec
- 9.6 GFLOPs 32-bit/19.2 GFLOPs 16-bit
- Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL
- Core clock frequency of 600 MHz
- Shader clock frequency of 600 MHz

LCDIF Display Controller

- Support up to 1080p60 display through MIPI DSI

MIPI Interface

- 4-lane MIPI DSI interface
- 4-lane MIPI CSI interface

On board memory

- Ram: 1GB (8Gb) 16bit LPDDR4-3000.
- Flash: 4GB (32Gb) eMMC 5.1 / 16GB(128Gb) eMMC 5.1 (Option)

WLAN

- Two Universal Asynchronous Receiver/Transmitter (UART) modules.
- Three I2C modules.
- One ECSPI modules

WLAN

- Enhanced radar detection for long and short pulse radar
- Enhanced AGC scheme for DFS channel.
- 20/40/80Mhz coexistence with middle packet detection (GI detection) for enhanced CCA.
- 1 spatial stream STBC reception.
- LDPC transmission and reception for both 802.1 256 QAM (MCS 8, 9) modulation, optional support for 802.11ac MCS 9 in 20MHz using LDPC.
- Short guard interval.
- Temporal Ley Integrity Protocol (TKIP)/ Wired Equivalent Privacy (WEP)/ Advanced Encryption
- Standard (AES)/ Counter Mode/ CBC MAC Protocol (CCMP)
- Cipher Based Message Authentication Code (CMAC)/ WLAN Authentication and Privacy
- Infrastructure (WAPI).1n and 802.11ac.

- 1 antennas to support 1(Transmit) x 1(Receive) technology and Bluetooth
- High speed wireless connection up to 433.3Mbps transmit/receive PHY rate using 80MHz bandwidth
- Backward compatibility with legacy 802.11n/a/g/b technology.
- 20MHz bandwidth/ channel, 40MHz bandwidth/ channel, upper/ lower 20MHz packets in 40MHz channel, 20MHz duplicate legacy packets in 40MHz channel mode operation.
- 80MHz bandwidth/ channel, 4 positions of 20MHz packets in 80MHz channel, upper/ lower 40MHz packets in 80MHz channel, 20MHz quadruplicate legacy packets in 80MHz channel mode operation.
- Dynamic frequency selection (radar detection)

Bluetooth (continued)

- LE Secure Connection.
- LE Data Length Extension.
- 2 Mbps LE
- Direction Finding – Connectionless Angle of Departure (AoD).
- Direction Finding – Connection – oriented Angle of Arrival (AoA)

Bluetooth

- Baseband and radio BDR and EDR packet types 1Mbps (GFSK), 2Mbps (π /4 DQPSK), and 3Mbps (8DPSK).
- Fully qualified Bluetooth BT4.2 and support Bluetooth 5.Including Enhanced Data Rate (EDR) compliant for both 2Mbps and 3Mbps supported.
- High speed UART and PCM for Bluetooth.
- Fully functional Bluetooth baseband AFH, forward error correction, header error control,
- Access code correlation, CRC, encryption bit stream generation, and whitening.

- Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER).
- SCO/ eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement.
- Standard Bluetooth power saving mechanisms.
- Automatic ACL packet type selection.
- Full master and slave piconet support.
- Scatternet support.
- Enhanced Power Control (EPC).
- Channel Quality Driven Data Rate (CQDDR).
- Encryption (AES) support.
- Supports link layer topology to be master and slave (connects up to 16 links).
- LE Privacy 1.2

Revision History

Document NO: R2-3552-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2021/06/20	DCN023028	● Initial Version	Licheng Wang	Chihhao Liao

Table of Contents

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the NXP i.MX 8M Nano SoM with Wi-Fi 1x1 Connectivity --- **AW-PU552.** AW-PU552 is an advanced application processor designed for smart audio and smart home applications. It integrates a powerful CPU subsystem, advanced multi-format audio processing unit, a secured runtime environment and all major peripherals for versatile smart home applications.

The main system CPU is a quad-core ARM Cortex-A53 CPU with 32 KB L1 Instruction Cache and a 512KB unified L2 cache to improve system performance. Cortex-A53 CPU can run up to 1.5GHz.

Media Processing Engine (MPE) with Arm NEON technology supporting the Advanced Single Instruction Multiple Data architecture. Floating Point Unit (FPU) with support of the Arm VFPv4-D16 architecture. Also support of 64-bit Arm®v8-A architecture.

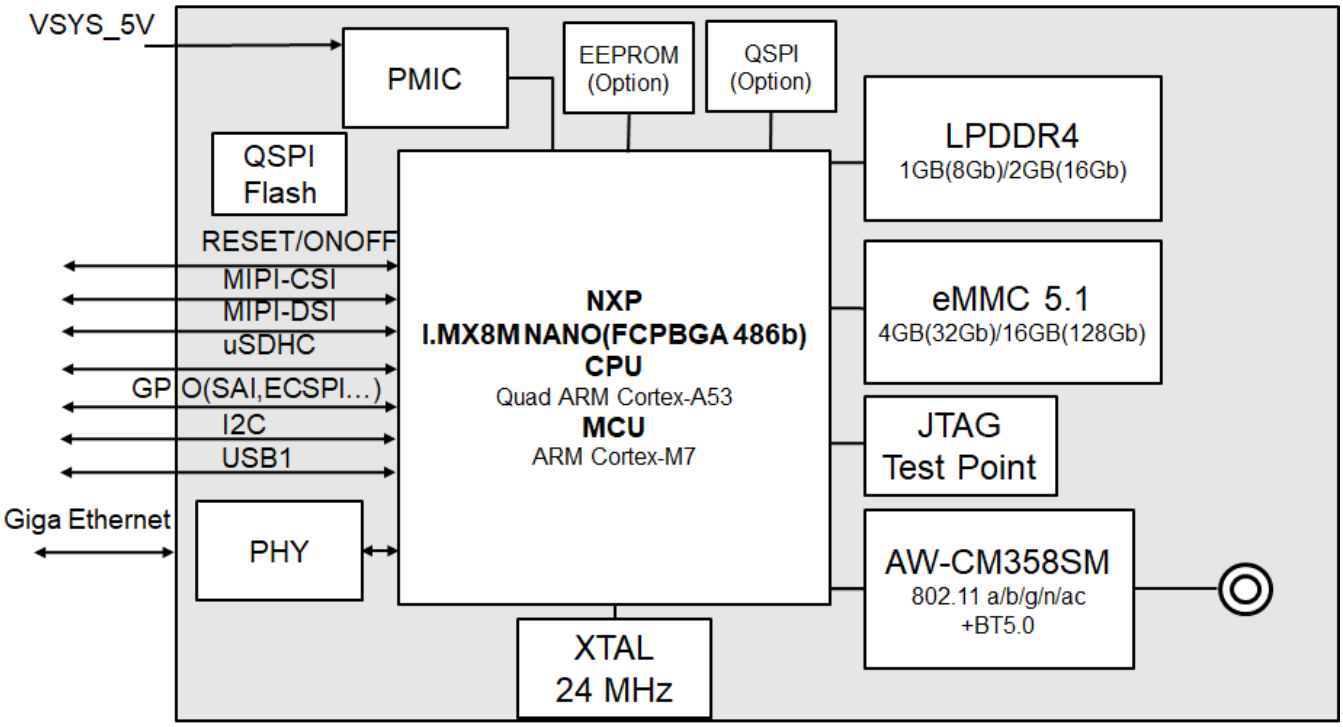
AW-PU552 integrates a wide range of standard audio input/output interfaces including multiple TDM, AC97, I2S and SPDIF. And Pulse Density Modulation (PDM) input. AW-PU552 module supports IEEE 802.11 a/b/g/n/ac 2.4GHz and 5GHz. It's also support BT5.0 with EDR and BLE. It has rich advanced peripheral interfaces, including USB 2.0 high-speed OTG port, SDIO controllers, UARTs, I2Cs, and PWMs.

The NXP i.MX 8M Nano SoC enabling application headroom for OEM features applications. The quad-core ARM Cortex-A53 architecture also supports advanced DSP algorithms for audio echo cancellation, beamforming, noise reduction, as well as audio post-processing, which eliminates the need for DSP hardware.

AW-PU552 module adopts NXP latest highly-integrated dual-band WLAN & Bluetooth SoC--- **88W8987**. All the other components are implemented by all means to reach the mechanical specification required.

1.2 Module Information

1.2.1 Block Diagram



AW-PU552 Block Diagram

1.2.2 Ordering information

Planned versions:

Model Name	Part Number of Main Chip	RAM Size	eMMC Size	Part Differentiator	Fusion	Flash & EEPROM
AW-PU552-6DA-0116-01	MIMX8MN6DVTJZAA	1GB(8Gb)	16GB(128Gb)	Full featured, 4x A53	N/A	√
AW-PU552-6DA-0116-02						x
AW-PU552-6DC-0116-01	MIMX8MN6DVTJZCA	1GB(8Gb)	16GB(128Gb)	No GPU, 4x A53	Immersiv3D w/ Dolby Atmos	√
AW-PU552-6DC-0116-02						x
AW-PU552-6DD-0116-01	MIMX8MN6DVTJZDA	1GB(8Gb)	16GB(128Gb)	No GPU, 4x A53	Immersiv3D w/ Dolby Atmos & DTS	√
AW-PU552-6DD-0116-02						x

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	NXP i.MX 8M Nano SoM with Wi-Fi 1x1 Connectivity
Major Chipset	NXP i.MX 8M Nano, NXP 88W8987
CPU Speed (frequency)	1.5GHz
USB	x1 USB 2.0 On-The-Go (OTG) interface
uSDHC	x1 Ultra Secure Digital Host Controller (uSDHC) interfaces
Ethernet	x1 Gigabit Ethernet controller with support for Energy Efficient, Ethernet (EEE),Ethernet AVB, and IEEE 1588
MIPI Interface	● 4-lane MIPI CSI interface ● 4-lane MIPI DSI interface
UART	x2 Universal Asynchronous Receiver/Transmitter (UART) modules
ECSPI	x1 ECSPI modules
I²C	x3 I²C modules
Audio Interface	● x1 S/PDIF input and output, including a new Raw Capture input mode ● x5 synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces ● x1 SAI with 4 Tx and 4 Rx lanes ● x2 SAI with 2 Tx and 2 Rx lanes ● x2 SAI with 1 Tx and 1 Rx lanes ● x1 Pulse Density Modulation (PDM) input
Ram	1GB(8Gb) 16bit LPDDR4-3000
Flash	4GB(32Gb) eMMC 5.1 / 16GB(128Gb) eMMC 5.1 (Option)
Dimension	85 X 50 X 4.2mm (typ)
Package	SMARC 2.1 short size
Antenna	I-PEX MHF4 Connector Receptacle (20449) Ant 1: Wi-Fi/BT Main
Weight	

1.3.2 WLAN

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>WLAN Standard</td><td>IEEE802.11 a/b/g/n/ac</td></tr>
<tr><td>Frequency Rage</td><td>2.4 GHz ISM Bands 2.412-2.472 GHz
5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe
5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe
5.47-5.725 GHz for Europe
5.725-5.825 GHz (FCC UNII-high band) for US/Canada</td></tr>
<tr><td>Modulation</td><td>802.11a/g/n/ac: OFDM
802.11b: CCK(11, 5.5Mbps), DQPSK(2Mbps), BPSK(1Mbps)</td></tr>
<tr><td>Number of Channels</td><td>2.4GHz
■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11
■ China, Australia, Most European Countries – 1 ~ 13
■ Japan, 1 ~ 14(CH14 only for 802.11b

5GHz
■ USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165</td></tr>
<tr><td>Output Power (Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps) @EVM<35%</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11g (54Mbps) @EVM≦-25 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-27 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-27 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps) @EVM ≦-25 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-27 dB</td><td>8</td><td>10</td><td>12</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-27 dB</td><td>8</td><td>10</td><td>12</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9) @EVM≦-32 dB</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>2.4G:
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)</td><td></td><td>-87</td><td>-84</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td></td><td>-73</td><td>-70</td><td>dBm</td></tr>
</table></td></tr>
</table>

	11n (HT20 MCS7)		-69	-66	dBm
	11n (HT40 MCS7)		-67	-64	dBm

5G:

	Min	Typ	Max	Unit
11a (54Mbps)		-71	-68	dBm
11n (HT20 MCS7)		-67	-64	dBm
11n (HT40 MCS7)		-63	-60	dBm
11ac (VHT80 MCS9)		-55	-52	dBm

* If you have any certification questions about output power please contact FAE directly.

*** RF spec only for reference.**

1.3.3 Bluetooth

Features	**Description**
Bluetooth Standard	BT5.0+Enhanced Data Rate (EDR)
Frequency Rage	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: 4-DQPSK Payload 3M: 8DPSK

Output Power

	Min	Typ	Max	Unit
BDR	0	2	4	dBm
EDR	-4	-1	1	dBm
Low Energy	0	2	4	dBm

Receiver Sensitivity

BT Sensitivity (BER<0.1%)

	Min	Typ	Max	Unit
GFSK		-88	-86	dBm
4-DQPSK		-88	-86	dBm
8DPSK		-80	-78	dBm

*** RF spec only for reference.**

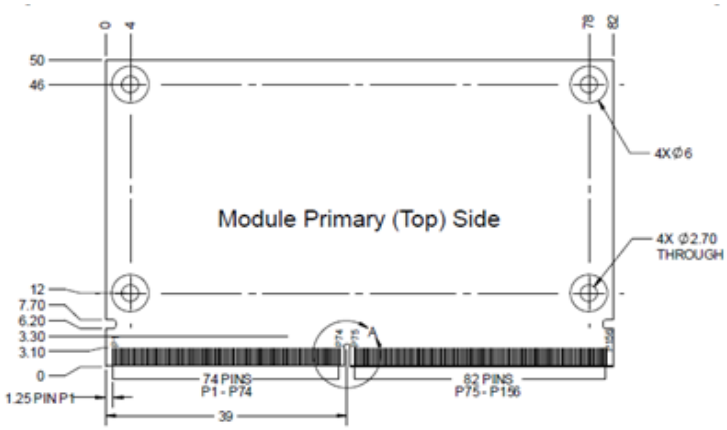
1.3.4 Operating Conditions

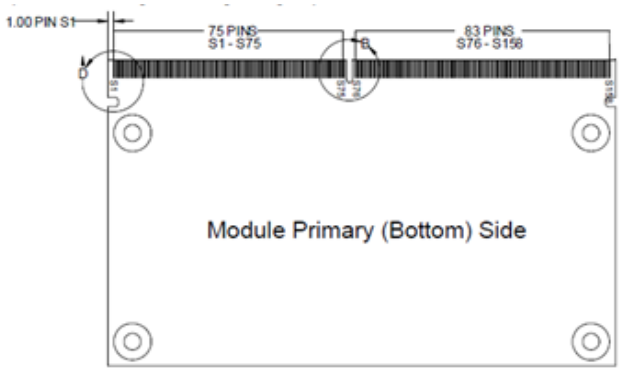
Features	Description
Operating Conditions	
Voltage	VBAT: 5V +/-10%
Operating Temperature	0℃ to +70℃[1]
Operating Humidity	less than 85%R.H.
Storage Temperature	-25℃ to +85℃
Storage Humidity	less than 60%R.H.
ESD Protection	
Human Body Model	1KV per JS-001-2017
Changed Device Model	250V per JS-002-2018

[1] Based on temperature Tj of i.MX 8M Nano is 0 ~ +95℃. If you have questions, please contact your AzureWave FAE.

2. Pin Definition

2.1 Pin Map





2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
P1	SMB_ALERT	SMBus Alert# (Interrupt) Signal	1.8-5V	I OD CMOS
P2	GND_P2	Ground		Ground
P3	CSI1_CK+	MIPI-CSI Data Lane		I
P4	CSI1_CK-	MIPI-CSI Data Lane		I
P5	NC_GBE1_SDP	Floating Pin, No connect to anything.		Floating
P6	NC_GBE0_SDP	Floating Pin, No connect to anything.		Floating
P7	CSI1_RX0+	MIPI-CSI Data Lane		I
P8	CSI1_RX0-	MIPI-CSI Data Lane		I
P9	GND_P9	Ground		Ground
P10	CSI1_RX1+	MIPI-CSI Data Lane		I
P11	CSI1_RX1-	MIPI-CSI Data Lane		I
P12	GND_P12	Ground		Ground
P13	CSI1_RX2+	MIPI-CSI Data Lane		I
P14	CSI1_RX2-	MIPI-CSI Data Lane		I
P15	GND_P15	Ground		Ground
P16	CSI1_RX3+	MIPI-CSI Data Lane		I
P17	CSI1_RX3-	MIPI-CSI Data Lane		I
P18	GND_P18	Ground		Ground
P19	GBE0_MDI3-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P20	GBE0_MDI3+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet		I/O

		implementations		
P21	GBE0_LINK100#	Link Speed Indication LED for GBE0 100Mbps	3.3V	O
P22	GBE0_LINK1000#	Link Speed Indication LED for GBE0 1000Mbps	3.3V	O
P23	GBE0_MDI2-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P24	GBE0_MDI2+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P25	GBE0_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	3.3V	O
P26	GBE0_MDI1-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P27	GBE0_MDI1+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P28	NC_GBE0_CTREF	Floating Pin, No connect to anything.		Floating
P29	GBE0_MDI0-	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P30	GBE0_MDI0+	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations		I/O
P31	NC_SPI0_CS1#	Floating Pin, No connect to anything.		Floating
P32	GND_P32	Ground		Ground
P33	SDIO_WP	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	1.8/3.3V	I
P34	SDIO_CMD	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	1.8/3.3V	I/O
P35	SDIO_CD#	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	1.8/3.3V	I
P36	SDIO_CK	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	1.8/3.3V	O

P37	SDIO_PWR_EN	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	3.3V	O
P38	GND_P38	Ground		Ground
P39	SDIO_D0	SDIO Data lines. These signals operate in push-pull mode.	1.8/3.3V	I/O
P40	SDIO_D1	SDIO Data lines. These signals operate in push-pull mode.	1.8/3.3V	I/O
P41	SDIO_D2	SDIO Data lines. These signals operate in push-pull mode.	1.8/3.3V	I/O
P42	SDIO_D3	SDIO Data lines. These signals operate in push-pull mode.	1.8/3.3V	I/O
P43	SPI0_CS0#	SPI0 Master Chip Select 0	1.8V	O
P44	SPI0_CK	SPI0 Clock	1.8V	O
P45	SPI0_DIN	SPI0 Master input / Slave output	1.8V	I
P46	SPI0_DO	SPI0 Master output / Slave input	1.8V	O
P47	GND_P47	Ground		Ground
P48	NC_SATA_TX+	Floating Pin, No connect to anything.		Floating
P49	NC_SATA_TX-	Floating Pin, No connect to anything.		Floating
P50	GND_P50	Ground		Ground
P51	NC_SATA_RX+	Floating Pin, No connect to anything.		Floating
P52	NC_SATA_RX-	Floating Pin, No connect to anything.		Floating
P53	GND_P53	Ground		Ground
P54	QSPI_CS0#	floating, if internal QSPI flash is used	1.8V	O CMOS
P55	NC_SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	Floating Pin, No connect to anything.		Floating
P56	QSPI_CK	floating, if internal QSPI flash is used	1.8V	O CMOS
P57	QSPI_IO_1	floating, if internal QSPI flash is used	1.8V	I/O CMOS
P58	QSPI_IO_0	floating, if internal QSPI flash is used	1.8V	I/O CMOS
P59	GND_P59	Ground		Ground
P60	USB0+	USB Differential Data Pairs for Port 0		I/O
P61	USB0-	USB Differential Data Pairs for Port 0		I/O

P62	USB0_EN_OC#	USB Over-Current Sense for Port 0. 500mA Max	3.3V	I/O OD CMOS
P63	USB0_VBUS_DET	Isolated with a 30K resistor inside the module	USB VBUS 5V	USB VBUS 5V
P64	NC_USB0_OTG_ID	Input Pin to Announce OTG Device Insertion on USB Port	3.3V	I CMOS
P65	USB1+	Floating Pin, No connect to anything.		Floating
P66	USB1-	Floating Pin, No connect to anything.		Floating
P67	USB1_EN_OC#	Floating Pin, No connect to anything.		Floating
P68	GND_P68	Ground		Ground
P69	USB2+	Floating Pin, No connect to anything.		Floating
P70	USB2-	Floating Pin, No connect to anything.		Floating
P71	USB2_EN_OC#	Floating Pin, No connect to anything.		Floating
P72	RSVD_EARC_P_UTIL	Floating Pin, No connect to anything.		Floating
P73	RSVD_EARC_N_HPD	Floating Pin, No connect to anything.		Floating
P74	USB3_EN_OC#	Floating Pin, No connect to anything.		Floating
P75	NC_PCIE_A_RST#	Floating Pin, No connect to anything.		Floating
P76	USB4_EN_OC#	Floating Pin, No connect to anything.		Floating
P77	NC_PCIE_B_CKREQ#	Floating Pin, No connect to anything.		Floating
P78	NC_PCIE_A_CKREQ#	Floating Pin, No connect to anything.		Floating
P79	GND_P79	Ground		Ground
P80	NC_PCIE_C_REFCK+	Floating Pin, No connect to anything.		Floating
P81	NC_PCIE_C_REFCK-	Floating Pin, No connect to anything.		Floating
P82	GND_P82	Ground		Ground
P83	NC_PCIE_A_REFCK+	Floating Pin, No connect to anything.		Floating
P84	NC_PCIE_A_REFCK-	Floating Pin, No connect to anything.		Floating
P85	GND_P85	Ground		Ground
P86	NC_PCIE_A_RX+	Floating Pin, No connect to anything.		Floating
P87	NC_PCIE_A_RX-	Floating Pin, No connect to anything.		Floating

P88	GND_P88	Ground		Ground
P89	NC_PCIE_A_TX+	Floating Pin, No connect to anything.		Floating
P90	NC_PCIE_A_TX-	Floating Pin, No connect to anything.		Floating
P91	GND_P91	Ground		Ground
P92	HDMI_D2+ / DP1_LANE0+	Floating Pin, No connect to anything.		Floating
P93	HDMI_D2- / DP1_LANE0-	Floating Pin, No connect to anything.		Floating
P94	GND_P94	Ground		Ground
P95	HDMI_D1+ / DP1_LANE1+	Floating Pin, No connect to anything.		Floating
P96	HDMI_D1- / DP1_LANE1-	Floating Pin, No connect to anything.		Floating
P97	GND_P97	Ground		Ground
P98	HDMI_D0+ / DP1_LANE2+	Floating Pin, No connect to anything.		Floating
P99	HDMI_D0- / DP1_LANE2-	Floating Pin, No connect to anything.		Floating
P100	GND_P100	Ground		Ground
P101	HDMI_CK+ / DP1_LANE3+	Floating Pin, No connect to anything.		Floating
P102	HDMI_CK- / DP1_LANE3-	Floating Pin, No connect to anything.		Floating
P103	GND_P103	Ground		Ground
P104	HDMI_HPD / DP1_HPD	Floating Pin, No connect to anything.		Floating
P105	HDMI_CTRL_CK / DP1_AUX+	Floating Pin, No connect to anything.		Floating
P106	HDMI_CTRL_DAT / DP1_AUX-	Floating Pin, No connect to anything.		Floating
P107	NC_DP1_AUX_SEL	Floating Pin, No connect to anything.		Floating
P108	GPIO0 / CAM0_PWR#	GPIO	1.8V	I/O
P109	GPIO1 / CAM1_PWR#	GPIO	1.8V	I/O
P110	GPIO2 / CAM0_RST#	GPIO	1.8V	I/O
P111	GPIO3 / CAM1_RST#	GPIO	1.8V	I/O
P112	GPIO4 / HDA_RST#	GPIO	1.8V	I/O
P113	GPIO5 / PWM_OUT	GPIO5 PWM capability	1.8V	I/O

P114	GPIO6 / TACHIN	GPIO6 Tachin capability	1.8V	I/O
P115	GPIO7	GPIO	1.8V	I/O
P116	GPIO8	GPIO	1.8V	I/O
P117	GPIO9	GPIO	1.8V	I/O
P118	GPIO10	GPIO	1.8V	I/O
P119	GPIO11	GPIO	1.8V	I/O
P120	GND_P120	Ground		Ground
P121	I2C_PM_CK	Power management I2C bus CLK	1.8V	I/O
P122	I2C_PM_DAT	Power management I2C bus DATA	1.8V	I/O
P123	BOOT_SEL0#	IMX8MN BOOT mode select BOOT_MODE0. 10 K ohms internal pull up	1.8V	I
P124	BOOT_SEL1#	IMX8MN BOOT mode select BOOT_MODE1. 10 K ohms internal pull up	1.8V	I
P125	BOOT_SEL2#	IMX8MN BOOT mode select BOOT_MODE2. 100 K ohms internal pull down	1.8V	I
P126	RESET_OUT#	General purpose reset output to Carrier Board.	1.8V	O
P127	RESET_IN#	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise.	1.8-5V	I
P128	POWER_BTN#	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module	1.8-5V	I
P129	NC_SER0_TX	Floating Pin, No connect to anything.		Floating
P130	NC_SER0_RX	Floating Pin, No connect to anything.		Floating
P131	NC_SER0_RTS#	Floating Pin, No connect to anything.		Floating
P132	NC_SER0_CTS#	Floating Pin, No connect to anything.		Floating
P133	GND_P133	Ground		Ground
P134	SER1_TX	Asynchronous Serial Data Output Port 1	1.8V	O
P135	SER1_RX	Asynchronous Serial Data Input Port 1	1.8V	I
P136	SER2_TX	Asynchronous Serial Data Output Port 2	1.8V	O
P137	SER2_RX	Asynchronous Serial Data Input Port 2	1.8V	I
P138	SER2_RTS#	Request to Send Handshake Line for Port 1	1.8V	O

P139	SER2_CTS#	Clear to Send Handshake Line for Port 1	1.8V	I
P140	SER3_TX	Asynchronous Serial Data Output Port 3	1.8V	O
P141	SER3_RX	Asynchronous Serial Data Input Port 3	1.8V	I
P142	GND_P142	Ground		Ground
P143	CAN0_TX	Floating Pin, No connect to anything.		Floating
P144	CAN0_RX	Floating Pin, No connect to anything.		Floating
P145	CAN1_TX	Floating Pin, No connect to anything.		Floating
P146	CAN1_RX	Floating Pin, No connect to anything.		Floating
P147	VDD_IN_P147	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P148	VDD_IN_P148	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P149	VDD_IN_P149	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P150	VDD_IN_P150	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P151	VDD_IN_P151	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P152	VDD_IN_P152	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P153	VDD_IN_P153	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P154	VDD_IN_P154	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P155	VDD_IN_P155	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
P156	VDD_IN_P156	Module power input voltage - 3.0V min to 5.25V max	3-5.25V	Power In
S1	CSI1_TX+ / I2C_CAM1_CK	CAM1 I2C clock for serial camera data support link.	1.8V	I/O
S2	CSI1_TX- / I2C_CAM1_DAT	CAM1 I2C clock for serial camera data support link.	1.8V	I/O
S3	GND_S3	Ground		Ground
S4	RSVD_PMIC_32K_OUT_1V8_CEC	Floating Pin, No connect to anything.		Floating
S5	CSI0_TX- / I2C_CAM0_CK	Floating Pin, No connect to anything.		Floating
S6	CAM_MCK	Master clock output. Connect to SMARC MIPI-CSI Feature Connector Pin 22 internally.	1.8V	O
S7	CSI0_TX+ / I2C_CAM0_DAT	Floating Pin, No connect to anything.		Floating
S8	CSI0_CK+	Floating Pin, No connect to anything.		Floating

S9	CSI0_CK-	Floating Pin, No connect to anything.		Floating
S10	GND_S10	Ground		Ground
S11	CSI0_RX0+	Floating Pin, No connect to anything.		Floating
S12	CSI0_RX0-	Floating Pin, No connect to anything.		Floating
S13	GND_S13	Ground		Ground
S14	CSI0_RX1+	Floating Pin, No connect to anything.		Floating
S15	CSI0_RX1-	Floating Pin, No connect to anything.		Floating
S16	GND_S16	Ground		Ground
S17	GBE1_MDI0+	Floating Pin, No connect to anything.		Floating
S18	GBE1_MDI0-	Floating Pin, No connect to anything.		Floating
S19	GBE1_LINK100#	Floating Pin, No connect to anything.		Floating
S20	GBE1_MDI1+	Floating Pin, No connect to anything.		Floating
S21	GBE1_MDI1-	Floating Pin, No connect to anything.		Floating
S22	GBE1_LINK1000#	Floating Pin, No connect to anything.		Floating
S23	GBE1_MDI2+	Floating Pin, No connect to anything.		Floating
S24	GBE1_MDI2-	Floating Pin, No connect to anything.		Floating
S25	GND_S25	Ground		Ground
S26	GBE1_MDI3+	Floating Pin, No connect to anything.		Floating
S27	GBE1_MDI3-	Floating Pin, No connect to anything.		Floating
S28	NC_GBE1_CTREF	Floating Pin, No connect to anything.		Floating
S29	NC_PCIE_D_TX+	Floating Pin, No connect to anything.		Floating
S30	NC_PCIE_D_TX-	Floating Pin, No connect to anything.		Floating
S31	GBE1_LINK_ACT#	Floating Pin, No connect to anything.		Floating
S32	NC_PCIE_D_RX+	Floating Pin, No connect to anything.		Floating
S33	NC_PCIE_D_RX-	Floating Pin, No connect to anything.		Floating
S34	GND_S34	Ground		Ground

S35	USB4+	Floating Pin, No connect to anything.		Floating
S36	USB4-	Floating Pin, No connect to anything.		Floating
S37	USB3_VBUS_DET	Floating Pin, No connect to anything.		Floating
S38	AUDIO_MCK	Master Clock Output to I2S Codec(s)	1.8V	O CMOS
S39	I2S0_LRCK	I2S0 Left & Right Synchronization Clock	1.8V	I/O CMOS
S40	I2S0_SDOUT	I2S0 Digital Audio Output	1.8V	O CMOS
S41	I2S0_SDIN	I2S0 Digital Audio Input	1.8V	I CMOS
S42	I2S0_CK	I2S0 Digital Audio Clock	1.8V	I/O CMOS
S43	NC_ESPI_ALERT0#	Floating Pin, No connect to anything.		Floating
S44	NC_ESPI_ALERT1#	Floating Pin, No connect to anything.		Floating
S45	NC_MDIO_CLK	Floating Pin, No connect to anything.		Floating
S46	NC_MDIO_DAT	Floating Pin, No connect to anything.		Floating
S47	GND_S47	Ground		Ground
S48	I2C_GP_CK	General Purpose I2C Clock Signal.	1.8V	I/O
S49	I2C_GP_DAT	General Purpose I2C Data Signal.	1.8V	I/O
S50	HDA_SYNC / I2S2_LRCK	I2S2 Left & Right Synchronization Clock.	1.8V	I/O CMOS
S51	HDA_SDO / I2S2_SDOUT	I2S2 Digital Audio Output	1.8V	O CMOS
S52	HDA_SDI / I2S2_SDIN	I2S2 Digital Audio Input	1.8V	I CMOS
S53	HDA_CK / I2S2_CK	I2S2 Digital Audio Clock.	1.8V	I/O CMOS
S54	NC_SATA_ACT#	Floating Pin, No connect to anything.		Floating
S55	USB5_EN_OC#	Floating Pin, No connect to anything.		Floating
S56	QSPI_IO_2	floating, if internal QSPI flash is used	1.8V	I/O CMOS
S57	QSPI_IO_3	floating, if internal QSPI flash is used	1.8V	I/O CMOS
S58	NC_ESPI_RESET#	Floating Pin, No connect to anything.		Floating
S59	USB5+	Floating Pin, No connect to anything.		Floating
S60	USB5-	Floating Pin, No connect to anything.		Floating

S61	GND_S61	Ground		Ground
S62	USB3_SSTX+	Floating Pin, No connect to anything.		Floating
S63	USB3_SSTX-	Floating Pin, No connect to anything.		Floating
S64	GND_S64	Ground		Ground
S65	USB3_SSRX+	Floating Pin, No connect to anything.		Floating
S66	USB3_SSRX-	Floating Pin, No connect to anything.		Floating
S67	GND_S67	Ground		Ground
S68	USB3+	Floating Pin, No connect to anything.		Floating
S69	USB3-	Floating Pin, No connect to anything.		Floating
S70	GND_S70	Ground		Ground
S71	NC_USB2_SSTX+	Floating Pin, No connect to anything.		Floating
S72	NC_USB2_SSTX-	Floating Pin, No connect to anything.		Floating
S73	GND_S73	Ground		Ground
S74	NC_USB2_SSRX+	Floating Pin, No connect to anything.		Floating
S75	NC_USB2_SSRX-	Floating Pin, No connect to anything.		Floating
S76	NC_PCIE_B_RST#	Floating Pin, No connect to anything.		Floating
S77	NC_PCIE_C_RST#	Floating Pin, No connect to anything.		Floating
S78	NC_PCIE_C_RX+	Floating Pin, No connect to anything.		Floating
S79	NC_PCIE_C_RX-	Floating Pin, No connect to anything.		Floating
S80	GND_S80	Ground		Ground
S81	NC_PCIE_C_TX+	Floating Pin, No connect to anything.		Floating
S82	NC_PCIE_C_TX-	Floating Pin, No connect to anything.		Floating
S83	GND_S83	Ground		Ground
S84	NC_PCIE_B_REFCK+	Floating Pin, No connect to anything.		Floating
S85	NC_PCIE_B_REFCK-	Floating Pin, No connect to anything.		Floating
S86	GND_S86	Ground		Ground

S87	NC_PCIE_B_RX+	Floating Pin, No connect to anything.		Floating
S88	NC_PCIE_B_RX-	Floating Pin, No connect to anything.		Floating
S89	GND_S89	Ground		Ground
S90	NC_PCIE_B_TX+	Floating Pin, No connect to anything.		Floating
S91	NC_PCIE_B_TX-	Floating Pin, No connect to anything.		Floating
S92	GND_S92	Ground		Ground
S93	NC_DP0_LANE0+	Floating Pin, No connect to anything.		Floating
S94	NC_DP0_LANE0-	Floating Pin, No connect to anything.		Floating
S95	NC_DP0_AUX_SEL	Floating Pin, No connect to anything.		Floating
S96	NC_DP0_LANE1+	Floating Pin, No connect to anything.		Floating
S97	NC_DP0_LANE1-	Floating Pin, No connect to anything.		Floating
S98	NC_DP0_HPD	Floating Pin, No connect to anything.		Floating
S99	NC_DP0_LANE2+	Floating Pin, No connect to anything.		Floating
S100	NC_DP0_LANE2-	Floating Pin, No connect to anything.		Floating
S101	GND_S101	Ground		Ground
S102	NC_DP0_LANE3+	Floating Pin, No connect to anything.		Floating
S103	NC_DP0_LANE3-	Floating Pin, No connect to anything.		Floating
S104	USB3_OTG_ID	Floating Pin, No connect to anything.		Floating
S105	NC_DP0_AUX+	Floating Pin, No connect to anything.		Floating
S106	NC_DP0_AUX-	Floating Pin, No connect to anything.		Floating
S107	NC_LCD1_BKLT_EN	Floating Pin, No connect to anything.		Floating
S108	LVDS1_CK+	Floating Pin, No connect to anything.		Floating
S109	LVDS1_CK-	Floating Pin, No connect to anything.		Floating
S110	GND_S110	Ground		Ground
S111	LVDS1_0+	Floating Pin, No connect to anything.		Floating
S112	LVDS1_0-	Floating Pin, No connect to anything.		Floating

S113	NC_eDP1_HPD	Floating Pin, No connect to anything.		Floating
S114	LVDS1_1+	Floating Pin, No connect to anything.		Floating
S115	LVDS1_1-	Floating Pin, No connect to anything.		Floating
S116	NC_LCD1_VDD_EN	Floating Pin, No connect to anything.		Floating
S117	LVDS1_2+	Floating Pin, No connect to anything.		Floating
S118	LVDS1_2-	Floating Pin, No connect to anything.		Floating
S119	GND_S119	Ground		Ground
S120	LVDS1_3+	Floating Pin, No connect to anything.		Floating
S121	LVDS1_3-	Floating Pin, No connect to anything.		Floating
S122	NC_LCD1_BKLT_PWM	Floating Pin, No connect to anything.		Floating
S123	GPIO13	GPIO	1.8V	I/O
S124	GND_S124	Ground		Ground
S125	DSI0_D0+	Primary DSI Panel Differential Pair Data Lines		I/O
S126	DSI0_D0-	Primary DSI Panel Differential Pair Data Lines		I/O
S127	LCD0_BKLT_EN	Primary Panel Backlight Enable	1.8V	O
S128	DSI0_D1+	Primary DSI Panel Differential Pair Data Lines		O
S129	DSI0_D1-	Primary DSI Panel Differential Pair Data Lines		O
S130	GND_S130	Ground		Ground
S131	DSI0_D2+	Primary DSI Panel Differential Pair Data Lines		O
S132	DSI0_D2-	Primary DSI Panel Differential Pair Data Lines		O
S133	LCD0_VDD_EN	Primary Panel Power Enable	1.8V	O
S134	DSI0_CLK+	Primary DSI Panel Differential Pair Clock Lines		O
S135	DSI0_CLK-	Primary DSI Panel Differential Pair Clock Lines		O
S136	GND_S136	Ground		Ground
S137	DSI0_D3+	Primary DSI Panel Differential Pair Data Lines		O
S138	DSI0_D3-	Primary DSI Panel Differential Pair Data Lines		O

S139	I2C_LCD_CK	DDC Clock Line Used for Flat Panel Detection and Control.	1.8V	I/O
S140	I2C_LCD_DAT	DDC Data Line Used for Flat Panel Detection and Control.	1.8V	I/O
S141	LCD0_BKLT_PWM	Primary Panel Brightness Control	1.8V	O
S142	GPIO12	Floating Pin, No connect to anything.		Floating
S143	GND_S143	Ground		Ground
S144	NC_eDP0_HPD	Floating Pin, No connect to anything.		Floating
S145	WDT_TIME_OUT#	Watch-Dog-Timer Output, low active	1.8V	O
S146	NC_PCIE_WAKE#	Floating Pin, No connect to anything.		Floating
S147	NC_VDD_RTC	Floating Pin, No connect to anything.		Floating
S148	LID#	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the Module.	1.8-5V	I
S149	SLEEP#	Sleep indicator from Carrier Board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	1.8-5V	I
S150	VIN_PWR_BAD#	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.	VDD_IN	I
S151	CHARGING#	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	1.8-5V	I
S152	CHARGER_PRSNT#	Held low by Carrier if DC input for battery charger is present.	1.8-5V	I
S153	CARRIER_STBY#	The Module shall drive this signal low when the system is in a standby power state.	1.8V	O
S154	CARRIER_PWR_ON	Carrier Board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	1.8V	O
S155	FORCE_RECOV#	Low on this pin allows nonprotected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module.	1.8V	I
S156	BATLOW#	Battery low indication to Module. Carrier to float the line in inactive state.	1.8-5V	I
S157	TEST#	IMX8MN BOOT mode select BOOT_MODE3. 100 K ohms internal pull down	1.8-5V	I
S158	GND_S158	Ground		Ground

2.3 Pin Multiplexing Tables[2]

Multiple usage pins are used to conserve pin consumption for different features. The AW-PU552 devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be used as a GPIO pin as well.

Table 1 (SD)

Pin Name	Default	FUNC0	FUNC1	FUNC2
SD1_STROBE	gpio2.IO[11]	usdhc1.STROBE		UART3_CTS_B
SD2_CD_B	gpio2.IO[12]	usdhc2.CD_B		
SD2_CLK	gpio2.IO[13]	usdhc2.CLK	SAI5_RX_SYNC	SAI5_MCLK
SD2_CMD	gpio2.IO[14]	usdhc2.CMD	SAI5_RX_BCLK	PDM_CLK
SD2_DATA0	gpio2.IO[15]	usdhc2.DATA0	SAI5_RX_DATA[0]	PDM_BIT[0]
SD2_DATA1	gpio2.IO[16]	usdhc2.DATA1	SAI5_TX_SYNC	PDM_BIT[1]
SD2_DATA2	gpio2.IO[17]	usdhc2.DATA2	SAI5_TX_BCLK	PDM_BIT[2]
SD2_DATA3	gpio2.IO[18]	usdhc2.DATA3	SAI5_TX_DATA[0]	PDM_BIT[3]
SD2_RESET_B	gpio2.IO[19]	usdhc2.RESET_B		
SD2_WP	gpio2.IO[20]	usdhc2.WP		

Table 1 (SD) continued

Pin Name	FUNC3	FUNC4	FUNC5	FUNC6	FUNC7
SD1_STROBE	I2C3_SDA	UART3_CTS_B	gpio2.IO[11]		
SD2_CD_B			gpio2.IO[12]		
SD2_CLK	UART4_RX	SAI5_MCLK	gpio2.IO[13]	reserved	reserved
SD2_CMD	UART4_TX	PDM_CLK	gpio2.IO[14]	reserved	reserved
SD2_DATA0	UART2_RX	PDM_BIT[0]	gpio2.IO[15]	reserved	reserved
SD2_DATA1	UART2_TX	PDM_BIT[1]	gpio2.IO[16]	reserved	reserved
SD2_DATA2	SPDIF_OUT	PDM_BIT[2]	gpio2.IO[17]	reserved	reserved

[2] For program GPIOs, please confirm with AZW software team.

SD2_DATA3	SPDIF_IN	PDM_BIT[3]	gpio2.IO[18]	reserved	
SD2_RESET_B			gpio2.IO[19]	reserved	
SD2_WP			gpio2.IO[20]	CORESIGHT_EVENTI	reserved

Table 2 (GPIOs)

Pin Name	Default	FUNC0	FUNC1	FUNC2
GPIO1_IO01	gpio1.IO[1]	gpio1.IO[1]	pwm1.OUT	
GPIO1_IO05	gpio1.IO[5]	gpio1.IO[5]	m4.NMI	
GPIO1_IO06	gpio1.IO[6]	gpio1.IO[6]	enet1.MDC	
GPIO1_IO07	gpio1.IO[7]	gpio1.IO[7]	enet1.MDIO	
GPIO1_IO08	gpio1.IO[8]	gpio1.IO[8]		PWM1_OUT
GPIO1_IO09	gpio1.IO[9]	gpio1.IO[9]		PWM2_OUT
GPIO1_IO10	gpio1.IO[10]	gpio1.IO[10]		PWM3_OUT
GPIO1_IO11	gpio1.IO[11]	gpio1.IO[11]	PWM2_OUT	
GPIO1_IO12	gpio1.IO[12]	gpio1.IO[12]	usb1.OTG_PWR	
GPIO1_IO13	gpio1.IO[13]	gpio1.IO[13]	usb1.OTG_OC	
GPIO1_IO14	gpio1.IO[14]	gpio1.IO[14]		
GPIO1_IO15	gpio1.IO[15]	gpio1.IO[15]		

Table 2 (GPIOs) continued

Pin Name	FUNC4	FUNC5	FUNC6	FUNC7
GPIO1_IO01		anamix.REF_CLK_24M	reserved	reserved
GPIO1_IO05		ccmsrcgpcmix.PMIC_READY	reserved	reserved
GPIO1_IO06		usdhc1.CD_B	reserved	reserved
GPIO1_IO07		usdhc1.WP	reserved	reserved
GPIO1_IO08		usdhc2.RESET_B	reserved	reserved
GPIO1_IO09	usdhc3.RESET_B	sdma2.XT_EVENT[0]	reserved	reserved
GPIO1_IO10				reserved
GPIO1_IO11	usdhc3.VSELECT	ccmsrcgpcmix.PMIC_READY	reserved	reserved
GPIO1_IO12		sdma2.EXT_EVENT[1]	reserved	reserved
GPIO1_IO13		pwm2.OUT	reserved	reserved
GPIO1_IO14	usdhc3.CD_B	pwm3.OUT	reserved	reserved
GPIO1_IO15	usdhc3.WP	pwm4.OUT	reserved	reserved

Table 3 (SAI5)

Pin Name	Default	FUNC0	FUNC3
SAI5_RXFS	gpio3.IO[19]	sai5.RX_SYNC	
SAI5_RXC	gpio3.IO[20]	sai5.RX_BCLK	
SAI5_RXD0	gpio3.IO[21]	sai5.RX_DATA[0]	
SAI5_RXD1	gpio3.IO[22]	sai5.RX_DATA[1]	sai5.TX_SYNC
SAI5_RXD2	gpio3.IO[23]	sai5.RX_DATA[2]	sai5.TX_BCLK
SAI5_RXD3	gpio3.IO[24]	sai5.RX_DATA[3]	sai5.TX_DATA[0]
SAI5_MCLK	gpio3.IO[25]	sai5.MCLK	

Table 3 (SAI5) continued

Pin Name	FUNC4	FUNC5	FUNC6	FUNC7
SAI5_RXFS		gpio3.IO[19]		reserved
SAI5_RXC	pdm.CLK	gpio3.IO[20]		reserved
SAI5_RXD0	pdm.BIT_STREAM[0]	gpio3.IO[21]		
SAI5_RXD1	pdm.BIT_STREAM[1]	gpio3.IO[22]		
SAI5_RXD2	pdm.BIT_STREAM[2]	gpio3.IO[23]		
SAI5_RXD3	pdm.BIT_STREAM[3]	gpio3.IO[24]		
SAI5_MCLK		gpio3.IO[25]	reserved	

Table 5 (SAI2)

Pin Name	Default	FUNC0	FUNC1	FUNC2
SAI2_RXFS	gpio4.IO[21]	sai2.RX_SYNC	sai5.TX_SYNC	sai5.TX_DATA[1]
SAI2_RXC	gpio4.IO[22]	sai2.RX_BCLK	sai5.TX_BCLK	
SAI2_RXD0	gpio4.IO[23]	sai2.RX_DATA[0]	sai5.TX_DATA[0]	
SAI2_TXFS	gpio4.IO[24]	sai2.TX_SYNC	sai5.TX_DATA[1]	
SAI2_TXC	gpio4.IO[25]	sai2.TX_BCLK	sai5.TX_DATA[2]	
SAI2_TXD0	gpio4.IO[26]	sai2.TX_DATA[0]	sai5.TX_DATA[3]	
SAI2_MCLK	gpio4.IO[27]	sai2.MCLK	sai5.MCLK	

Table 5 (SAI2) continued

Pin Name	FUNC3	FUNC4	FUNC5	FUNC6	FUNC7
SAI2_RXFS	sai2.RX_DATA[1]	uart1.TX	gpio4.IO[21]	PDM_BIT [2]	reserved
SAI2_RXC		uart1.RX	gpio4.IO[22]	PDM_BIT [1]	reserved
SAI2_RXD0	sai2.TX_DATA[1]	uart1.RTS_B	gpio4.IO[23]	PDM_BIT [3]	reserved
SAI2_TXFS	sai2.TX_DATA[1]	uart1.CTS_B	gpio4.IO[24]	PDM_BIT [2]	reserved

SAI2_TXC			gpio4.IO[25]	PDM_BIT [1]	reserved
SAI2_TXD0			gpio4.IO[26]		reserved
SAI2_MCLK			gpio4.IO[27]	SAI3_MCLK	reserved

Table 6 (SAI3, SPDIF)

Pin Name	Default	FUNC0	FUNC1	FUNC2
SAI3_RXFS	gpio4.IO[28]	sai3.RX_SYNC	gpt1.CAPTURE1	sai5.RX_SYNC
SAI3_RXC	gpio4.IO[29]	sai3.RX_BCLK	gpt1.CLK	sai5.RX_BCLK
SAI3_RXD	gpio4.IO[30]	sai3.RX_DATA[0]	gpt1.COMPARE1	sai5.RX_DATA[0]
SAI3_TXFS	gpio4.IO[31]	sai3.TX_SYNC	gpt1.CAPTURE2	sai5.RX_DATA[1]
SAI3_TXC	gpio5.IO[0]	sai3.TX_BCLK	gpt1.COMPARE2	sai5.RX_DATA[2]
SAI3_TXD	gpio5.IO[1]	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]
SAI3_MCLK	gpio5.IO[2]	sai3.MCLK	pwm4.OUT	sai5.MCLK
SPDIF_TX	gpio5.IO[3]	spdif1.OUT	pwm3.OUT	
SPDIF_RX	gpio5.IO[4]	spdif1.IN	pwm2.OUT	
SPDIF_EXT_CLK	gpio5.IO[5]	spdif1.EXT_CLK	pwm1.OUT	

Table 6 (SAI3, SPDIF) continued

Pin Name	FUNC3	FUNC4	FUNC5	FUNC6	FUNC7
SAI3_RXFS	sai3.RX_DATA[1]	SPDIF_IN	gpio4.IO[28]	PDM_BIT [0]	reserved
SAI3_RXC	sai3.RX_DATA[1]	uart2.CTS_B	gpio4.IO[29]	PDM_CLK	reserved
SAI3_RXD	sai3.TX_DATA[1]	uart2.RTS_B	gpio4.IO[30]	PDM_BIT [1]	reserved
SAI3_TXFS	sai3.TX_DATA[1]	uart2.RX	gpio4.IO[31]	PDM_BIT [3]	reserved
SAI3_TXC		uart2.TX	gpio5.IO[0]	PDM_BIT [2]	reserved
SAI3_TXD		SPDIF_EXT_CLK	gpio5.IO[1]		reserved
SAI3_MCLK		SPDIF_OUT	gpio5.IO[2]	SPDIF_IN	reserved

SPDIF_TX			gpio5.IO[3]		reserved
SPDIF_RX			gpio5.IO[4]		reserved
SPDIF_EXT_CLK			gpio5.IO[5]		reserved

Table 7 (I2C)

Pin Name	Default	FUNC0	FUNC1	FUNC2	FUNC3	FUNC5	FUNC7
I2C2_SCL	gpio5.IO[16]	i2c2.SCL	enet1.1588_ EVENT1_IN	usdhc3.CD_B	ECSPI1_MISO	gpio5.IO[16]	reserved
I2C2_SDA	gpio5.IO[17]	i2c2.SDA	enet1.1588_ EVENT1_OUT	usdhc3.WP	ECSPI1_SS0	gpio5.IO[17]	reserved
I2C3_SCL	gpio5.IO[18]	i2c3.SCL	pwm4.OUT	gpt2.CLK	ECSPI2_SCLK	gpio5.IO[18]	reserved
I2C3_SDA	gpio5.IO[19]	i2c3.SDA	pwm3.OUT	gpt3.CLK	ECSPI2_MOSI	gpio5.IO[19]	reserved
I2C4_SCL	gpio5.IO[20]	i2c4.SCL	pwm2.OUT		ECSPI2_MISO	gpio5.IO[20]	reserved
I2C4_SDA	gpio5.IO[21]	i2c4.SDA	pwm1.OUT		ECSPI2_SS0	gpio5.IO[21]	reserved

Table 8 (UART)

Pin Name	Default	FUNC0	FUNC1	FUNC3	FUNC5	FUNC7
UART2_RXD	gpio5.IO[24]	uart2.RX	ecspi3.MISO	GPT1_COMPARE3	gpio5.IO[24]	reserved
UART2_TXD	gpio5.IO[25]	uart2.TX	ecspi3.SS0	GPT1_COMPARE2	gpio5.IO[25]	reserved
UART4_RXD	gpio5.IO[28]	uart4.RX	uart2.CTS_B	GPT1_COMPARE1	gpio5.IO[28]	reserved
UART4_TXD	gpio5.IO[29]	uart4.TX	uart2.RTS_B	GPT1_CAPTURE1	gpio5.IO[29]	reserved

Table 9 (Ethernet)

Pin Name	Default	FUNC0	FUNC1	FUNC2
ENET_MDC	gpio1.IO[16]	enet1.MDC		SAI6_TX_DATA[0]
ENET_MDIO	gpio1.IO[17]	enet1.MDIO		SAI6_TX_SYNC
ENET_TD3	gpio1.IO[18]	enet1.RGMII_TD3		SAI6_TX_BCLK
ENET_TD2	gpio1.IO[19]	enet1.RGMII_TD2	INPUT=enet1.TX_CLK OUTPUT=ccmsrcgpcmix. ENET_REF_CLK_ROOT	SAI6_RX_DATA[0]
ENET_TD1	gpio1.IO[20]	enet1.RGMII_TD1		SAI6_RX_SYNC
ENET_TD0	gpio1.IO[21]	enet1.RGMII_TD0		SAI6_RX_BCLK
ENET_TX_CTL	gpio1.IO[22]	enet1.RGMII_TX_CTL		SAI6_MCLK
ENET_TXC	gpio1.IO[23]	enet1.RGMII_TXC	enet1.TX_ER	SAI7_TX_DATA[0]
ENET_RX_CTL	gpio1.IO[24]	enet1.RGMII_RX_CTL		SAI7_TX_SYNC
ENET_RXC	gpio1.IO[25]	enet1.RGMII_RXC	enet1.RX_ER	SAI7_TX_BCLK
ENET_RD0	gpio1.IO[26]	enet1.RGMII_RD0		SAI7_RX_DATA[0]
ENET_RD1	gpio1.IO[27]	enet1.RGMII_RD1		SAI7_RX_SYNC
ENET_RD2	gpio1.IO[28]	enet1.RGMII_RD2		SAI7_RX_BCLK
ENET_RD3	gpio1.IO[29]	enet1.RGMII_RD3		SAI7_MCLK

Table 9 (Ethernet) continued

Pin Name	FUNC3	FUNC4	FUNC5	FUNC6
ENET_MDC	PDM_BIT[3]	SPDIF_OUT	gpio1.IO[16]	USDHC3_STROBE
ENET_MDIO	PDM_BIT[2]	SPDIF_IN	gpio1.IO[17]	USDHC3_DATA5
ENET_TD3	PDM_BIT[1]	SPDIF_EXT_CLK	gpio1.IO[18]	USDHC3_DATA6
ENET_TD2	PDM_BIT[3]		gpio1.IO[19]	USDHC3_DATA7
ENET_TD1	PDM_BIT[2]		gpio1.IO[20]	USDHC3_CD_B
ENET_TD0	PDM_BIT[1]		gpio1.IO[21]	USDHC3_WP
ENET_TX_CTL			gpio1.IO[22]	USDHC3_DATA0

ENET_TXC			gpio1.IO[23]	USDHC3_DATA1
ENET_RX_CTL	PDM_BIT[3]		gpio1.IO[24]	USDHC3_DATA2
ENET_RXC	PDM_BIT[2]		gpio1.IO[25]	USDHC3_DATA3
ENET_RD0	PDM_BIT[1]		gpio1.IO[26]	USDHC3_DATA4
ENET_RD1	PDM_BIT[0]		gpio1.IO[27]	USDHC3_RESET_B
ENET_RD2	PDM_CLK		gpio1.IO[28]	USDHC3_CLK
ENET_RD3	SPDIF_IN		gpio1.IO[29]	USDHC3_CMD

Table 10 (ECSPI)

Pin Name	Default	FUNC0	FUNC1	FUNC2	FUNC3
ECSPI2_SCLK	gpio5.IO[10]	ecspi2.SCLK	uart4.RX	I2C3_SCL	SAI5_RX_DATA[2]
ECSPI2_MOSI	gpio5.IO[11]	ecspi2.MOSI	uart4.TX	I2C3_SDA	SAI5_RX_DATA[3]
ECSPI2_MISO	gpio5.IO[12]	ecspi2.MISO	uart4.CTS_B	I2C4_SCL	SAI5_MCLK
ECSPI2_SS0	gpio5.IO[13]	ecspi2.SS0	uart4.RTS_B	I2C4_SDA	

Table 10 (ECSPI) continued

Pin Name	FUNC4	FUNC5	FUNC7
ECSPI2_SCLK	SAI5_TX_BCLK	gpio5.IO[10]	reserved
ECSPI2_MOSI	SAI5_TX_DATA[0]	gpio5.IO[11]	reserved
ECSPI2_MISO		gpio5.IO[12]	reserved
ECSPI2_SS0		gpio5.IO[13]	reserved

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VSYS_5V	DC supply input	-0.3	--	+6	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VSYS_5V	DC supply input	4.5	5	5.5	V
NVCC_ENET	Power supply for Ethernet	1.65	1.8	1.95	V
		2.25	2.5	2.75	V
		3	3.3	3.6	V

3.3 Digital IO Pin DC Characteristics

For VDD = 1.8V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VOH	Output High Voltage	0.8 x VDD	-	VDD	V
VOL	Output low level	0	-	0.2 x VDD	V
VIH	Input High level	0.7 x VDD	-	VDD + 0.3	V
VIL	Input low level	-0.3	-	0.3 x VDD	V

For VDD = 3.3V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VOH	Output High Voltage	0.8 x VDD	-	VDD	V
VOL	Output low level	0	-	0.2 x VDD	V
VIH	Input High level	0.7 x VDD	-	VDD + 0.3	V
VIL	Input low level	-0.3	-	0.3 x VDD	V

3.4 Interface

3.4.1 ECSPI timing parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

3.4.1.1 ECSPI Master mode timing

Figure 1 depicts the timing of ECSPI in master mode. Table 11 lists the ECSPI master mode timing characteristics.

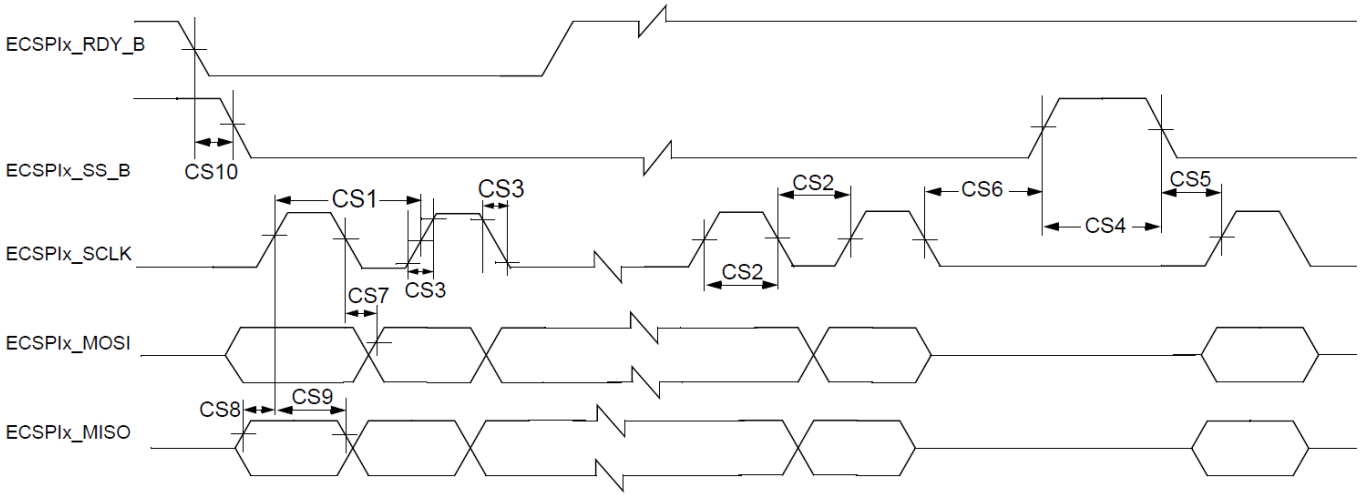


Figure 1 ECSPI Master mode timing diagram

Table 11 ECSPI Master mode timing diagram

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	18	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

3.4.1.2 ECSPI Slave mode timing

Figure 2 depicts the timing of ECSPI in Slave mode. Table 12 lists the ECSPI Slave mode timing characteristics.

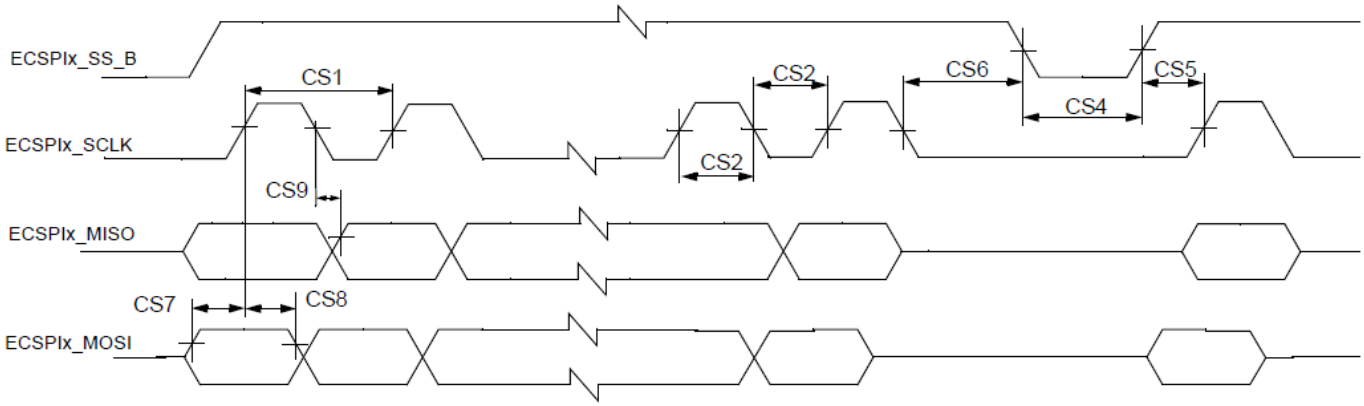


Figure 2 ECSPI Slave mode timing diagram

Table 12 ECSPI Slave mode timing diagram

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

3.4.2 Ultra-high-speed SD/SDIO host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD(single data rate) timing, SD3.0 (dual data rate) AC timing, and SDR50/SDR104 AC timing.

3.4.2.1 SD3.0 (single data rate) AC timing

Figure 3 depicts the timing of SD3.0 (SDR), and Table 13 lists the SD3.0 (SDR) timing characteristics.

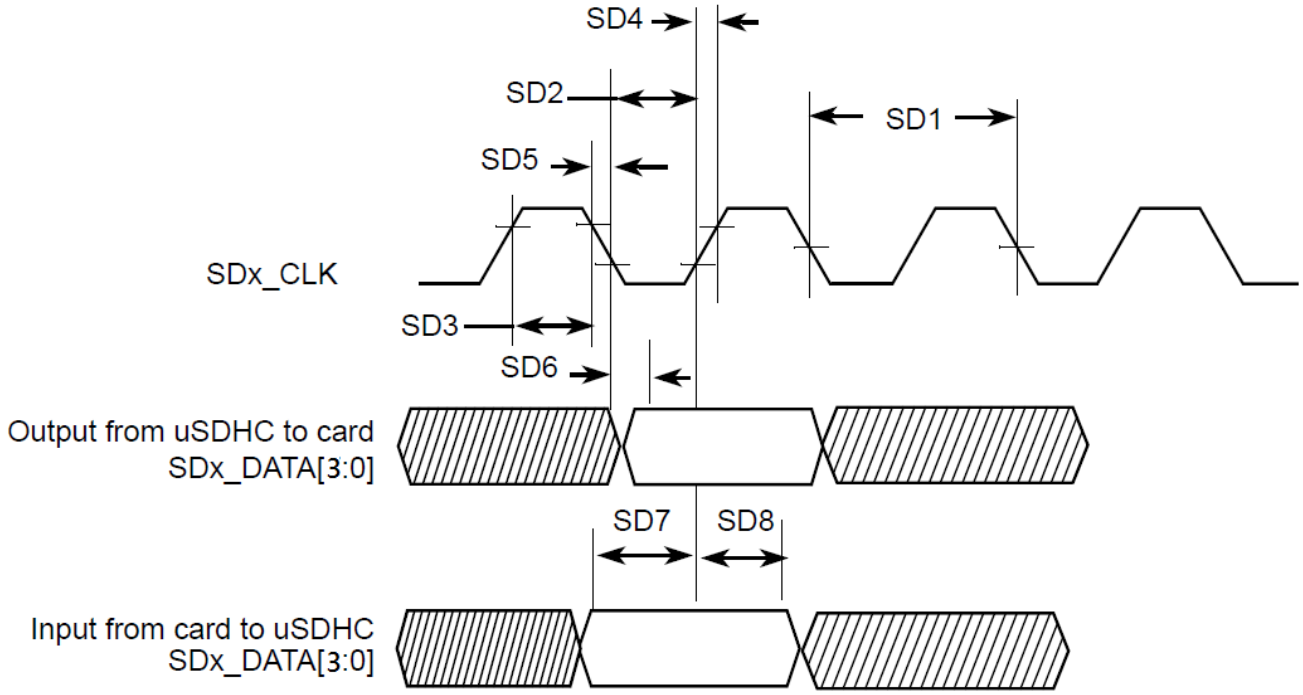


Figure 3 SD3.0 (SDR) timing

Table 13 SD3.0 (SDR) interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
	Card Input Clock				
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
	uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)				
SD6	uSDHC Output Delay	t_{OD}	6.6	3.6	ns
	uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)				
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In High-speed mode, clock frequency can be any value between 0—50 MHz.

3 In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In High-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.4.2.2 SD3.0 (dual data rate) AC timing

Figure 4 depicts the timing of SD3.0 (DDR). Table 14 lists the SD3.0 (DDR) timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

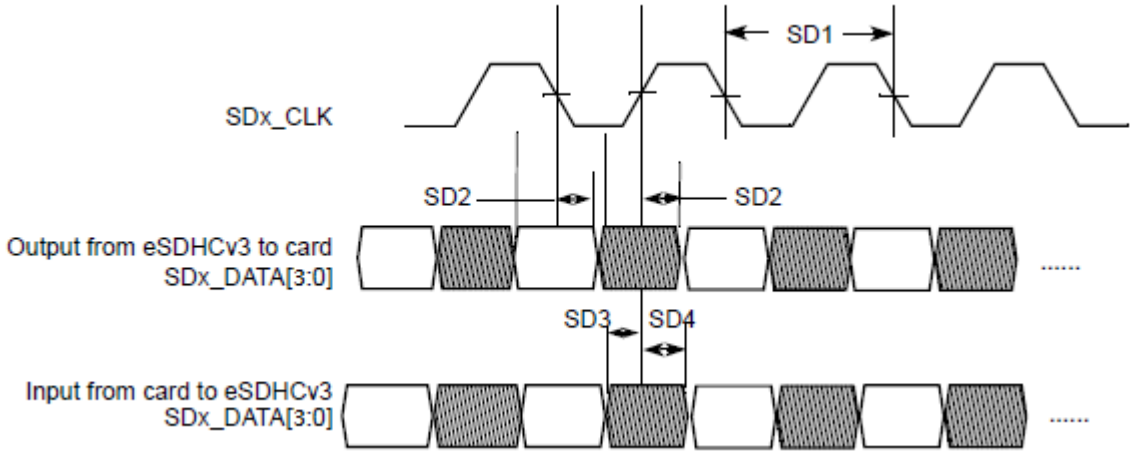


Figure 4 SD3.0 (DDR) interface timing specification

Table14 SD3.0 (DDR) interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC5.1 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.7	6.9	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.3	—	ns

3.4.3 Ethernet controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

3.4.3.1 RMII mode timing

Figure 5 shows RMII mode timings. Table 15 describes the timing parameters (M16–M21) shown in the figure.

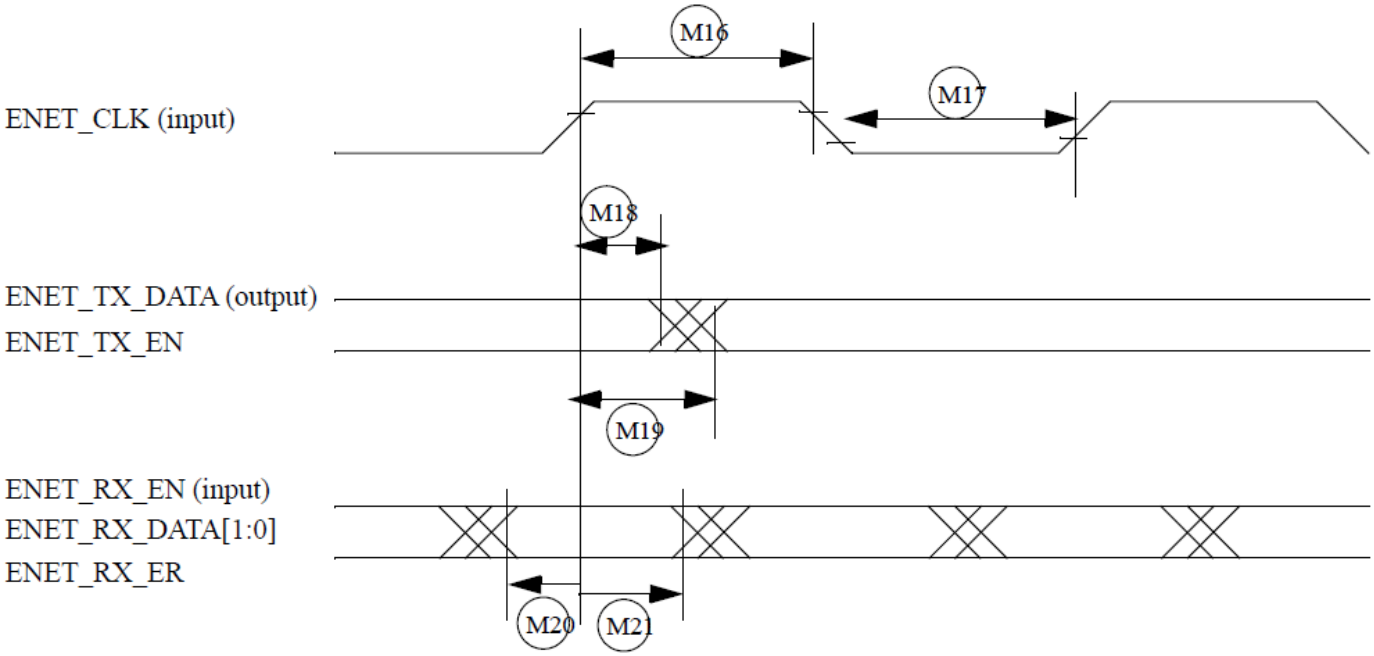


Figure 5. RMII mode signal timing diagram

Table 15. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	15	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

3.4.3.2 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table16. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

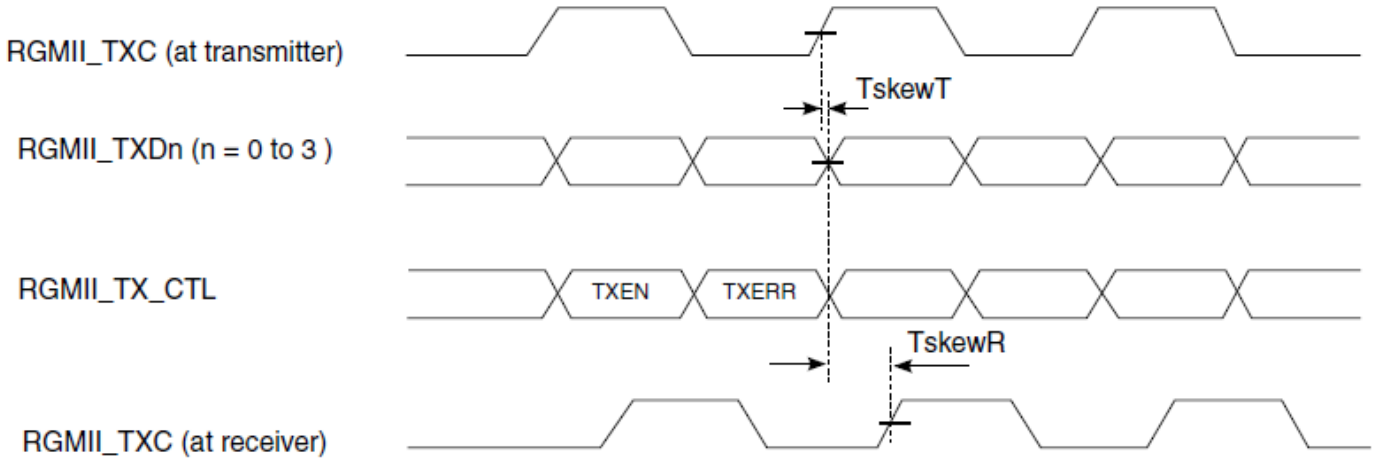


Figure 6. RGMII transmit signal timing diagram original

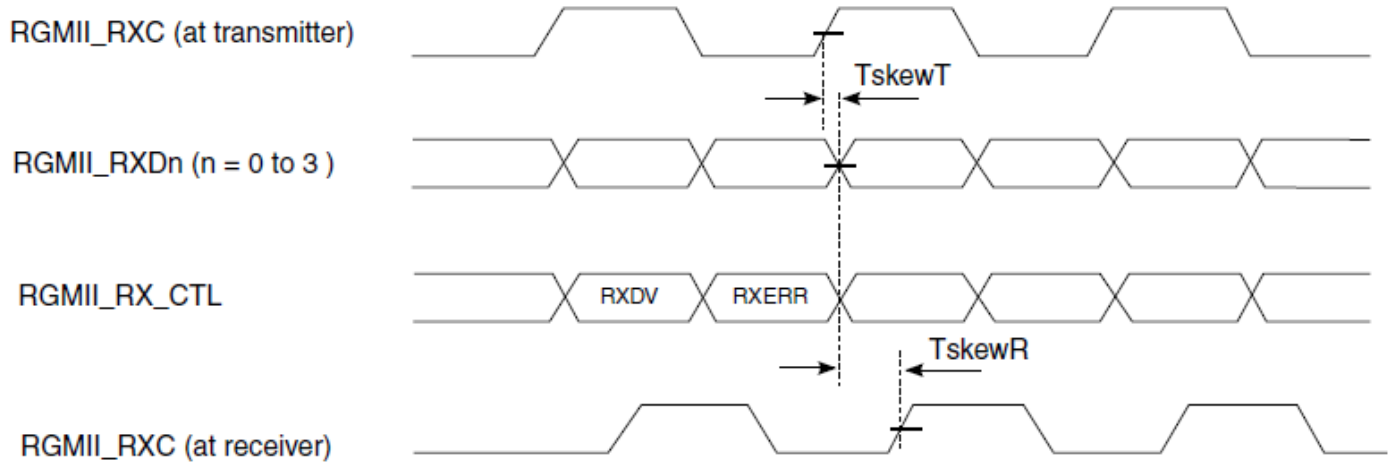


Figure 7. RGMII receive signal timing diagram original

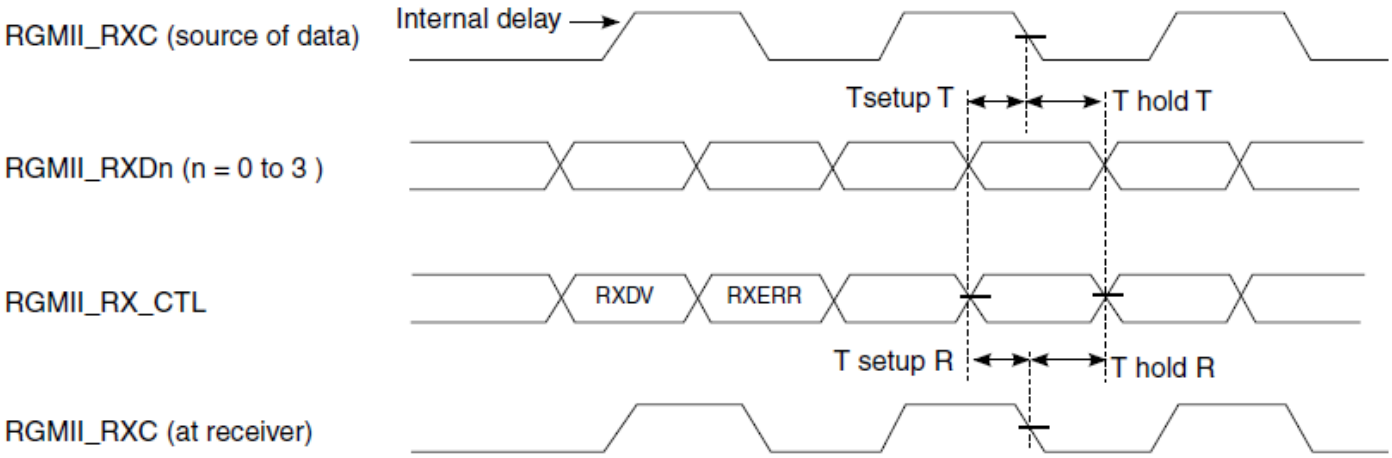


Figure 8. RGMII receive signal timing diagram with internal delay

3.4.4 I2C bus characteristics

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

3.4.5 MIPI D-PHY timing parameters

MIPI D-PHY electrical specifications are compliance.

3.4.6 PDM timing parameters

Figure 9 illustrates the input timing of the PDM.

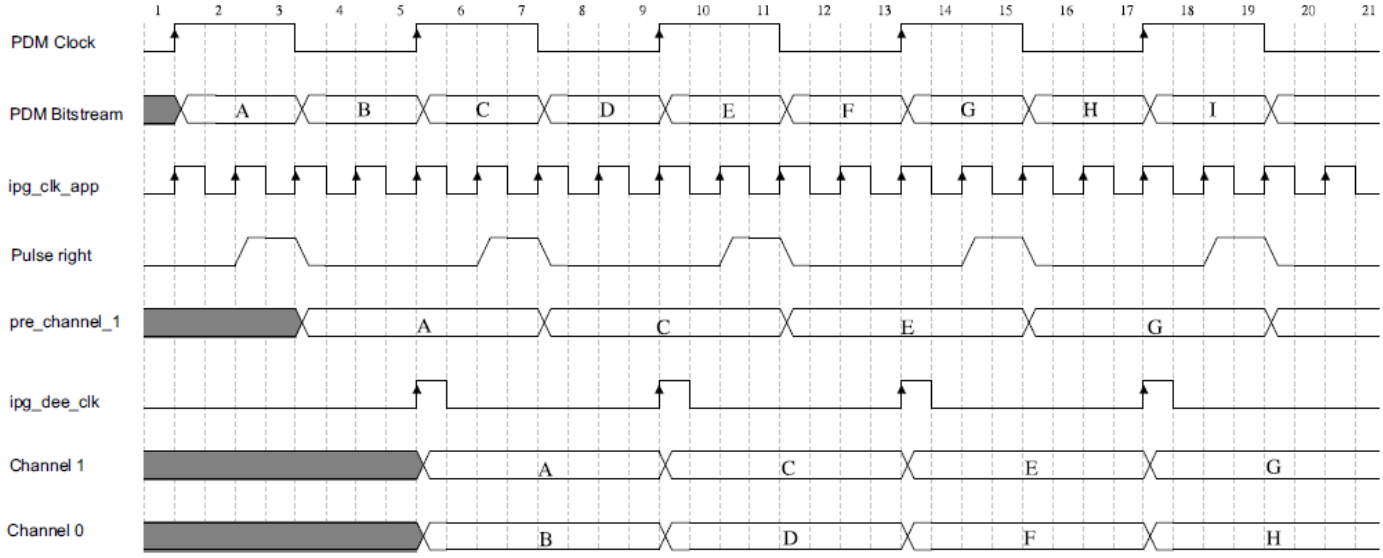


Figure 9. PDM input timing

PDM clock operative range is from 500 kHz to 6 MHz. Within range, only need to configure ipg_clk_app rate and CLKDIV without I/O timing concerns.

3.4.7 SAI/I2S switching specifications

This section provides the AC timings for the SAI in Master (clocks driven) and Slave (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP]= 0) and non inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 17. Master mode SAI timing (50 MHz)[1]

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	20	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	20	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	2	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	2	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	2	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

[1] To achieve 50 MHz for BCLK operation, clock must be set in feedback mode.

Table 18. Master mode SAI timing (25 MHz)

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	2	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	2	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	12	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

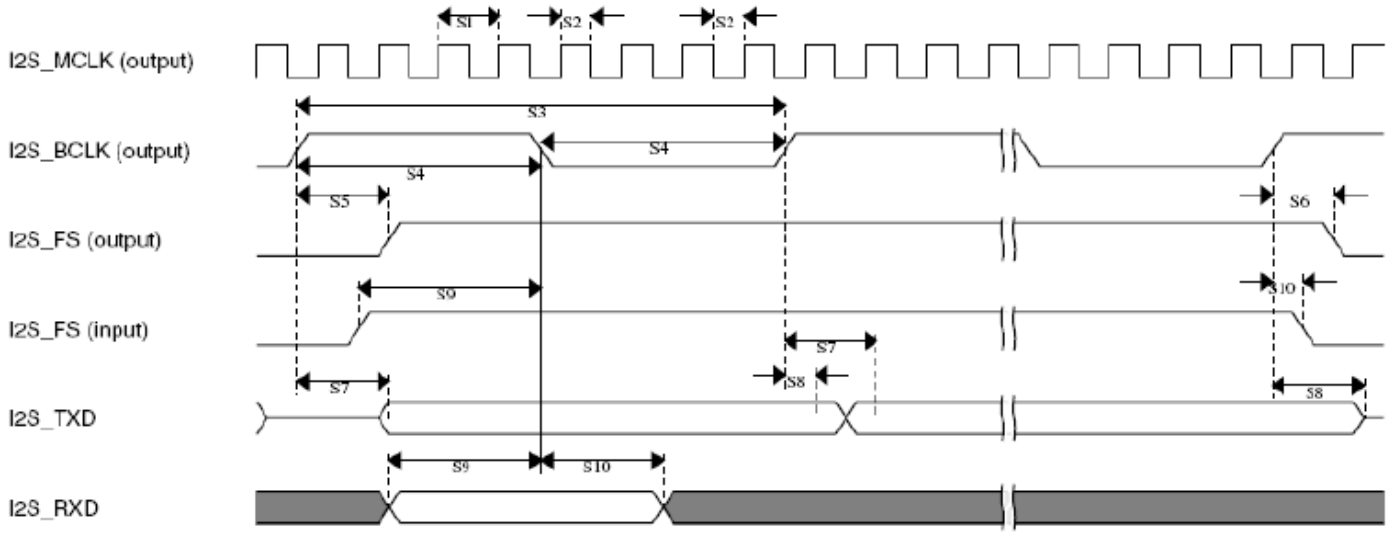


Figure 10. SAI timing—Master modes

Table 19. Slave mode SAI timing (50 MHz)[1]

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	20	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	2	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S17	SAI_RXD setup before SAI_BCLK	2	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

[1] TX does not support 50 MHz operation in Slave mode.

Table 20. Slave mode SAI timing (25 MHz)

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	12	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	7	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	12	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

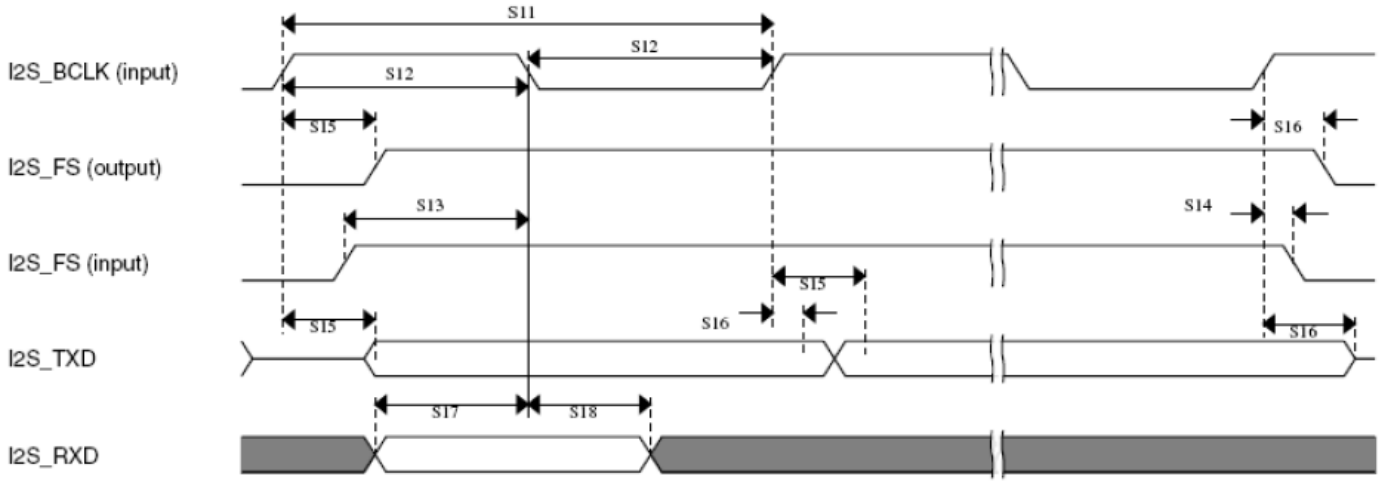


Figure 11. SAI Timing — Slave Modes

3.4.8 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal. Table 21 and Figure 12 and Figure 13 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 21. SPDIF timing parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

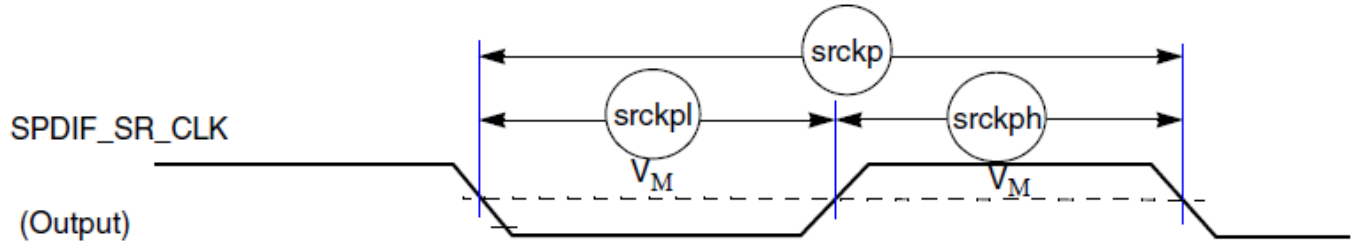


Figure 12. SPDIF_SR_CLK timing diagram

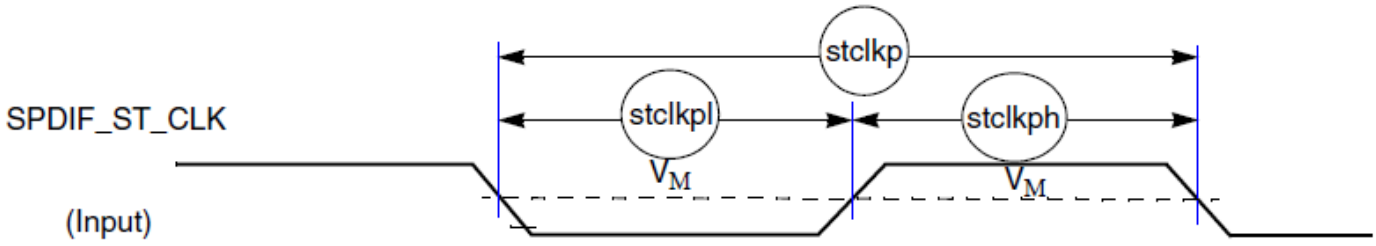


Figure 13. SPDIF_ST_CLK timing diagram

3.4.9 UART I/O configuration and timing parameters

The i.MX 8M Nano UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 22 shows the UART I/O configuration based on the enabled mode.

Table 22. UART I/O configuration vs. mode Port

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

3.4.9.1 UART transmitter

Figure 14 depicts the transmit timing of UART in the RS-232 Serial mode, with 8 data bit/1 stop bit format. Table 23 lists the UART RS-232 Serial mode transmit timing characteristics.

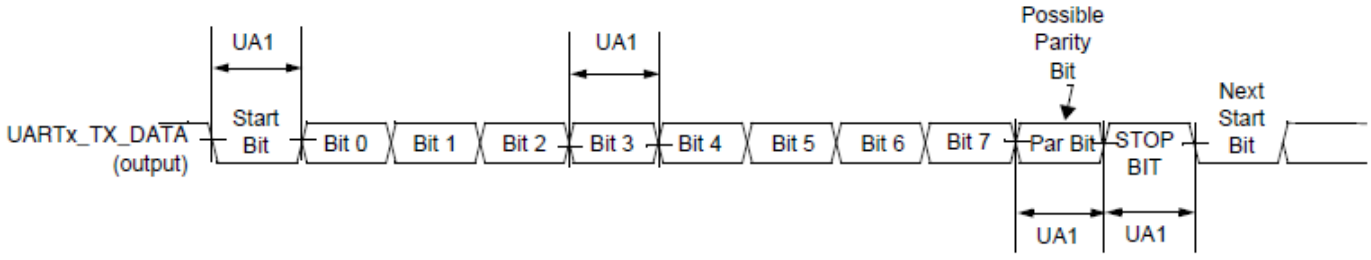


Figure 14. UART RS-232 Serial mode transmit timing diagram

Table 23. RS-232 Serial mode transmit timing parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.
[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.4.9.2 UART receiver

Figure 15 depicts the RS-232 Serial mode receive timing with 8 data bit/1 stop bit format. Table 24 lists Serial mode receive timing characteristics.

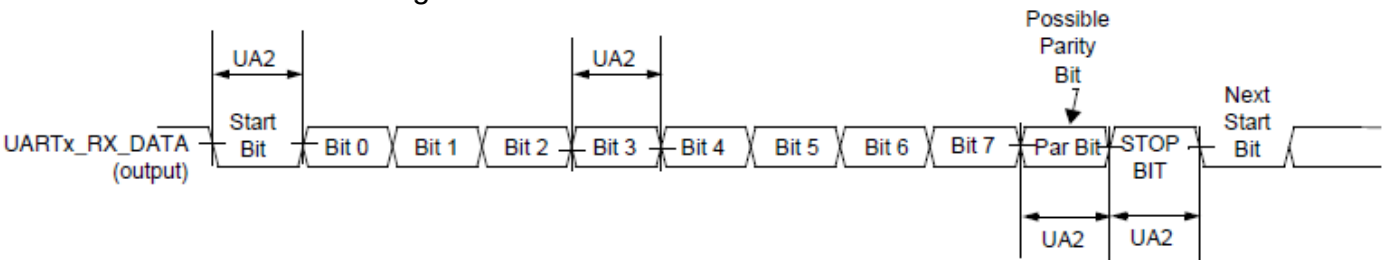


Figure 15. UART RS-232 Serial mode receive timing diagram

Table 24. RS-232 Serial mode receive timing parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

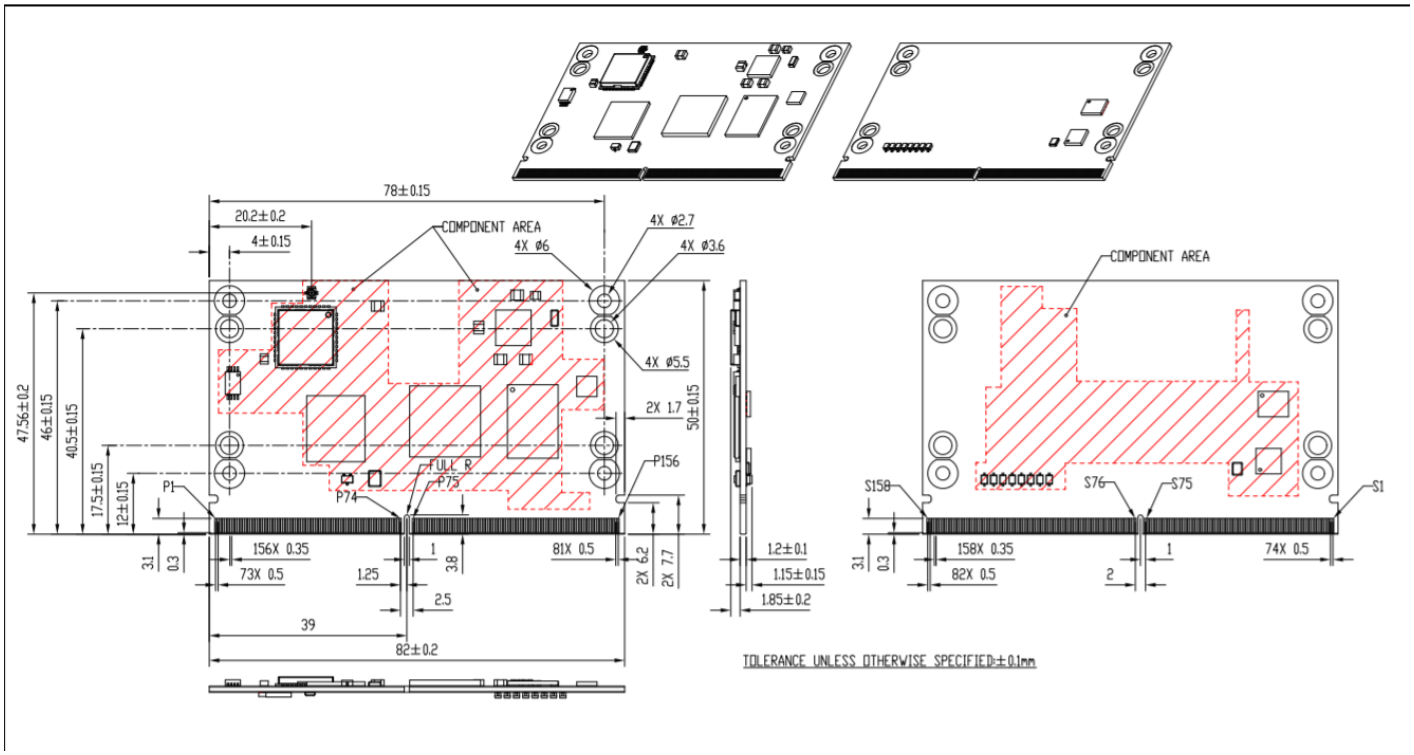
[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.
[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

3.5 Power Consumption*

Operation mode	avg	peak	MHz	remark
Off Mode	TBD	TBD	TBD	
Suspend, WLAN disconnected, BT page scan	TBD	TBD	TBD	
WLAN off, only Linux kernel, no application software	TBD	TBD	TBD	
WLAN connected, only Linux kernel, no application software	TBD	TBD	TBD	
Audio Playback, low network load	TBD	TBD	TBD	iperf 1Mbit/s over WLAN
Audio Playback, high network load	TBD	TBD	TBD	iperf 50Mbit/s over WLAN
Bluetooth A2DP Receive	TBD	TBD	TBD	

4. Mechanical Information

4.1 Mechanical Drawing



4.2 Sample Information

Top side	Bottom side

5. Packaging Information

TBD