

AW-NM191NF

IEEE 802.11 b/g/n Wireless LAN Module

Layout Guide

Version 0.4

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Document release	Date	Modification	Initials	Approved
Version 0.1	2014/3/06	Initial Version	Terry	Amos
Version 0.2	2014/03/05	Updated Mechanical dwg. and schematics	Terry	Amos
Version 0.3	2014/05/14	Updated schematics	Terry	Amos
Version 0.4	2015/08/25	Update Mechanical dwg	Terry	Amos

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INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating AW-NM191NF layout. It is strongly recommended that layout be reviewed by AzureWave engineering team before released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- Ground Layout
- Power Layout
- Digital Interface
- The other layout guide Information

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1. Ground Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- (1) The top layer of customer platform should keep completed ground for our module.
- (2) The area under our module forbidden any trace and via on top layer of customer platform.

2. Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

- (1) Power traces shall surround ground to get stable and make sure all power traces have good return path to ground.
- (2) Do not get close to digital traces (SDIO,USB) or continuous data traces, there could be coupling noise affect power traces and IC.

3. Digital Interface

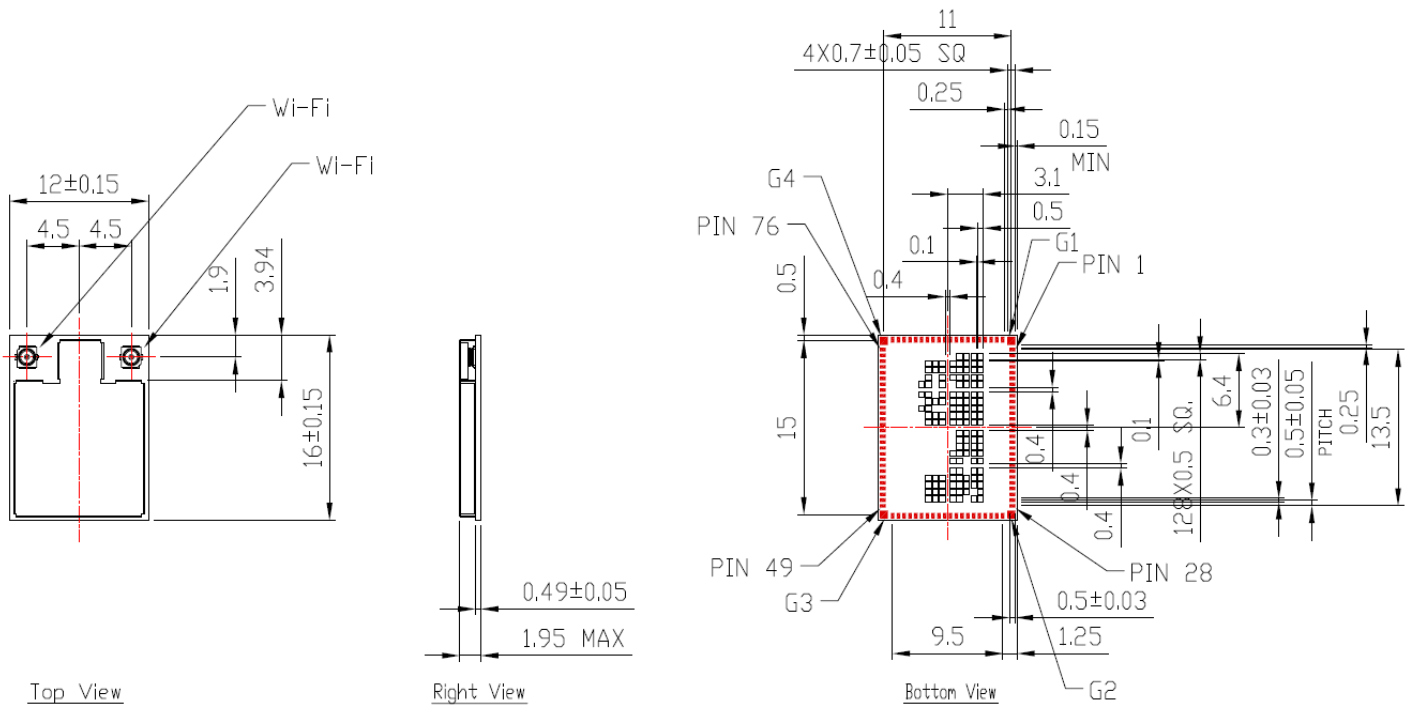
Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

- (1) The digital Interface to the module must be well routed to minimize coupling to power planes and other digital signals.
- (2) Make sure USB differential traces impedance is 90 ohm.

4. The other layout guide information

- Keep the module unused function pins floating.
- High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.
- Good power integrity of VDD will improve the signal integrity of digital interfaces.
- Clock(SUSCLK) should have complete ground to make sure coupling will not happen to any other path.

5. Mechanical Drawing



Tolerances unless otherwise specified : ± 0.15 mm

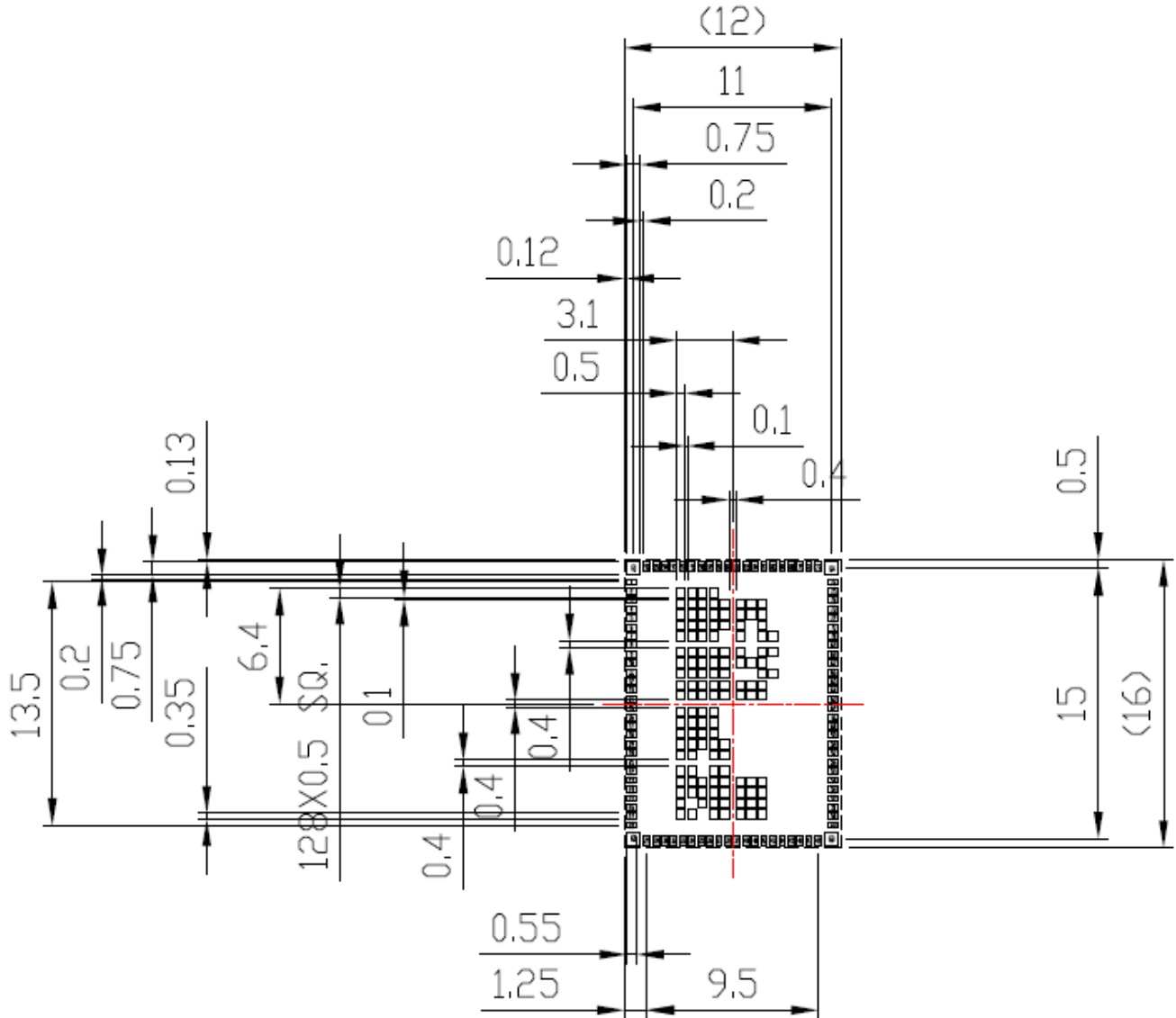
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Top View PCB Layout Footprint



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