AzureWave Technologies, Inc.

AW-CU484

IEEE 802.15.4 and Bluetooth LE 5.0 wireless microcontroller Stamp LGA Module

Datasheet

Rev. E

DF

(For STD)

Features

Benefits

- Very low current solution for long battery life
- Single chip device to run stack and application
- System BOM is low in component count and cost
- Flexible sensor interfacing
- Embedded NTAG

Radio

- 2.4 GHz IEEE 802.15.4 2011 compliant
- 2.4 GHz Bluetooth Low Energy 5.0 compliant
- Bluetooth Low Energy 5.0 2Mbps high data rate
- Improved co-existence with WiFi
- 1.9 V to 3.6 V supply voltage
- Antenna Diversity control
- 32 MHz XTAL cell with internal capacitors, able with suitable external XTAL to meet the required accuracy for radio operation over the operating conditions
- Integrated RF balun
- Integrated Ultra Low-power sleep oscillator
- Deep Power-down current 350 nA (with wake-up from IO)
- 128-bit or 256-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers

Microcontroller

- Application CPU, Arm Cortex-M4 CPUs:
  - Arm Cortex-M4 processor, running at a frequency of up to 48 MHz.
  - Arm built-in Nested Vectored Interrupt Controller (NVIC)
  - Memory Protection Unit (MPU)
  - Non-maskable Interrupt (NMI) with a selection of sources
  - Serial Wire Debug (SWD) with 8 breakpoints and 4 watch points
  - System tick timer
  - Includes Serial Wire Output for enhanced debug capabilities.
- On-Chip memory
  - 640 KB flash
  - 152 KB SRAM
- 12 MHz to 48 MHz system clock speed for low-power
- 2 x I2C-bus interface, operate as either master or slave
- 10 x PWM
- 2 x Low-power timers
- 2 x USART, one with flow control
- 2 x SPI-bus, master or slave
- 1 x PDM digital audio interface with a hardware based voice activity detector to reduce power consumption in voice applications. Support for dual-channel microphone interface, flexible decimators, 16 entry FIFOs and optional DC blocking.
- 19-channel DMA engine for efficient data transfer between peripherals and SRAM, or SRAM to SRAM. DMA can operate with fixed or incrementing addresses. Operations can be chained together to provide complex functionality with low CPU overhead.

- Up to four GPIOs can be selected as pin interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- 32-bit Real Time clock (RTC) with 1 s resolution. A timer in the RTC can be used to wake from Sleep, Deep-sleep and Power-down, with 1 ms resolution
- Voltage Brown Out with 8 programmable thresholds
- 8-input 12-bit ADC, 190 kS/sec. HW support for continuous operation or single conversions, single or multiple inputs can be sampled within a sequence. DMA operation can be linked to achieve low overhead operation.
- 1 x analog comparator
- Battery and temperature sensors
- Watchdog timer and POR
- Standby power controller
- Up to 22 Digital IOs (DIO)
- 1 x Quad SPIFI for accessing an external flash device
- Integrated NTAG I2C plus device, NFC Forum Type 2
- Random Number Generator engine
- AES engine AES-128 to 256
- Hash hardware accelerator support SHA-1 and SHA-256
- EFuse:
  - 128-bit random AES key
  - configuration modes
  - Trimming
- ISO7816 smart card digital interface which with a suitable external analogue device can operate as a smart card reader

Applications

- ZigBee 3.0, Thread networks
- Bluetooth Low Energy 5.0 networks
- Robust and secure low-power wireless applications
- Smart lighting, door locks, thermostats and home automation
- Wireless sensor networks

Revision History

Document NO: R2-2484-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/6/22	DCN017604	● Initial Version	Shihhua Huang	NC Chen
B	2020/7/2	DCN017677	● Correct BT output power	Shihhua Huang	NC Chen
C	2020/12/4	DCN019432	● Add Thread features ● Modify chapter 1.3 info ● Update power consumption	Shihhua Huang	NC Chen
D	2021/4/22	DCN021245	*Changed to new format ● Modify Block Diagram	Shihhua Huang	NC Chen
E	2021/8/30	DCN023041	● Modify chapter 1.3 info	Shihhua Huang	NC Chen

Table of Contents

Revision History **4**
Table of Contents **5**
1. Introduction **6**
1.1 Product Overview **6**
1.2 Block Diagram **7**
1.3 Specifications Table **8**
1.3.1 General 8
1.3.2 Bluetooth 8
1.3.3 Zigbee 8
1.3.4 Operating Conditions 9
2. Pin Definition **10**
2.1 Pin Map **10**
2.2 Pin Table **11**
3. Electrical Characteristics **13**
3.1 Recommended Operating Conditions **13**
3.2 Absolute Maximum Ratings **13**
3.3 AC characteristics **14**
3.3.1 Reset and Supply Voltage Monitor 14
3.3.2 USART timing 15
3.3.3 SPIFI timing 16
3.3.4 PWM timing 17
3.3.5 DMIC timing 17
3.3.6 SPI timing 18
3.4 Power Consumption* **20**
4. Mechanical Information **21**
4.1 Mechanical Drawing **21**
5. Packaging Information **22**
5.1 Tape & Reel Picture **22**
5.2 Packing Picture **22**
5.3 Inside of Inner Box Picture **23**
5.4 Inner Box Picture **23**
5.5 Inside of Carton Picture **24**
5.6 Carton and Label Picture **24**

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.15.4 Zigbee and Bluetooth module --- AW-CU484. The AW-CU484 is ultra-low power, high performance Arm® Cortex®-M4 based wireless microcontrollers supporting Zigbee 3.0, Thread and Bluetooth Low Energy 5.0 networking stack to facilitate home and building automation, smart lighting, smart locks and sensor network applications.

The AW-CU484 includes a 2.4 GHz Bluetooth Low Energy 5 (supporting eight simultaneous connections) compliant transceiver, a 2.4 GHz IEEE 802.15.4 compliant transceiver and a comprehensive mix of analog and digital peripherals. Ultra-low current consumption in both radio receive and transmit modes and also in the power down modes allow use of coin cell batteries.

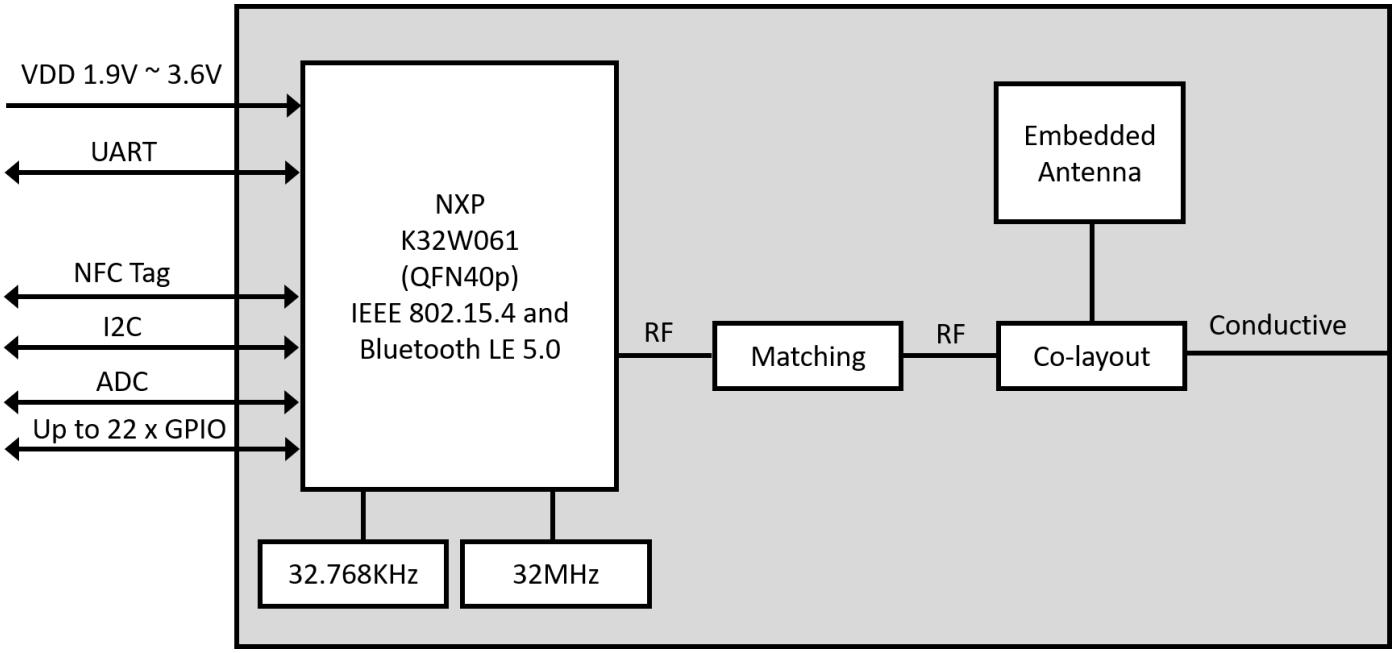
The product has 640 KB embedded Flash and 152 KB RAM memory. The embedded flash can support Over the Air (OTA) code download to applications. The devices include 10-channel PWM, two timers, one RTC/alarm timer, a Windowed Watchdog Timer (WWDT), two USARTs, two SPI interfaces, two I2C interfaces, a DMIC subsystem including a dual-channel PDM microphone interface with voice activity detector, one 12-bit ADC, temperature sensor and comparator.

The AW-CU484 variant has an internal NFC tag with connections to the external NFC antenna.

The Arm Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level support of the block integration.

The Arm Cortex-M4 CPU, operates at up to 48 MHz.

1.2 Block Diagram



AW-CU484 BLOCK DIAGRAM

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.15.4 and Bluetooth LE 5.0 1T1R (Stamp LGA)
Major Chipset	K32W061 (QFN 40p)
Host Interface	Zigbee + BT ● UART
Dimension	15mm x 19.615mm x 2.45mm (Tolerance remarked in mechanical drawing)
Form factor	Stamp LGA Module
Antenna	Main：Zigbee/ Bluetooth → TX/RX
Weight	1.2g

1.3.2 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth Low Energy 5.0
Bluetooth VID/PID	N/A
Frequency Rage	2402~2480MHz
Modulation	GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps)
Output Power (Board Level Limit)*	See table below
Receiver Sensitivity	See table below

	Min	Typ	Max	Unit
Low Energy (1MHz)	8	10	12	dBm
Low Energy (2MHz)	8	10	12	dBm

	Min	Typ	Max	Unit
Low Energy (1MHz)		-94	-87	dBm
Low Energy (2MHz)		-90	-84	dBm

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Zigbee

Features	Description
WLAN Standard	IEEE 802.15.4 1T1R
WLAN VID/PID	N/A

<table>
<tr><td>WLAN SVID/SPID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2.4 GHz：2.405 ~ 2.480 GHz</td></tr>
<tr><td>Modulation</td><td>O-QPSK</td></tr>
<tr><td>Number of Channels</td><td>2.4GHz
■ USA, NORTH AMERICA, Canada and Taiwan – 11 ~ 24
■ China, Australia, Most European Countries – 11 ~ 26</td></tr>
<tr><td>Output Power
(Board Level Limit)*</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>15.4 (0.25Mbps)
@EVM<35%</td><td>8</td><td>10</td><td>12</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>15.4 (0.25Mbps)</td><td></td><td>-97</td><td>-94</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Data Rate</td><td>Zigbee:
802.15.4: 0.25Mbps</td></tr>
<tr><td>Security</td><td>■ 128-bit AES-CCM modes as specified by the IEEE802.15.4 2006 standard.</td></tr>
</table>

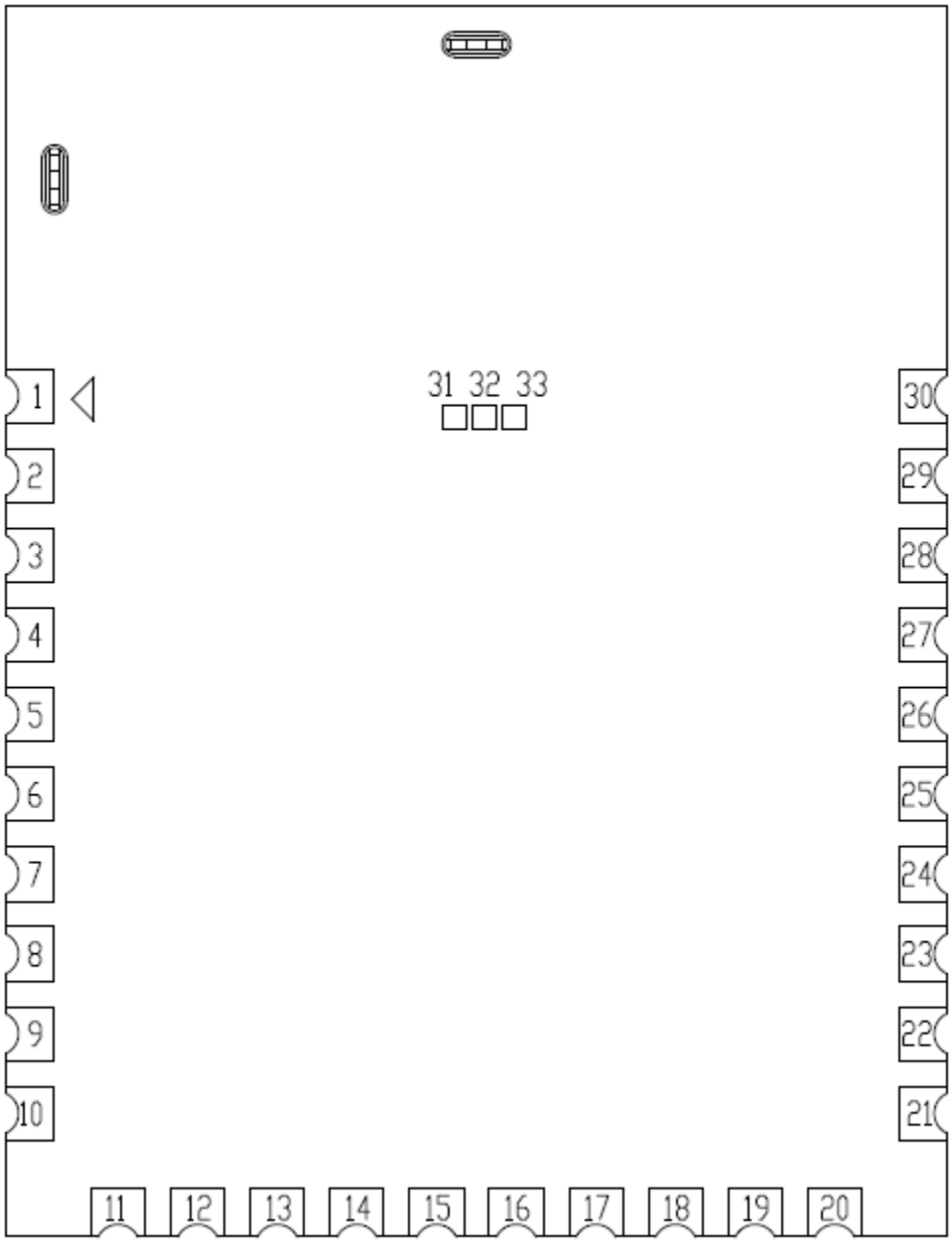
* If you have any certification questions about output power please contact FAE directly.

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	Power supply for host: 1.9V ~ 3.6V
Operating Temperature	-40℃~ 85℃
Operating Humidity	less than 85%R.H.
Storage Temperature	-40℃~ 125℃
Storage Humidity	less than 60%R.H.
ESD Protection	
Human Body Model	3KV
Changed Device Model	500V

2. Pin Definition

2.1 Pin Map



AW-CU484 Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	LB	NFC tag antenna input B		
2	LA	NFC tag antenna input A		
3	PIO_0/SPI1_SCK	General Purpose digital Input/ Output 0		IO
4	PIO_1/SPI1_MISO	General Purpose digital Input/ Output 1		IO
5	PIO_2/SPI1_MOSI	General Purpose digital Input/ Output 2		IO
6	PIO_3/SPI1_SSELN0	General Purpose digital Input/ Output 3		IO
7	PIO_4/PWM4-PU	General Purpose digital Input/ Output 4		IO
8	PIO_5/ISP_ENTRY	General Purpose digital Input/ Output 5		IO
9	PIO_6/PWM6-PD	General Purpose digital Input/ Output 6		IO
10	PIO_7/PWM7-PD	General Purpose digital Input/ Output 7		IO
11	PIO_8/USART0_TXD	UART0_TX		IO
12	PIO_9/USART0_RXD	UART0_RX		IO
13	PIO_10/I2C0_SCL	General Purpose digital Input/ Output 10		IO
14	PIO_11/I2C0_SDA	General Purpose digital Input/ Output 11		IO
15	PIO_12/SWCLK	General Purpose digital Input/ Output 12		IO
16	PIO_13/SWDIO	General Purpose digital Input/ Output 13		IO
17	PIO_14/ADC0	General Purpose digital Input/ Output 14		IO
18	PIO_15/ADC1	General Purpose digital Input/ Output 15		IO
19	PIO_16/SPIFI_CSN	General Purpose digital Input/ Output 16		IO
20	GND	Ground.		GND
21	GND	Ground.		GND

22	VDD	Power supply	1.9 ~3.6V	VDD
23	PIO_17/SPIFI_IO3	General Purpose digital Input/ Output 17		IO
24	PIO_18/SPIFI_CLK	General Purpose digital Input/ Output 18		IO
25	PIO_19/SPIFI_IO0	General Purpose digital Input/ Output 19		IO
26	PIO_20/SPIFI_IO2	General Purpose digital Input/ Output 20		IO
27	PIO_21/SPIFI_IO1	General Purpose digital Input/ Output 21		IO
28	RSTN	Reset. Active low.		I
29	GND	Ground.		GND
30	GND	Ground.		GND
31	GND	Ground.		GND
32	RF	RF out.		O
33	GND	Ground.		GND

3. Electrical Characteristics

3.1 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD	DCDC voltage	1.9		3.6	V

3.2 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{LX}	LA and LB pin voltage	-0.3		4.6	V_{peak}
V_{DD}	Supply voltage DCDC input	-0.3		3.96	V
V_{IO}	IO pins voltage	-0.3		3.96	V
V_{RST}	RSTIN voltage	-0.3		3.96	V
V_{ADC}	ADC pins voltage	-0.3		3.96	V

3.3 AC characteristics

3.3.1 Reset and Supply Voltage Monitor

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
t_{rst}	Reset time	External reset pluse width to initiate reset sequence	--	500	--	us
V_{rh}	Reset high voltage	External threshold voltage, for reset to be sampled high (inactive)	0.7xVDDE	--	--	V
V_{rl}	Reset low voltage	External threshold voltage for reset to be low (active)	--	--	0.7xVDDE	V
$V_{th(POR)}$	Power-on reset threshold voltage	Rise time > 10 ms				
		rising	--	1.85	--	V
		falling	--	1.75	--	V
t_{STAB}	Stabilisation time	Time after release of reset until application runs	--	--	1.9	ms
I_{DD}	Supply current	Chip current when held in reset, VDDE = 3 V	--	132	--	uA
$I_{rst(bodvbat)}$	Brownout reset current	Chip current when held in reset when voltage is above power-on-reset threshold but below brownout threshold	--	46	--	uA

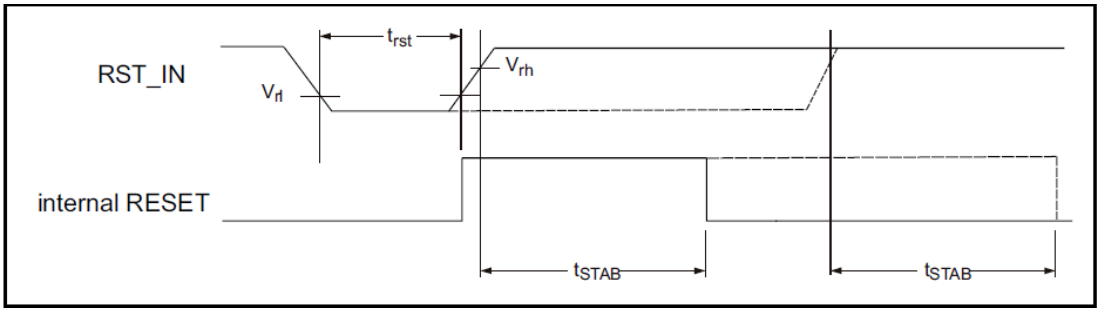


Fig 1. Reset signal timing

3.3.2 USART timing

Table 1. USART master timing (in synchronous mode)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$T_{SU(D)}$	Data set-up time		45	--	--	ns
$t_{h(D)}$	Data hold time		5	--	--	ns
$t_{V(Q)}$	Data output valid time		0	--	25	ns
$t_{CY(SCLK)}$	SCLK frequency		--	--	5	MHz

Table 2. USART slave timing (in synchronous mode)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$T_{SU(D)}$	Data set-up time		5	--	--	ns
$t_{h(D)}$	Data hold time		5	--	--	ns
$t_{V(Q)}$	Data output valid time		0	--	55	ns
$t_{CY(SCLK)}$	SCLK frequency		--	--	5	MHz

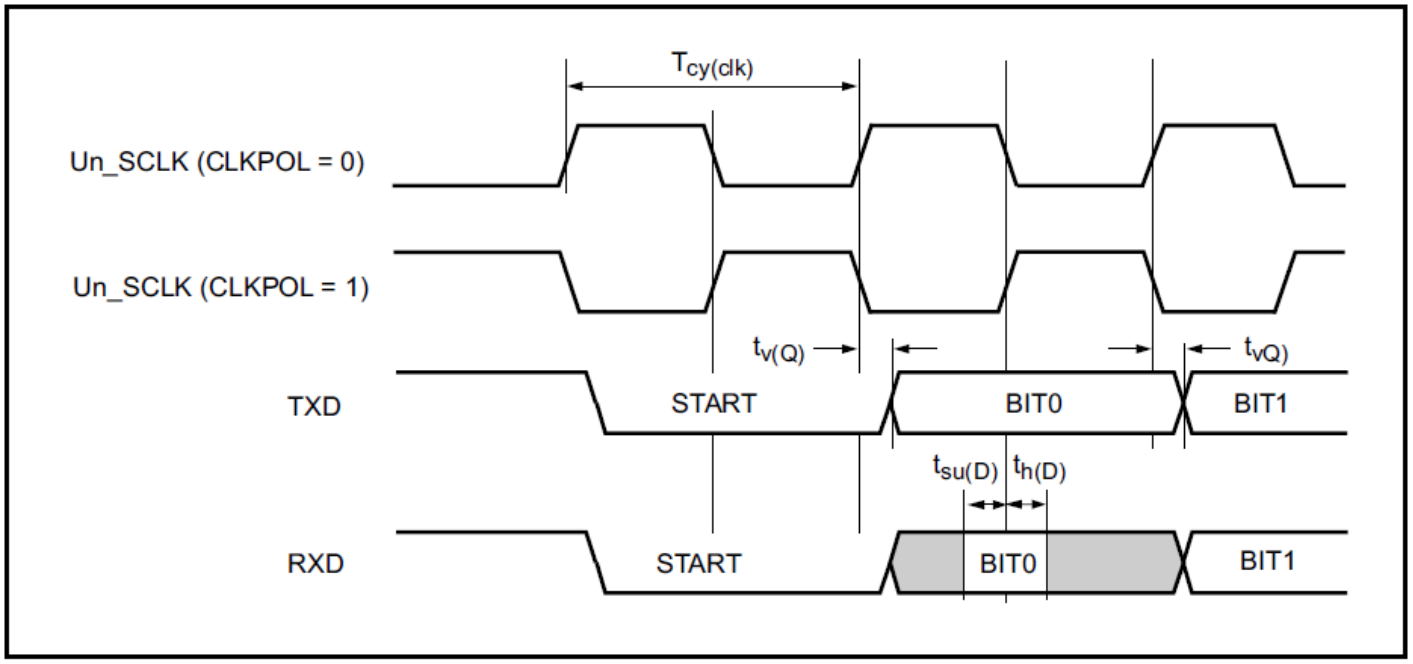


Fig 2. USART interface timings

3.3.3 SPIFI timing

Table 3. SPIFI timing

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$t_{cy(CLK)}$	Clock cycle time		30.0			ns
t_{DS}	Data set-up time		3			ns
t_{DH}	Data hold time		3			ns
$t_{V(Q)}$	Data output valid time		--	--	5	ns
$t_{H(Q)}$	Data output hold time		-10.5	--	--	ns
	Duty cycle		40	--	60	%
t_{SS}	SSEL set-up time, time SSEL is low before first SCK edge.		0.5	--	--	SCK cycles
t_{SH}	SSEL hold time, time SSEL is low after last SCK.		0.5	--	--	SCK cycles

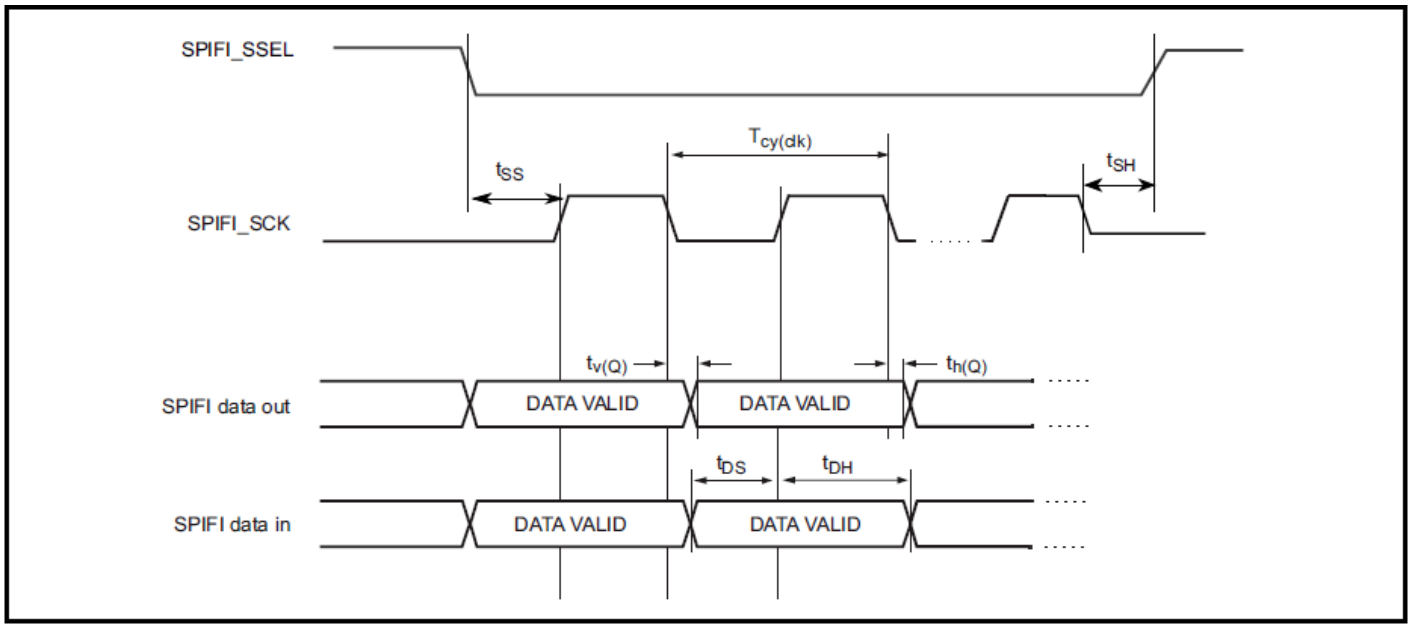


Fig 3. SPIFI interface timings

3.3.4 PWM timing

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
t_{SK}	Output skew time		0	--	10	ns

3.3.5 DMIC timing

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$t_{cy(CLK)}$	DMIC CLK frequency		--	--	2	MHz
	Duty cycle		48	--	52	%
t_{DS}	Data set-up time		25	--	--	ns
t_{DH}	Data hold time		1	--	--	ns

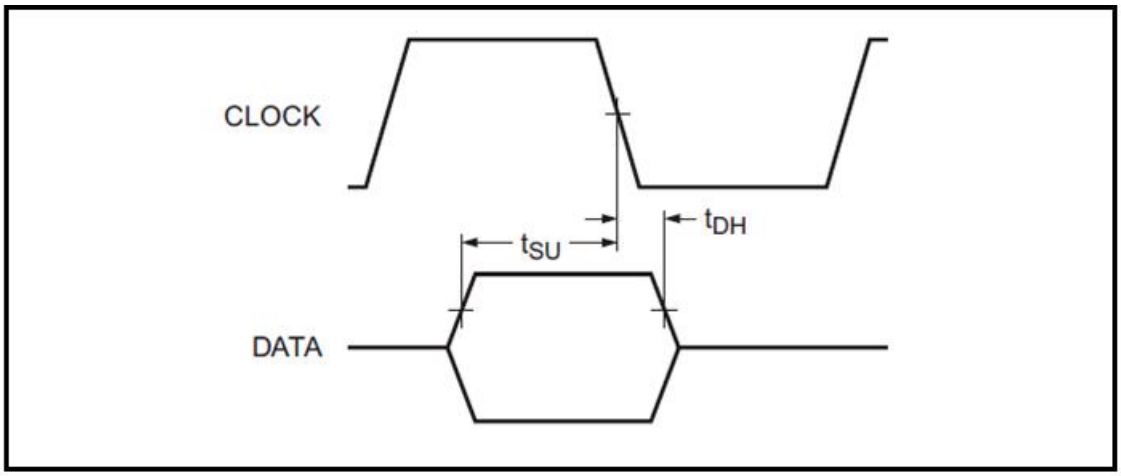


Fig 4. DMIC interface timings

3.3.6 SPI timing

Table 4. SPI master timing

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
t_{DS}	Data set-up time		10	--	--	ns
t_{DH}	Data hold time		5	--	--	ns
$t_{V(Q)}$	Data output valid time		-2	--	15	ns
$t_{cy(SLK)}$	SCK frequency		0.01	--	8	MHz
	Duty cycle		45	50	55	%
t_{SS}	SSEL low before SCK edge[1]		1	--	--	SCK cycles
t_{SH}	SSEL low after last SCK edge[2]		0.5	--	--	SCK cycles

[1] Pre-delay can be configured to increase this time in steps of 1 SCK cycle
[2] Post-delay can be configured to increase this time in steps of 1 SCK cycle

Table 5. SPI slave timing

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
t_{DS}	Data set-up time		12	--	--	ns
t_{DH}	Data hold time		5	--	--	ns
$t_{V(Q)}$	Data output valid time		0	--	35	ns
$t_{cy(SLK)}$	SCK frequency		--	--	8	MHz
t_{SS}	SSEL low before SCK edge[1]		1	--	--	ns
t_{SH}	SSEL low after last SCK edge[2]		0.5	--	--	ns

[1] Pre-delay can be configured to increase this time in steps of 1 SCK cycle
[2] Post-delay can be configured to increase this time in steps of 1 SCK cycle

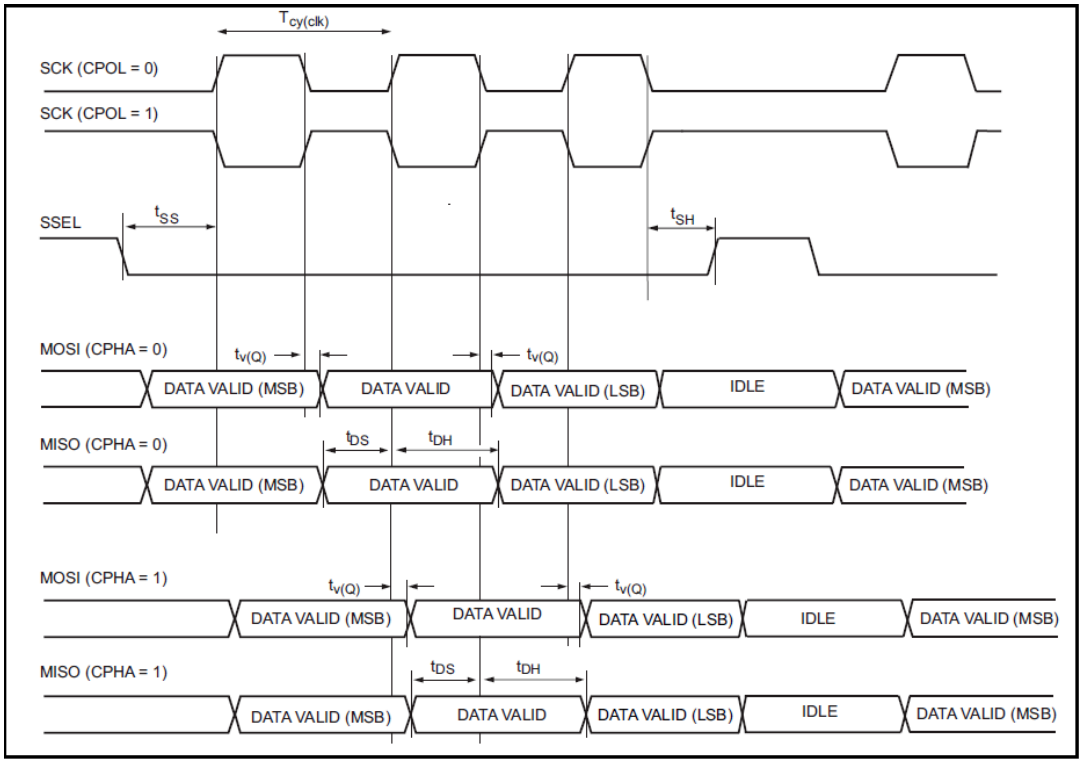


Fig 5. SPI master interface timings

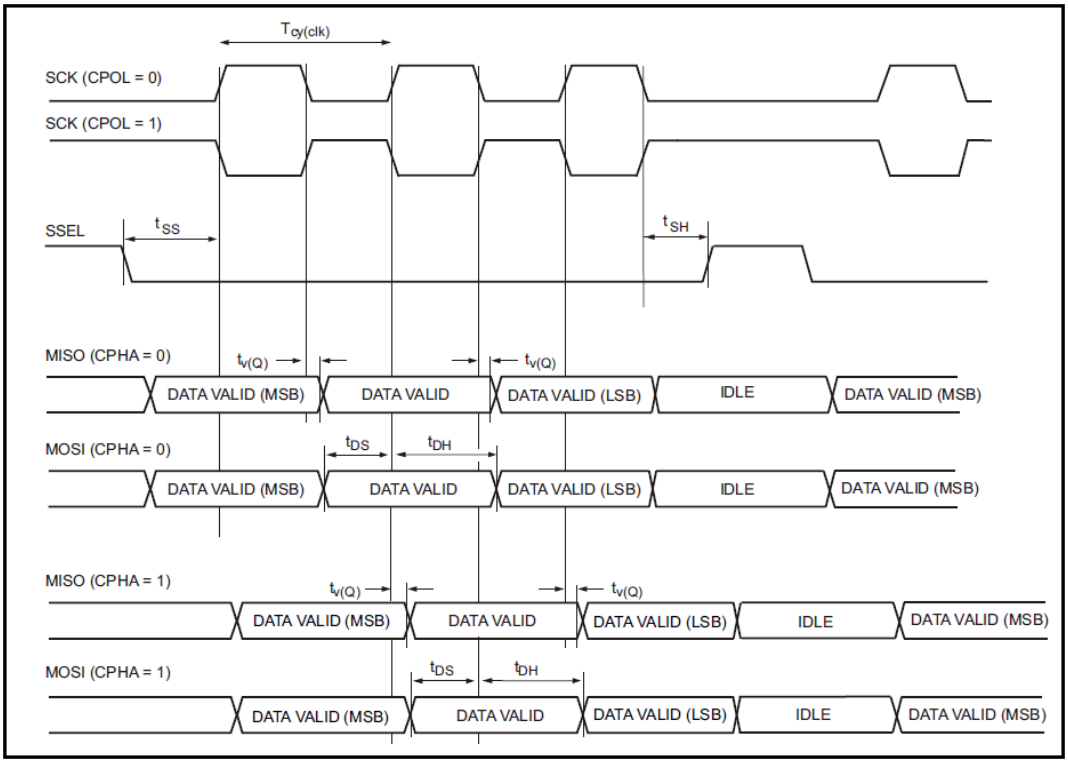


Fig 6. SPI slave interface timings

3.4 Power Consumption*

Zigbee

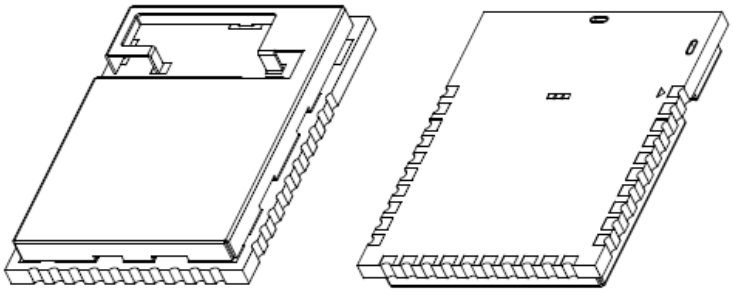
No.	Item	VDD_IN=3.3V		
		Max.	Avg.	Unit.
1	Power deep down*(2)	0.763	0.276	uA
2	Power down mode with no RAM retention *(1)(2)	1.42	0.902	uA
3	Power active with radio Tx 10dBm	15.84	15.82	mA
4	Power active with radio RX	6.33	6.27	mA

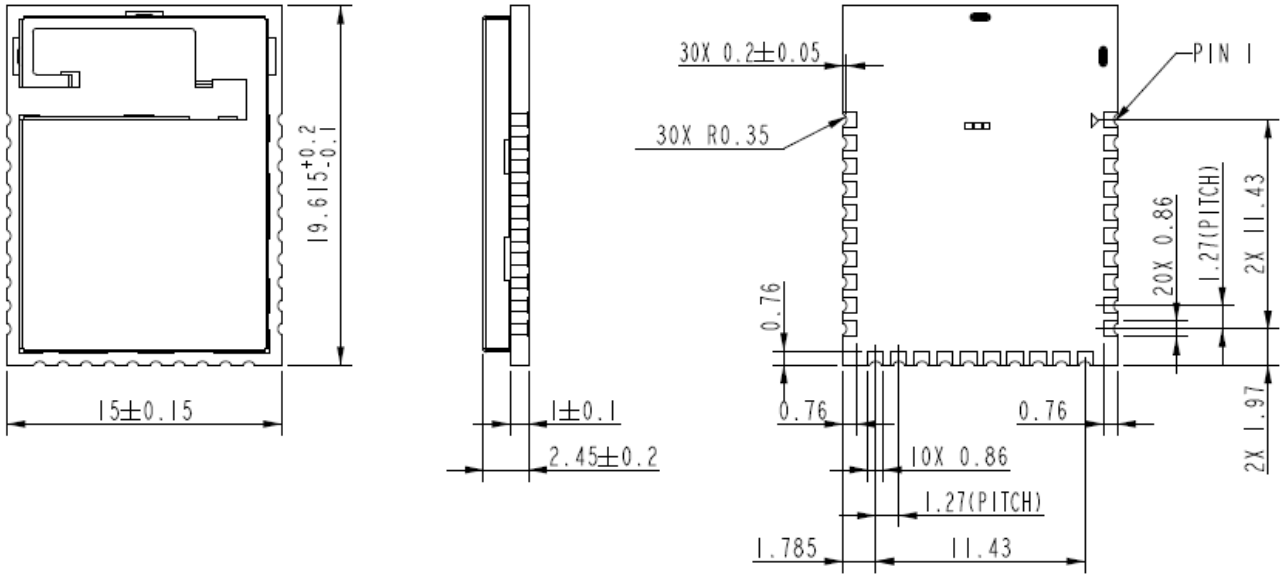
BLE

No.	Item	VDD_IN=3.0V(PIN_22)		
		Max.	Avg.	Unit.
1	Deep power-down (everything is powered off, wake-up on HW reset only)	0.549	0.227	uA
2	Power-Down (wake-up on HW reset or an IO event, wake-up timer ON, 32 kHz FRO on, no SRAM retention).	1.21	0.839	uA
3	Deep Power-Down-IO. Everything is powered off, wake-up on HW reset only or an event on any of the 22 GPIOs and NTAG interrupt) (for K32W061)	0.658	0.347	uA
4	Sleep	2.59	2.24	mA
5	RX Idle	2.69	2.35	mA
6	Advertising mode	2.21	1.89	uA

4. Mechanical Information

4.1 Mechanical Drawing





5. Packaging Information

Tape reel = 1 Box = 700 pcs

Carton = 3 Boxes = 2,100 pcs

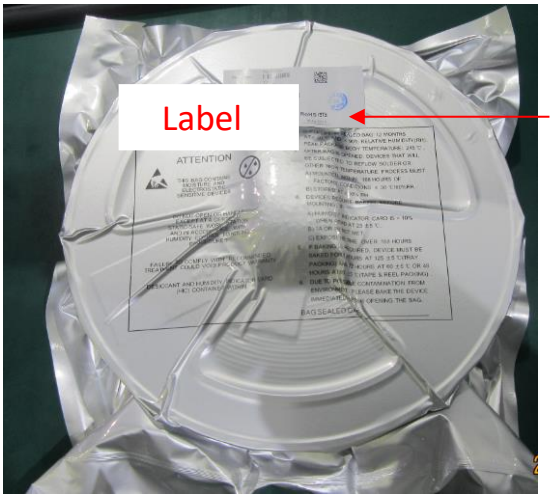
5.1 Tape & Reel Picture

DESICCANT

HUMIDITY INDICATOR CARD

AFFIX PACKING LABEL

5.2 Packing Picture



AFFIX PACKING LABEL

5.3 Inside of Inner Box Picture

PINK BUBBLE WRAP

5.4 Inner Box Picture

AFFIX PACKING LABEL

5.5 Inside of Carton Picture

1 Carton = 3 Boxes

5.6 Carton and Label Picture

AFFIX SHIPPING LABEL

AFFIX PACKING LABEL

AFFIX BOX LABEL