AzureWave Technologies, Inc.

AW-CM520

IEEE 802.11a/b/g/n/ac WLAN with Bluetooth 5 Combo LGA Module

Datasheet

Rev. A

DF

(For Standard)

Features

Wi-Fi

- 1 antennas to support 1(Transmit) × 1(Receive) technology and Bluetooth
- High speed wireless connection up to 433.3Mbps transmit/receive PHY rate using 80MHz bandwidth
- Backward compatibility with legacy 802.11 ac/n/a/g/b technology.
- 20MHz bandwidth/ channel, 40MHz bandwidth/ channel, upper/ lower 20MHz packets in 40MHz channel, 20MHz duplicate legacy packets in 40MHz channel mode operation.
- 80MHz bandwidth/ channel, 4 positions of 20MHz packets in 80MHz channel, upper/ lower 40MHz packets in 80MHz channel, 20MHz quadruplicate legacy packets in 80MHz channel mode operation.
- Dynamic frequency selection (radar detection)
- Enhanced radar detection for long and short pulse radar.
- Enhanced AGC scheme for DFS channel.
- 20/40/80Mhz coexistence with middle-packet detection (GI detection) for enhanced CCA.
- 1 spatial stream STBC reception.
- LDPC transmission and reception for both 802.11n and 802.11ac.
- 256 QAM (MCS 8, 9) modulation, optional support for 802.11ac MCS 9 in 20MHz using LDPC.
- Short guard interval.
- Temporal Ley Integrity Protocol (TKIP)/ Wired Equivalent Privacy (WEP)/ Advanced Encryption Standard (AES)/ Counter-Mode/ CBC-MAC Protocol (CCMP).
- Cipher-Based Message Authentication Code (CMAC)/ WLAN Authentication and Privacy Infrastructure (WAPI).
- External Crystal frequenc

Bluetooth

- Baseband and radio BDR and EDR packet types – 1Mbps (GFSK), 2Mbps (π/4-DQPSK), and 3Mbps (8DPSK).
- Fully qualified Bluetooth BT4.2 and support Bluetooth 5.
- Enhanced Data Rate (EDR) compliant for both 2Mbps and 3Mbps supported.
- High speed UART and PCM for Bluetooth.
- Fully functional Bluetooth baseband-AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening.
- Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER).
- SCO/ eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement.
- Standard Bluetooth power saving mechanisms.
- Automatic ACL packet type selection.
- Full master and slave piconet support.

- Scatternet support.
- Enhanced Power Control (EPC).
- Channel Quality Driven Data Rate (CQDDR).
- Encryption (AES) support.
- Supports link layer topology to be master and slave (connects up to 16 links).
- LE Privacy 1.2
- LE Secure Connection.
- LE Data Length Extension.
- 2 Mbps LE
- Direction Finding – Connectionless Angle of Departure (AoD).
- Direction Finding – Connection – oriented Angle of Arrival (AoA).

Revision History

Document NO: R2-2520-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	**2021/03/09**	**DCN020946**	● **Initial Version**	**JM.Pang**	**Chihhao Liao**

Table of Contents

1. Introduction

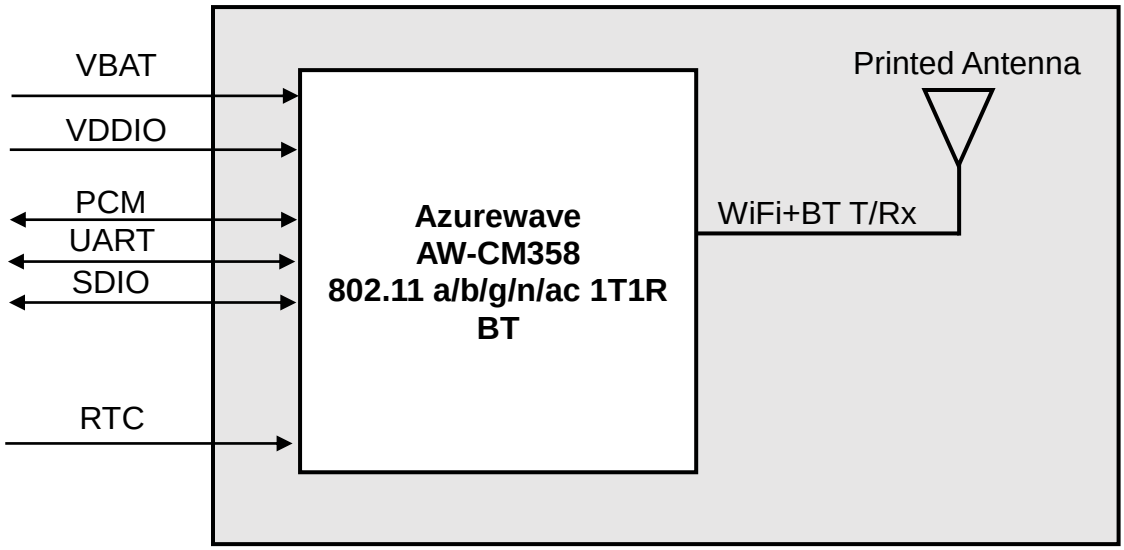
1.1 Product Overview

AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.11 a/b/g/n/ac WIFI with Bluetooth 5 combo SDIO and UART LGA Module --- **AW-CM520.** The AW-CM520 IEEE 802.11 a/b/g/n/ac WIFI with Bluetooth 5 combo module is a highly integrated wireless local area network (WLAN) solution to let users enjoy the digital content through the latest wireless technology without using the extra cables and cords. It combines with Bluetooth 4.2 and provides a complete 2.4GHz Bluetooth system which is fully compliant to Bluetooth 4.2 and v2.1 that supports EDR of 2Mbps and 3Mbps for data and audio communications. It enables a high performance, cost effective, low power, compact solution that easily fits onto the SDIO and UART combo LGA module. Generic interfaces include SDIO 3.0 and high-speed UART interfaces for connecting WLAN and Bluetooth technologies to the host processor.

AW-CM520 uses Direct Sequence Spread Spectrum (DSSS), Orthogonal Frequency Division Multiplexing (OFDM), BPSK, QPSK, CCK and QAM baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM520. In addition to the support of **WPA/WPA2/WPA3** and **WEP** 64-bit and 128-bit encryption, It also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP), AES/Galois/Counter Mode Protocol (GCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP)**, Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms. For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported. The device also supports 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

Wireless home audio and video entertainment systems including DVT, set-top boxes, blue-ray DVD players, media servers, and gaming consoles. Mobile routers and Internet of Things (IoT) gateways. AW-CM520 module adopts NXP’s latest highly-integrated WLAN & Bluetooth SoC---**88W8987**. All the other components are implemented by all means to reach the mechanical specification required.

1.2 Block Diagram



AW-CM520 BLOCK DIAGRAM

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac Wi-Fi with Bluetooth 5 combo LGA module
Major Chipset	NXP 88W8987
Host Interface	WiFi + BT ● SDIO + UART
Dimension	28mm(L) x 18mm(W) x 2.65mm(T)
Form Factor	LGA module, 110 pins
Antenna	1T1R ANT1(Printing Antenna)：WiFi/Bluetooth → TX/RX
Weight	TBD

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac 1T1R
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	WLAN: 2.4 GHz / 5GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9)
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 Japan – 1 ~ 13 802.11g: USA and Canada – 1 ~ 11

<table>
<tr><td></td><td>Most European Countries – 1 ~ 13
802.11n:
USA and Canada – 1 ~ 11
Most European Countries – 1 ~ 13
802.11a:
USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165</td></tr>
<tr><td>Output Power</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)
@EVM<35%</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦-25 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)
@EVM≦-27 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)
@EVM≦-25 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)
@EVM≦-27 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ac (VHT20 MCS8)
@EVM≦-30 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ac (VHT40 MCS9)
@EVM≦-32 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9)
@EVM≦-32 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td></td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td></td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td></td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table>
5G(n/ac packets with LDPC)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td></td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td></td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table></td></tr>
</table>

	11ac (VHT20 MCS8)		TBD	TBD	dBm
	11ac (VHT40 MCS9)		TBD	TBD	dBm
	11ac (VHT80 MCS9)		TBD	TBD	dBm
Data Rate	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: MCS0~7 HT20/HT40 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac: MCS0~8 VHT20 802.11ac: MCS0~9 VHT40/VHT80				
Security	● WPA™- and WPA2™- (Personal) support for powerful encryption and authentication ● AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility ● Wi-Fi Protected Setup (WPS) ● WEP ● CKIP(Software) ● WPA3				

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

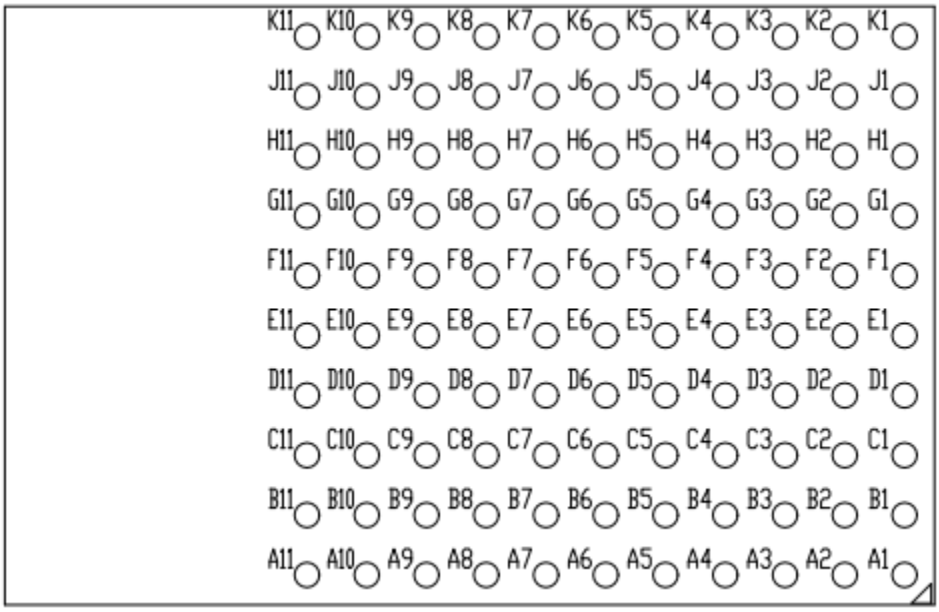
Features	**Description**				
Bluetooth Standard	Bluetooth 2.1+Enhanced Data Rate (EDR)/BT3.0/BT4.2/BT5.0				
Bluetooth VID/PID	N/A				
Frequency Rage	2400~2483.5MHz				
Modulation	GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)				
Output Power		Min	Typ	Max	Unit
	Basic rate	TBD	TBD	TBD	dBm
	LE	TBD	TBD	TBD	dBm
Receiver Sensitivity		Min	Typ	Max	Unit
	DH5		TBD	TBD	dBm
	2DH5		TBD	TBD	dBm
	3DH5		TBD	TBD	dBm
	LE		TBD	TBD	dBm

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT: 3.07~3.53 VIO : 1.8
Operating Temperature	-30°C ~85°C
Operating Humidity	less than 85% R.H.
Storage Temperature	-40°C ~90°C
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

2. Pin Definition

2.1 Pin Map



AW-CM520 Top View Pin Map

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
A1	GND	Ground.		GND
A2	SDIO_DATA1	SDIO Data Line 1.	VDDIO	I/O
A3	SDIO_DATA0	SDIO Data Line 0.	VDDIO	I/O
A4	SDIO_DATA_CLK	SDIO Clock Input.	VDDIO	I
A5	SDIO_DATA_CMD	SDIO Command Input.	VDDIO	I/O
A6	SDIO_DATA3	SDIO Data Line 3.	VDDIO	I/O
A7	SDIO_DATA2	SDIO Data Line 2.	VDDIO	I/O
A8	WL_HOST_WAKE	WLAN to wake-up HOST		O
A9	PDn	Power up/ down internal regulators. 0 = full power-down mode 1 = normal mode Default pull high in module internal		I
A10	VBAT	3.3V power pin	3.3V	VCC
A11	VBAT	3.3V power pin	3.3V	VCC
B1	GND	Ground.		GND
B2	GND	Ground.		GND
B3	GND	Ground.		GND
B4	GND	Ground.		GND
B5	GND	Ground.		GND
B6	GND	Ground.		GND
B7	GND	Ground.		GND
B8	GND	Ground.		GND
B9	NC	Floating Pin, No connect to anything		Floating
B10	GND	Ground.		GND
B11	GND	Ground.		GND

C1	GND	Ground.		GND
C2	GND	Ground.		GND
C3	GND	Ground.		GND
C4	GND	Ground.		GND
C5	GND	Ground.		GND
C6	GND	Ground.		GND
C7	GND	Ground.		GND
C8	GND	Ground.		GND
C9	GND	Ground.		GND
C10	GND	Ground.		GND
C11	GND	Ground.		GND
D1	GND	Ground.		GND
D2	GND	Ground.		GND
D3	GND	Ground.		GND
D4	GND	Ground.		GND
D5	GND	Ground.		GND
D6	GND	Ground.		GND
D7	GND	Ground.		GND
D8	GND	Ground.		GND
D9	GND	Ground.		GND
D10	GND	Ground.		GND
D11	GND	Ground.		GND
E1	SUSCLK_IN	External 32K or RTC clock		I
E2	GND	Ground.		GND
E3	GND	Ground.		GND
E4	GND	Ground.		GND

E5	GND	Ground.		GND
E6	GND	Ground.		GND
E7	GND	Ground.		GND
E8	GND	Ground.		GND
E9	GND	Ground.		GND
E10	GND	Ground.		GND
E11	GND	Ground.		GND
F1	BT_PCM_OUT	PCM data out		O
F2	NC	Floating Pin, No connect to anything		Floating
F3	GND	Ground.		GND
F4	GND	Ground.		GND
F5	GND	Ground.		GND
F6	GND	Ground.		GND
F7	GND	Ground.		GND
F8	GND	Ground.		GND
F9	GND	Ground.		GND
F10	GND	Ground.		GND
F11	GND	Ground.		GND
G1	BT_PCM_CLK	PCM Clock		I/O
G2	NC	Floating Pin, No connect to anything		Floating
G3	GND	Ground.		GND
G4	GND	Ground.		GND
G5	GND	Ground.		GND
G6	GND	Ground.		GND
G7	GND	Ground.		GND
G8	GND	Ground.		GND

G9	GND	Ground.		GND
G10	GND	Ground.		GND
G11	GND	Ground.		GND
H1	BT_PCM_IN	PCM data Input		I
H2	GND	Ground.		GND
H3	GND	Ground.		GND
H4	GND	Ground.		GND
H5	GND	Ground.		GND
H6	GND	Ground.		GND
H7	GND	Ground.		GND
H8	GND	Ground.		GND
H9	GND	Ground.		GND
H10	GND	Ground.		GND
H11	GND	Ground.		GND
J1	BT_PCM_SYNC	PCM Synchronization control		O
J2	GND	Ground.		GND
J3	HOST_WL_WAKE	Host wake-up WLAN device		Floating
J4	NC	Floating Pin, No connect to anything		Floating
J5	NC	Floating Pin, No connect to anything		Floating
J6	NC	Floating Pin, No connect to anything		Floating
J7	NC	Floating Pin, No connect to anything		Floating
J8	NC	Floating Pin, No connect to anything		Floating
J9	BT_WAKE_HOST	Bluetooth device to wake-up Host		O
J10	GND	Ground.		GND
J11	GND	Ground.		GND
K1	GND	Ground.		GND

K2	VDDIO	1.8V VDDIO supply for WLAN and Bluetooth	1.8V	VCC
K3	NC	Floating Pin, No connect to anything		Floating
K4	HOST_WAKE_BT	Host wake-up Bluetooth device		I
K5	NC	Floating Pin, No connect to anything		Floating
K6	UART_RTS_N	High-Speed UART RTS		O
K7	UART_TXD	High-Speed UART Data Out		O
K8	UART_RXD	High-Speed UART Data In		I
K9	UART_CTS_N	High-Speed UART CTS		I
K10	GND	Ground.		GND
K11	GND	Ground.		GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	2.5	3.3	4.0	V
VDDIO	DC supply voltage for digital I/O		1.8	2.2	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	3.07	3.3	3.53	V
VDDIO	DC supply voltage for digital I/O	1.67	1.8	1.98	V

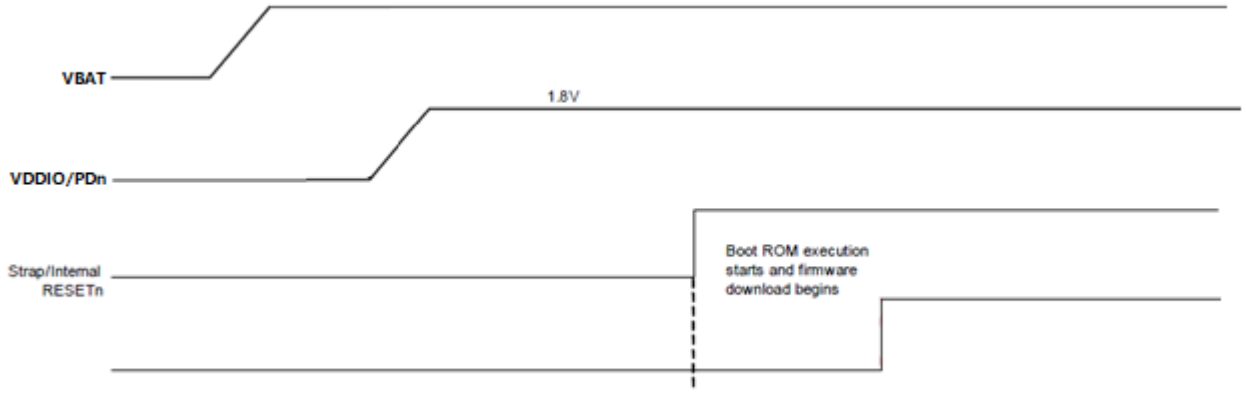
3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital I/O pins, VDDIO=1.8V					
V_{IH}	Input high voltage	1.26	-	2.2	V
V_{IL}	Input low voltage	-0.4	-	0.54	V
V_{OH}	Output high voltage	1.4	-	-	V
V_{OL}	Output Low Voltage	-	-	0.4	V

3.4 Host Interface

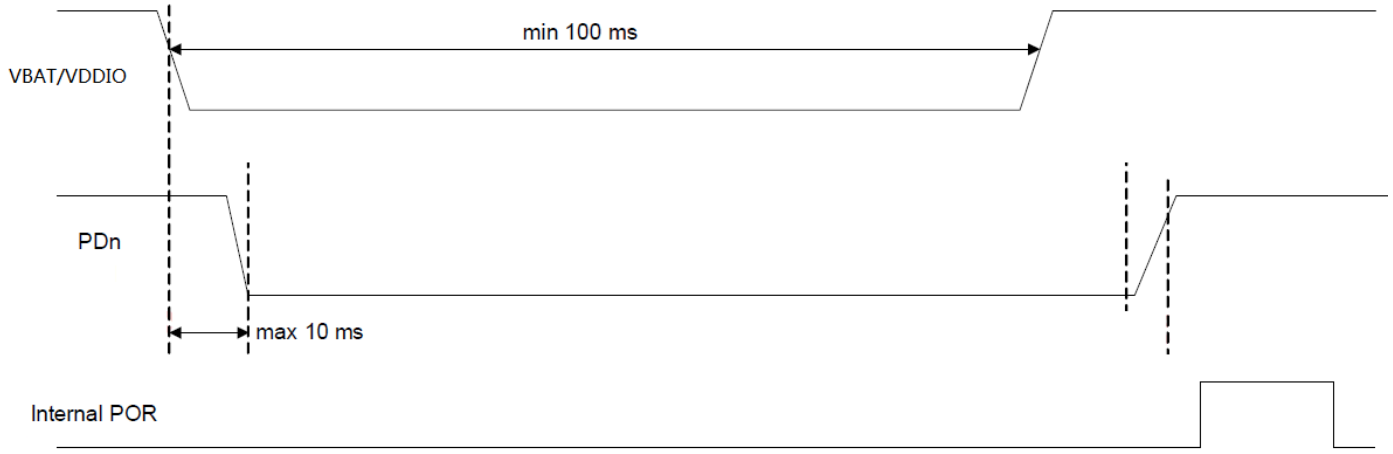
Power-up Sequence

VDDIO/Pdn no specific time requirement, just need to follow up the power on sequence waveform.



Power-down Sequence

The table is AW-CM520 module power down sequence, the maximum ramp-down time for PDn from VBAT assertion is 10ms.VBAT must be asserted a minimum of 100 ms to guarantee that PDn are discharged to less than 0.2V for the POR generate properly after VBAT is deasserted.



3.4.1 SDIO Interface

The AW-CM520 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-CM520 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the frvice through the use of BARs and a DMA engine.

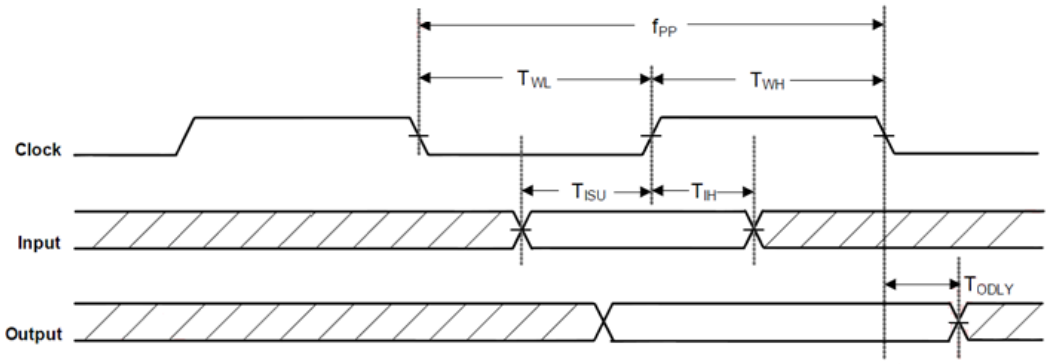
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.

SDIO Interface Signals

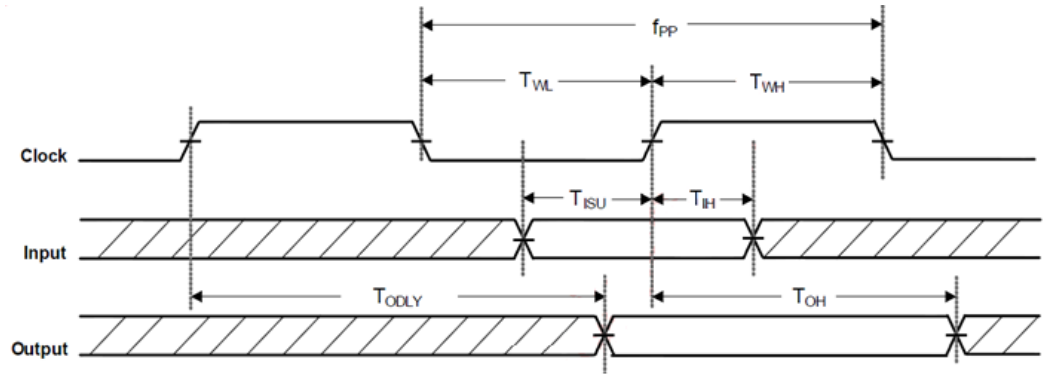
AW-CM520 SDIO Pin Name	Type	Description
SDIO_DATA_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_DATA_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA_3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA_2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA_1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA_0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

Default Speed, High-Speed Modes

SDIO Protocol Timing Diagram – Default Speed Mode



SDIO Protocol Timing Diagram – High Speed Mode

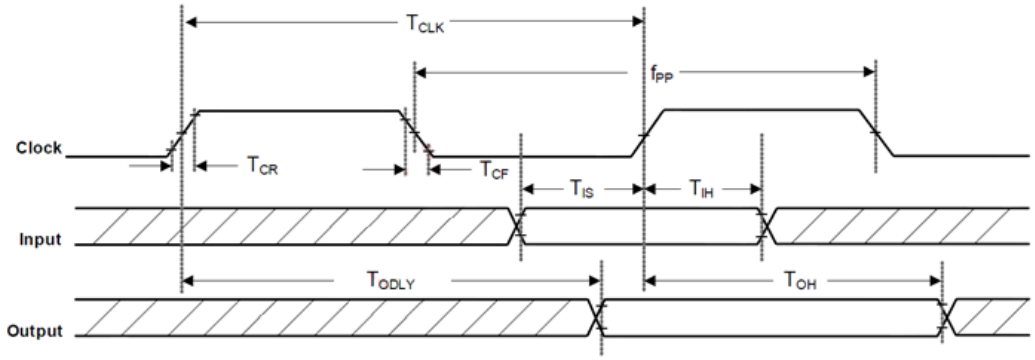


SDIO Timing Data- Default Speed, High-Speed Modes

Symbol	Parameter	Condition	Min	Max	Units
f_{pp}	CLK Frequency	Normal	0	25	MHz
		High Speed	0	50	
t_{WL}	CLK low Time	Normal	10	-	
		High Speed	7	-	
t_{WH}	CLK High Time	Normal	10	-	
		High Speed	7	-	
t_{ISU}	Input Setup Time	Normal	5	-	
		High Speed	6	-	
t_{IH}	Input Hold Time	Normal	5	-	
		High Speed	2	-	
t_{ODLY}	Output Delay Time	Normal	-	14	
		High Speed	-	14	
T_{OH}	Output hold time	High Speed	2.5		

1. For SDIO 2.0 running at 50MHz clock frequency, only 1.8V is supported.
2. For SDIO 2.0 running at 25MHz clock frequency, 1.8V is supported.

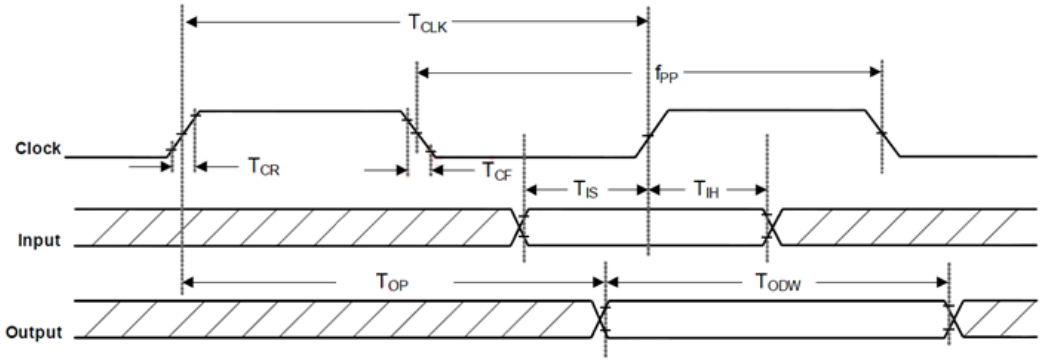
SDIO Protocol Timing Diagram – SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)



SDIO Timing Data- SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	-	-	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	-	-	ns
T_{CLK}	Clock time	SDR12/25/50	10	-	40	ns
T_{CR}, T_{CF}	Rise time, fall time	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output hold time	SDR12/25/50	1.5	-	-	ns

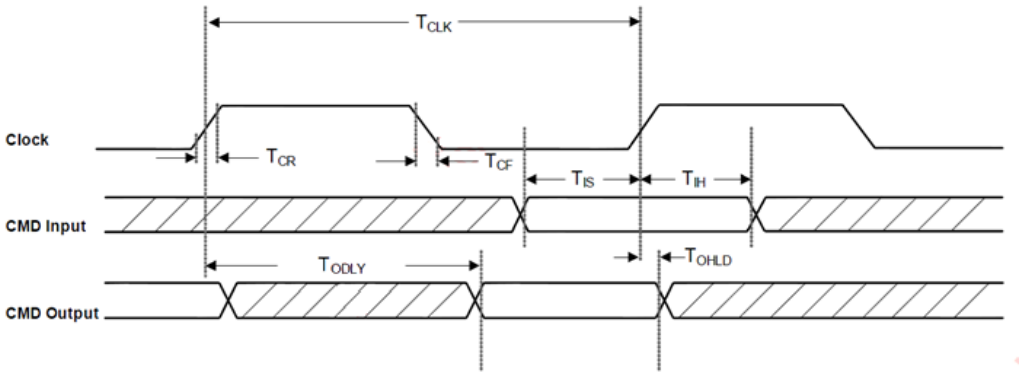
SDIO Protocol Timing Diagram – SDR104 Mode (208MHz)



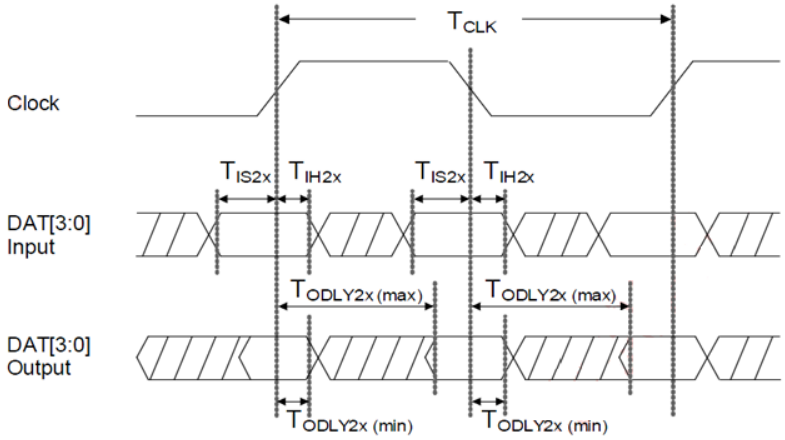
SDIO Timing Data- SDR104 Mode (208MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	CLK Frequency	SDR104	0	-	208	MHz
T_{IS}	Input setup time	SDR104	1.4	-	-	ns
T_{IH}	Input hold time	SDR104	0.8	-	-	ns
T_{CLK}	Clock time	SDR104	4.8	-		ns
T_{CR}, T_{CF}	Rise time, fall time	SDR104	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time	SDR104	0	-	10	ns
T_{OH}	Output hold time	SDR104	2.88	-	-	ns

SDIO CMD Timing Diagram – DDR50 Mode (50MHz)



SDIO SAT [3:0] Timing Diagram – SDR50 Mode (50MHz)



SDIO Timing Data- DDR50 Mode (50MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time	DDR50	20	-	-	ns
T_{CR}, T_{CF}	Rise time, fall time	DDR50	-	-	0.2*T_{CLK}	Ns
Clock Duty		DDR50	45	-	55	%
CMD Input						
T_{IS}	Input setup time	DDR50	6	-	-	ns
T_{IH}	Input hold time	DDR50	0.8	-	-	ns
CMD Output						
T_{ODLY}	Output delay time during data transfer mode	DDR50	-	-	13.7	ns
T_{OHLD}	Output hold time	DDR50	1.5	-	-	ns
DAT [3:0] Input						
T_{IS2X}	Input hold time	DDR50	3	-	-	ns
T_{IH2X}	Input hold time	DDR50	0.8	-	-	ns
DAT [3:0] Output						
$T_{ODLY2X(max)}$	Output delay time during data transfer mode	DDR50	-	-	7	ns
$T_{ODLY2X(min)}$	Output hold time	DDR50	1.5	-	-	ns

3.4.2 UART Interface

High-Speed UART interface

The AW-CM520 supports a high-speed Universal Asynchronous Receiver/ Transmitter (UART) interface, compliant to the industry standard 16550 specification.

- FIFO mode permanently selected for transmit and receive operations.
- 2 pins for transmit and receive operations.
- 2 flow control pins.
- Interrupt triggers for low-power, internal CPU (for debug purposes).
- Support diagnostic tests.
- Support data input/ output operations for peripheral devices connected through a standard UART interface.

UART Interface Signals

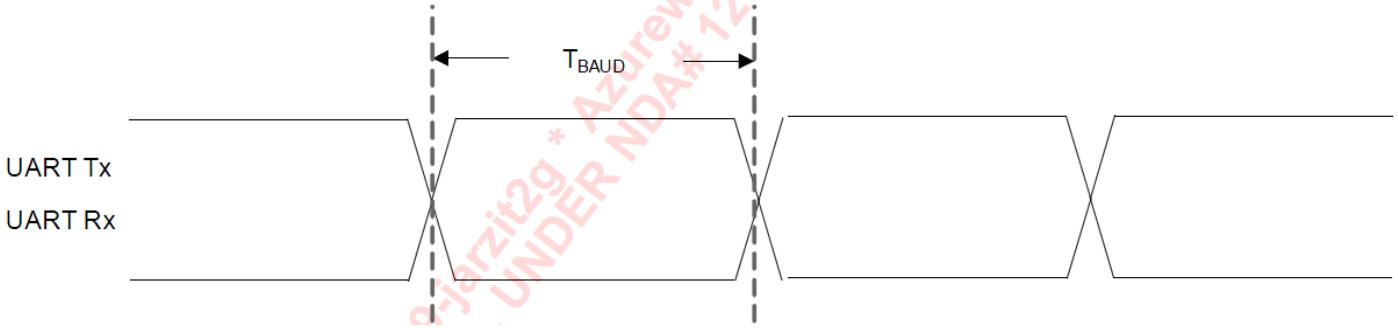
Pin Number	Signal Name	16550 Standard Name	Type	Description
K7	UART_TXD	SOUT	O	Serial data
K8	UART_RXD	SIN	I	Serial data
K9	UART_CTSn	CTSn	I	Clear To Send
K6	UART_RTSn	RTSn	O	Request To Send

UART Baud Rates Supported

Baud Rate				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	-

The UART Tx and Rx pins are powered from the VDDIO voltage supply.

UART Timing Diagram



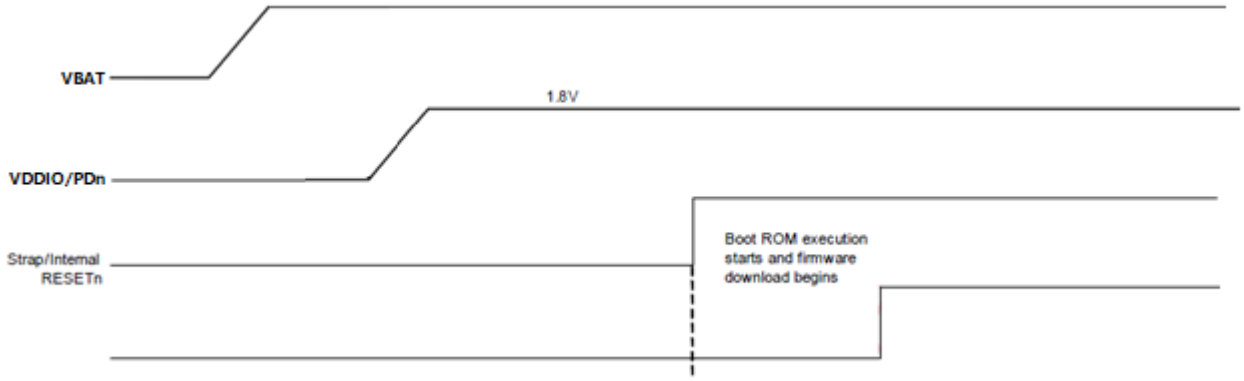
UART Timing Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
TBAUD	Baud rate	38.4MHz input clock	250	-	-	ns

3.5 Power up Timing Sequence

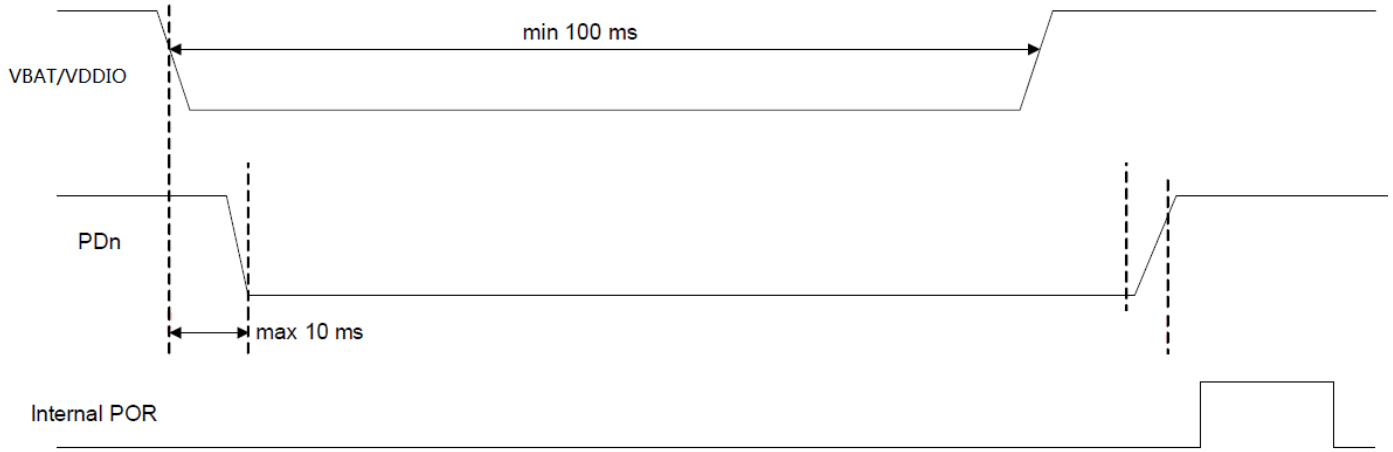
Power-up Sequence

VDDIO/Pdn no specific time requirement, just need to follow up the power on sequence waveform.



Power-down Sequence

The table is AW-CM520 module power down sequence, the maximum ramp-down time for PDn from VBAT assertion is 10ms.VBAT must be asserted a minimum of 100 ms to guarantee that PDn are discharged to less than 0.2V for the POR generate properly after VBAT is deasserted.



3.6 Power Consumption*

3.6.1 WLAN

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

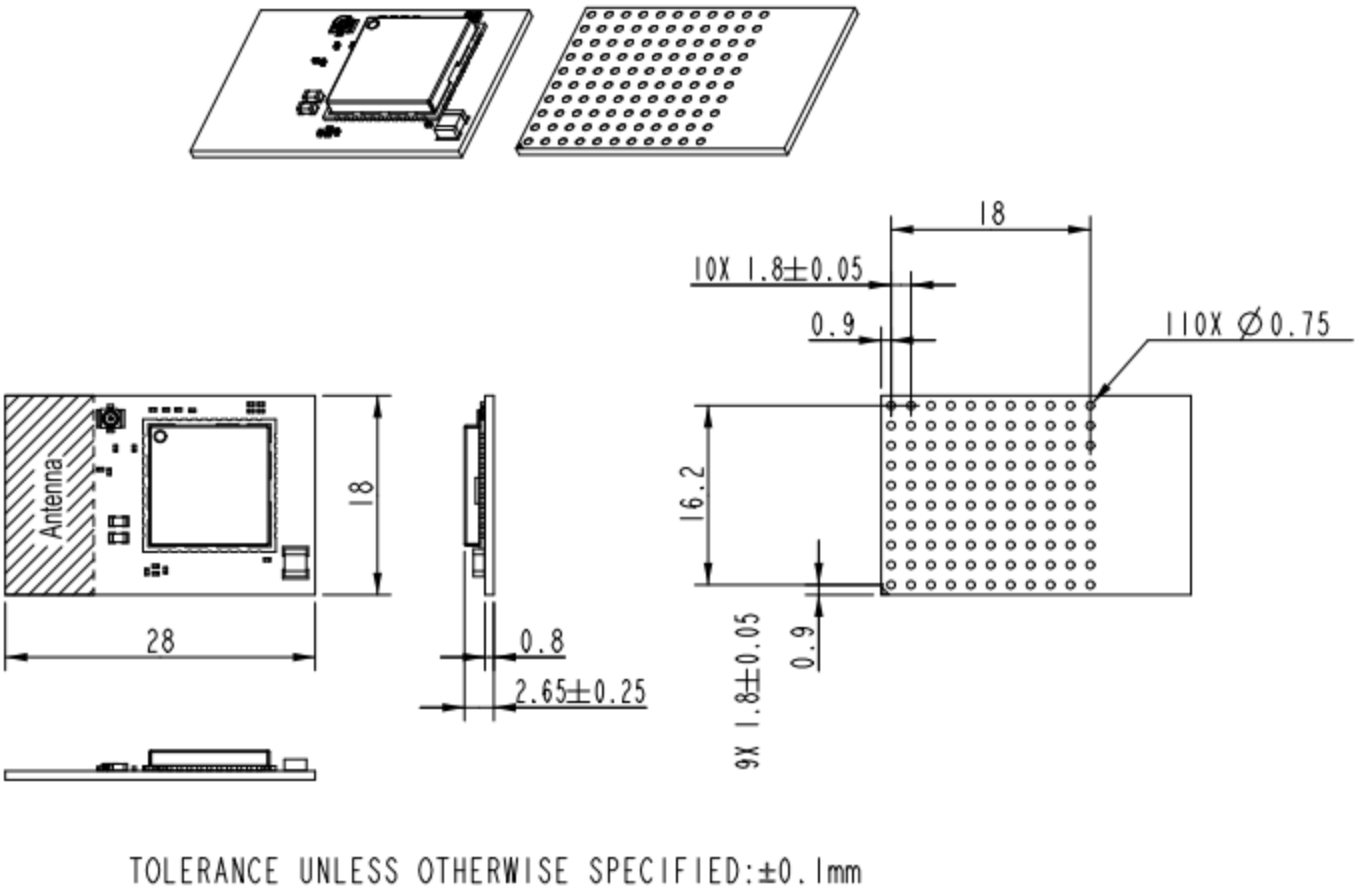
3.6.2 Bluetooth

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

5. Packaging Information

TBD