AzureWave Technologies, Inc.

# AW-CM389NF

## IEEE 802.11 a/b/g/n/ac 2x2 MIMO Wi-Fi with Bluetooth 5.0 Combo Module

## Datasheet

**Rev. E**

**0B**

**(For Standard)**

# Features

## WLAN

- IEEE 802.11ac compliant, 2x2 MIMO spatial stream with data rates up to MCS9 (866.7 Mbps).
- SDIO 3.0, G-SPI, USB interfaces support for WLAN.
- IEEE 802.11i for advanced security.
- Quality of Service (QoS) support for multimedia applications
- Multiple power saving modes for low power consumption.
- SDIO 3.0 device interface may be used as host interface for WLAN/Bluetooth.
- Drip-in WLAN Linux drivers are Android ready and validated on Android based systems.
- Simultaneous AP-STA.
- Support China WAPI.

## Bluetooth

- Bluetooth 5.0 complaint with Bluetooth 2.1 + Enhanced Data Rate (EDR).
- High speed UART, PCM/Inter-IC Sound (I2S) and SDIO3.0, USB for Bluetooth.
- Baseband and radio BDR and EDR packet types – 1Mbps (GFSK), 2Mbps (π/4-DQPSK), and 3Mbps (8DPSK).
- Standard Bluetooth power saving mechanisms.
- WLAN/Bluetooth Coexistence (BCA) protocol support.
- Enhanced low-power scan mode.
- Support for BlueZ v4.47 Bluetooth profiles stack used in Android Éclair.
- Audio Codec interface support.
- Cellular phone co-existence support.

# Revision History

Document NO: R2-1280NF-DST-01

| Version | Revision Date | DCN NO. | Description | Initials | Approved |
|---|---|---|---|---|---|
| A | 2019/10/23 | DCN016183 | Update datasheet format | Grace Liu | N.C Chen |
| B | 2020/06/16 | DCN017550 | Remove watermark | Grace Liu | N.C Chen |
| C | 2020/09/01 | DCN018170 | Change IC vender name from Marvell to NXP | Grace Liu | N.C Chen |
| D | 2020/11/18 | DCN019205 | 1. Modify title of cover page<br>2. Update Bluetooth from 4.2 to 5.0 | Grace Liu | N.C Chen |
| E | 2021/04/16 | DCN021417 | Change format | Grace Liu | N.C Chen |
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# 1. Introduction

## 1.1 Product Overview

**AzureWave Technologies, Inc.** introduces the IEEE 802.11 a/b/g/n/ac 2x2 MIMO Wi-Fi with Bluetooth 5.0 Combo Module --- **AW-CM389NF**. The module is targeted to mobile devices including **Notebook, TV, Tablet and Gaming Device** which need small package module, low power consumption, multiple interfaces and OS support. By using AW-CM389NF, the customers can easily enable the Wi-Fi, and BT embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11ac/a/b/g/n standard, the AW-CM389NF uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM389NF. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, the AW-CM389NF also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP)**, Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms.

For the video, voice and multimedia applications the AW-CM389NF support **802.11e Quality of Service** (**QoS).** The device also supports **802.11h Dynamic Frequency Selection (DFS)** for detecting radar pulses when operating in the 5GHz range.

For Bluetooth operation, AW-CM389NF is **Bluetooth 5.0 (supports Low Energy).**

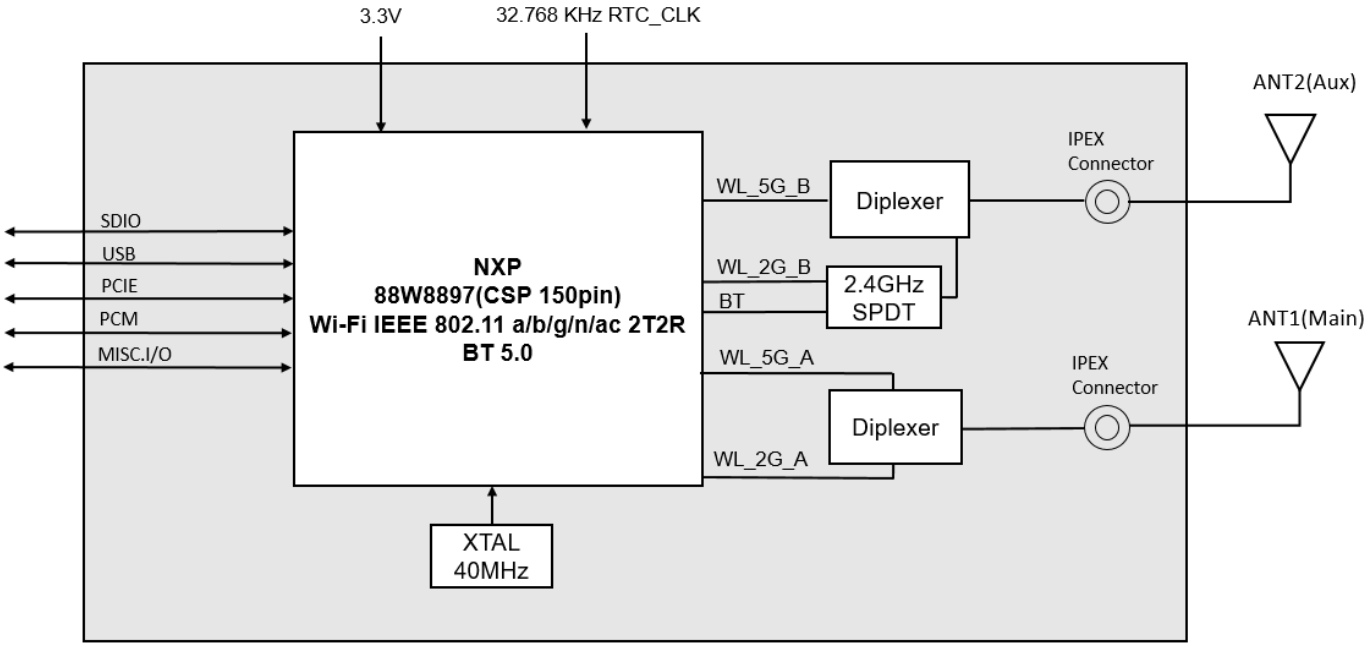
AW-CM389NF supports **SDIO, PCIE, USB,** and high speed **UART interfaces** for WLAN and Bluetooth to the host processor.

AW-CM389NF is suitable for multiple mobile processors for different applications with the support **cellular phone co-existence**.

AW-CM389NF module adopts NXP’s latest highly-integrated dual-band WLAN & Bluetooth SoC---**88W8897**. All the other components are implemented by all means to reach the mechanical specification required.

## 1.2 Block Diagram

A simplified block diagram of the AW-CM389NF module is depicted in the figure below.




**AW-CM389NF Block Diagram**

## 1.3 Specifications Table

### 1.3.1 General

| Features | Description |
|---|---|
| **Product Description** | IEEE 802.11 a/b/g/n/ac 2x2 MIMO Wi-Fi with Bluetooth 5.0 Combo Module |
| **Major Chipset** | NXP 88W8897 (CSP) |
| **Host Interface** | Wi-Fi + BT<br>SDIO+SDIO |
| **Dimension** | 12 mm X 16 mm x 1.4 mm(Max) |
| **Form factor** | M.2 1216 |
| **Antenna** | I-PEX MHF4 Connector Receptacle<br>ANT1(Main)：Main : Wi-Fi<br>ANT2(Aux)：Aux : Wi-Fi + Bluetooth |
| **Weight** | 0.514g |

### 1.3.2 WLAN

| Features | Description |
|---|---|
| **WLAN Standard** | IEEE 802.11 a/b/g/n/ac, Wi-Fi compliant |
| **WLAN VID/PID** | N/A |
| **WLAN SVID/SPID** | N/A |
| **Frequency Rage** | 2.4 GHz ISM Bands 2.412-2.472 GHz<br>5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe<br>5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe<br>5.47-5.725 GHz for Europe<br>5.725-5.825 GHz (FCC UNII-high band) for US/Canada |
| **Modulation** | DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-QAM |
| **Number of Channels** | 2.4GHz:<br>■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11<br>■ China, Australia, Most European Countries - 1 ~ 13<br>■ Japan - 1 ~ 13<br><br>5GHz:<br>■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,1 |

<table>
<tr><td></td><td>40,149,153,157,161,165<br>■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140<br>■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power (Board Level Limit)*</td><td>
2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps) @EVM<35%</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11g (54Mbps) @EVM≦-27 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps) @EVM≦-27 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7) @EVM≦-28 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7) @EVM≦-28 dB</td><td>8</td><td>10</td><td>12</td><td>dBm</td></tr>
<tr><td>11ac (VHT20 MCS8) @EVM≦-30 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
<tr><td>11ac (VHT40 MCS9) @EVM≦-32 dB</td><td>8</td><td>10</td><td>12</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9) @EVM≦-32 dB</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-83</td><td>-80</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-72</td><td>-69</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-68</td><td>-65</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-65</td><td>-62</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-67</td><td>-64</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-67</td><td>-64</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-64</td><td>-61</td><td>dBm</td></tr>
<tr><td>11ac (VHT20 MCS8)</td><td>-</td><td>-59</td><td>-56</td><td>dBm</td></tr>
<tr><td>11ac (VHT40 MCS9)</td><td>-</td><td>-54</td><td>-51</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9)</td><td>-</td><td>-54</td><td>-51</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:<br>802.11b : 1, 2, 5.5, 11Mbps<br>802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps<br>802.11ac/n : MIMO with maximum data rates up to 192.6Mbps<br>( supports MCS9 in 20 MHz using LDPC, 20 MHz channel), 400Mbps (40 MHz channel), 866.7Mbps (80 MHz channel)</td></tr>
<tr><td>Security</td><td>■ WAPI<br>■ WEP 64-bit and 128-bit encryption with H/W TKIP processing<br>■ WPA/WPA2 (Wi-Fi Protected Access)<br>■ AES-CCMP hardware implementation as part of 802.11i security standard</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

## 1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>BLE.2.1 + EDR<br>Bluetooth 5.0</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK<br>Payload 2M: π/4-DQPSK<br>Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>-6</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>-6</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

| | | | | | |
|---|---|---|---|---|---|
| **Receiver Sensitivity** | BT Sensitivity (BER<0.1%) | | | | |
| | | Min | Typ | Max | Unit |
| | BDR(DH1) | - | -86 | -70 | dBm |
| | EDR(3DH5) | - | -84 | -70 | dBm |

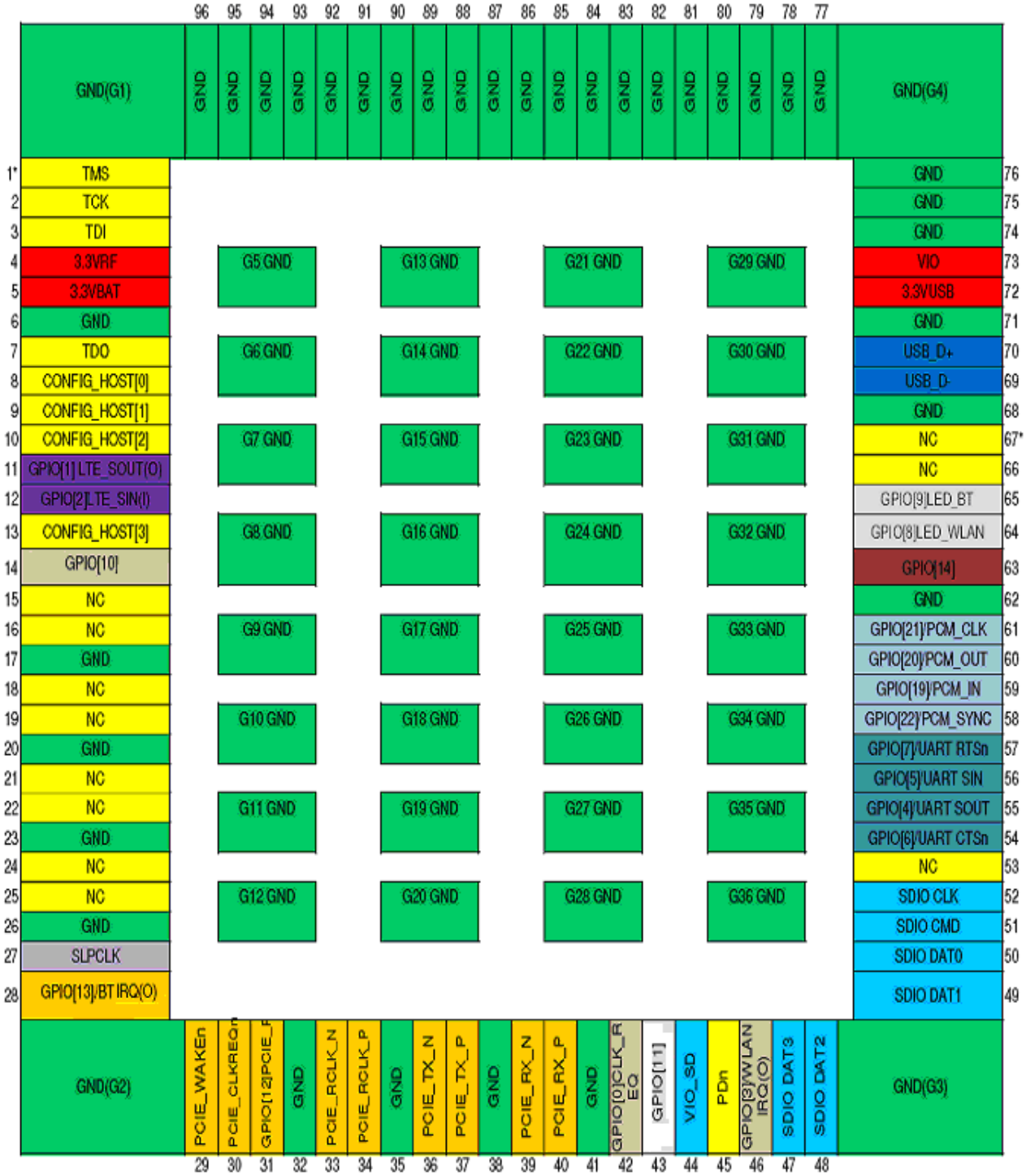
## 1.3.4 Operating Conditions

| Features | Description |
|---|---|
| **Operating Conditions** | |
| **Voltage** | 3.3V |
| **Operating Temperature** | -30 ℃ to +85 ℃ |
| **Operating Humidity** | Less than 85% R.H. |
| **Storage Temperature** | -40 ℃ to +85 ℃ |
| **Storage Humidity** | Less than 60% R.H. |
| **ESD Protection** | |
| **Human Body Model** | N/A<br>±1KV (MIL-STD-883H Method 3015.8) |
| **Changed Device Model** | N/A<br>±500V (JEDEC EIA/JESD22-C101E) |

# 2. Pin Definition

## 2.1 Pin Map

AW-CM389NF pin map (top view).



## 2.2 Pin Table

| Pin No | Definition | Basic Description | Voltage | Type |
|---|---|---|---|---|
| **1** | TMS | JTAG controller select | VIO | I/O |
| **2** | TCK | JTAG test clock | VIO | I/O |
| **3** | TDI | JTAG test data(input) | VIO | O |
| **4** | 3.3V | 3.3V Analog RF Power Supply | 3.3V | Power |
| **5** | 3.3V | 3.3V VBAT system power supply input | 3.3V | Power |
| **6** | GND | System Ground Pin | -- | -- |
| **7** | TDO | JTAG test data(output) | VIO | O |
| **8** | CONFIG_HOST[0] | Configuration : CONFIG_HOST[0] | 1.8V | I |
| **9** | CONFIG_HOST[1] | Configuration : CONFIG_HOST[1] | 1.8V | I |
| **10** | CONFIG_HOST[2] | Configuration : CONFIG_HOST[2] | 1.8V | I |
| **11** | GPIO[1]/LTE_SOUT | UART_LTE_SOUT (output) | VIO | O |
| **12** | GPIO[2]/LTE_SIN | UART_LTE_SIN (input) | VIO | I |
| **13** | CONFIG_HOST[3] | Configuration : CONFIG_HOST[3] | 1.8V | I |
| **14** | GPIO[10] | GPIO[10] (input/output) | VIO | I/O |
| **15** | NC | No Connect | -- | -- |
| **16** | NC | No Connect | -- | -- |
| **17** | GND | System Ground Pin | -- | -- |
| **18** | NC | No Connect | -- | -- |
| **19** | NC | No Connect | -- | -- |
| **20** | GND | System Ground Pin | -- | -- |
| **21** | NC | No Connect | -- | -- |
| **22** | NC | No Connect | -- | -- |
| **23** | GND | System Ground Pin | -- | -- |
| **24** | NC | No Connect | -- | -- |
| **25** | NC | No Connect | -- | -- |

| | | | | |
|---|---|---|---|---|
| **26** | GND | System Ground Pin | -- | -- |
| **27** | SLP_CLK | Sleep Clock Input<br>Used for WLAN and Bluetooth low-power modes. External sleep clock of 32.768 KHz must be used for auto reference clock calibration and for WLAN/Bluetooth low power operation. | VIO | I |
| **28** | GPIO[13]/BT IRQ(O) | GPIO[13] (input/output) | VIO | I/O |
| **29** | PCIE_WAKEn | PCIe wake signal (output) (active low) | VIO | O |
| **30** | PCIE_CLKREQn | PCIe clock request (input/output) (active low) | VIO | I/O |
| **31** | GPIO[12]/PCIE_PERSTn | PCIe host indication to reset the device (input) (active low) | VIO | I |
| **32** | GND | System Ground Pin | -- | -- |
| **33** | PCIE_RCLK_N | PCI Express Differential Clock Input—Negative | 1.8V | I |
| **34** | PCIE_RCLK_P | PCI Express Differential Clock Input—Positive | 1.8V | I |
| **35** | GND | System Ground Pin | -- | -- |
| **36** | PCIE_TX_N | PCI Express Transmit Data—Negative | 1.8V | O |
| **37** | PCIE_TX_P | PCI Express Transmit Data—Positive | 1.8V | O |
| **38** | GND | System Ground Pin | -- | -- |
| **39** | PCIE_RX_N | PCI Express Receive Data—Negative | 1.8V | I |
| **40** | PCIE_RX_P | PCI Express Receive Data—Positive | 1.8V | I |
| **41** | GND | System Ground Pin | -- | -- |
| **42** | GPIO[0]/CLK_REQ | GPIO[0] (input/output) | VIO | I/O |
| **43** | GPIO[11] | GPIO[11] (input/output) | VIO | I/O |
| **44** | VIO_SD | 1.8V/3.3V Digital I/O SDIO Power Supply | 1.8V/3.3V | Power |
| **45** | PDn | Full Power Down (input) (active low) | 3.3V | I |
| **46** | GPIO[3]/WLAN IRQ(O) | GPIO[3] (input/output) | VIO | I/O |
| **47** | SD_DAT[3] | SDIO Data line Bit[3] | VIO_SD | I |
| **48** | SD_DAT[2] | SDIO Data line Bit[2] | VIO_SD | I |
| **49** | SD_DAT[1] | SDIO Data line Bit[1] | VIO_SD | I |

| | | | | |
|---|---|---|---|---|
| **50** | SD_DAT[0] | SDIO Data line Bit[0] | VIO_SD | I |
| **51** | SD_CMD | SDIO Command/response (input/output) | VIO_SD | I |
| **52** | SD_CLK | SDIO Clock input | VIO_SD | I |
| **53** | NC | No Connect | -- | -- |
| **54** | GPIO[6] | UART_CTSn (input) | VIO | I |
| **55** | GPIO[4] | UART_SOUT (output) | VIO | O |
| **56** | GPIO[5] | UART_SIN (input) | VIO | I |
| **57** | GPIO[7] | UART_RTSn (output) | VIO | O |
| **58** | GPIO[22]/PCM_SYNC | GPIO[22] (input/output) | VIO | I/O |
| **59** | GPIO[19]/PCM_IN | GPIO[19] (input/output) | VIO | I/O |
| **60** | GPIO[20]/PCM_OUT | GPIO[20] (input/output) | VIO | I/O |
| **61** | GPIO[21]/PCM_CLK | GPIO[21] (input/output) | VIO | I/O |
| **62** | GND | System Ground Pin | -- | -- |
| **63** | GPIO[14] | GPIO[14] (input/output) | VIO | I/O |
| **64** | GPIO[8]/WLAN_LED | LED_OUT_WLAN (output) | VIO | O |
| **65** | GPIO[9]/BT_LED | LED_OUT_BT (output) | VIO | O |
| **66** | NC | No Connect | -- | -- |
| **67** | NC | No Connect | -- | -- |
| **68** | GND | System Ground Pin | -- | -- |
| **69** | USB_DN | USB Serial Differential Data Negative | 3.3V | I/O |
| **70** | USB_DP | USB Serial Differential Data Positive | 3.3V | I/O |
| **71** | GND | System Ground Pin | -- | -- |
| **72** | 3V3_USB | 3.3V USB Power Supply | 3.3V | Power |
| **73** | VIO | Digital I/O Power Supply | 1.8V/2.5V/3.3V | Power |
| **74~96** | GND | System Ground Pin | -- | -- |
| **G1~G36** | GND | System Ground Pin | -- | -- |

**Notes:**

1. SDIO signals should have 50 ohm impedances.
2. For SDIO interface, 33ohm inline resistor may be needed to help with signal integrity.
3. For GPIO[8], it's internal pull up to VIO-RF(3.3V).
4. For GPIO[9], it's internal pull up to VIO-RF(3.3V).
5. For PDn pin, please pull up resistor(51k ohm) to host or VBAT(3V3).
6. For SDIO interface, the pull up value is between 10K to 100K ohm according to the SDIO v3.0 SPEC.
7. PCIE Impedance targets : Single-ended Z of 60 ohms +- 15%. Differential Impedance of ~100 ohm +- 20%.
8. USB Impedance targets : D+/D- are differential and should have 90ohms impedance.
9. For GPIO[3] pin, please pull up resistor(10k ohm) to VIO.

## Note: Interface supports and combinations as shown below:

| Scenario | WLAN | BT | BT_AMPS | Firmware Download I/F | Firmware Download Mode | Configuration* |
|---|---|---|---|---|---|---|
| **1** | SDIO | SDIO | -- | SDIO | Serial | CON[3:0]=b'0001 |
| **2** | SDIO | SDIO | SDIO | SDIO | Serial | CON[3:0]=b'0111 |
| **3** | PCIe | UART | -- | PCIe + UART | Parallel | CON[3:0]=b'1111 |
| **4** | PCIe | UART | -- | PCIe or UART | Serial | CON[3:0]=b'1100 |
| **5** | PCIe | USB | USB | PCIe | Serial | CON[3:0]=b'1110 |

***Configuration pins:**

| Configuration | Pin No | Pin Name |
|---|---|---|
| **CON[3]** | 13 | CONFIG_HOST[3] |
| **CON[2]** | 10 | CONFIG_HOST[2] |
| **CON[1]** | 9 | CONFIG_HOST[1] |
| **CON[0]** | 8 | CONFIG_HOST[0] |

# 3. Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **Pin73/ VIO** | Host I/O power supply | - | 1.8 | 2.2 | V |

| | | | | | |
|---|---|---|---|---|---|
| | | - | 2.5 | 3.0 | |
| | | - | 3.3 | 4.0 | |
| **Pin44/ VIO_SD** | SDIO power supply | - | 1.8 | 2.2 | V |
| | | - | 3.3 | 4.0 | |
| **Pin5/ 3.3V** | LDO VBAT input | - | 3.3 | 5.0 | V |
| **Pin72/ 3V3_USB** | LDO USB VBAT input | - | 3.3 | 4.0 | V |
| **Pin4/ 3.3V** | LDO RF VBAT input | - | 3.3 | 4.0 | V |

## 3.2 Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **Pin73/ VIO** | 1.8V/2.5V/3.3V digital I/O power supply | 1.62 | 1.8 | 1.98 | V |
| | | 2.25 | 2.5 | 2.75 | |
| | | 2.97 | 3.3 | 3.63 | |
| **Pin44/ VIO_SD** | 1.8V/3.3V digital I/O SDIO power supply | 1.62 | 1.8 | 1.98 | V |
| | | 2.97 | 3.3 | 3.63 | |
| **Pin5/ 3.3V** | LDO VBAT input | 2.7 | 3.3 | 5.0 | V |
| **Pin72/ 3V3_USB** | LDO USB VBAT input | 2.97 | 3.3 | 3.63 | V |
| **Pin4/ 3.3V** | LDO RF VBAT input | 2.97 | 3.3 | 3.63 | V |

### 3.2.1 The Interface Pins Power Supply

The SDIO host interface pins are powered from the chip VIO_SD (pin 44) 1.8V/3.3V voltage supply.

- SDIO Default Speed, High Speed Modes (3.3V)
- SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)
- SDR104 Mode (208MHz) (1.8V)

The PCI Express host interface pins are powered from the module's chip LDO 1.8V voltage supply internal.

The USB2.0 host interface pins are powered from the 3V3_USB (pin 72) 3.3V voltage supply.

The UART Tx and Rx pins are powered from the VIO (pin 73) voltage supply.

The GPIO pins are powered from the VIO (pin 73) voltage supply (GPIO [9:8] from 3.3V voltage internal).

The clocked serial pins are powered from the module's chip LDO 1.8V voltage supply internal.

The audio pins are powered from the chip VIO (pin 73) voltage supply.

## 3.3 Digital IO Pin DC Characteristics

### 3.3.1 Digital Pad Ratings-VIO

#### 3.3.1.1 1.8V Operation (VIO)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7*V18 | - | V18+0.4 | V |
| $V_{IL}$ | Input low voltage | -0.4 | - | 0.3*V18 | |
| $V_{OH}$ | Output high voltage | V18-0.4 | - | - | |
| $V_{OL}$ | Output low voltage | - | - | 0.4 | |

#### 3.3.1.2 2.5V Operation (VIO)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7*V25 | - | V25+0.4 | V |
| $V_{IL}$ | Input low voltage | -0.4 | - | 0.3*V25 | |
| $V_{OH}$ | Output high voltage | V25-0.4 | - | - | |
| $V_{OL}$ | Output low voltage | - | - | 0.4 | |

#### 3.3.1.3 3.3V Operation (VIO)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7*V33 | - | V33+0.4 | V |
| $V_{IL}$ | Input low voltage | -0.4 | - | 0.3*V33 | |
| $V_{OH}$ | Output High Voltage | V33-0.4 | - | - | |
| $V_{OL}$ | Output Low Voltage | - | - | 0.4 | |

### 3.3.2 Digital Pad Ratings-VIO_SD

#### 3.3.2.1 1.8V Operation (VIO_SD)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7*V18 | - | V18+0.4 | V |
| $V_{IL}$ | Input low voltage | -0.4 | - | 0.3*V18 | |
| $V_{OH}$ | Output high voltage | V18-0.4 | - | - | |
| $V_{OL}$ | Output low voltage | - | - | 0.4 | |

#### 3.3.2.2 3.3V Operation (VIO_SD)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7*V33 | - | V33+0.4 | V |
| $V_{IL}$ | Input low voltage | -0.4 | - | 0.3*V33 | |
| $V_{OH}$ | Output High Voltage | V33-0.4 | - | - | |
| $V_{OL}$ | Output Low Voltage | - | - | 0.4 | |

## 3.4 Host Interface

### 3.4.1 SDIO Interface

The AW-CM389NF supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless module device.

The AW-CM389NF acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

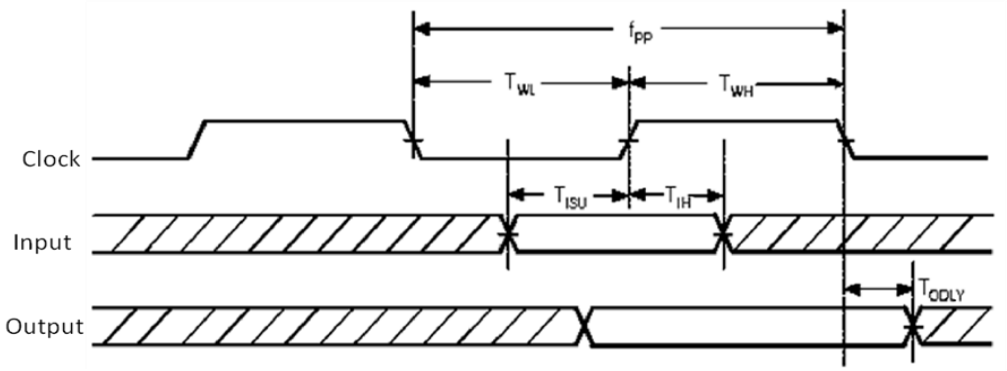
- Supports SDIO 3.0 Standard
- On-chip memory used for CIS
- Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes
- Special interrupt register for information exchange
- Allows card to interrupt host

**SDIO Interface Signals**

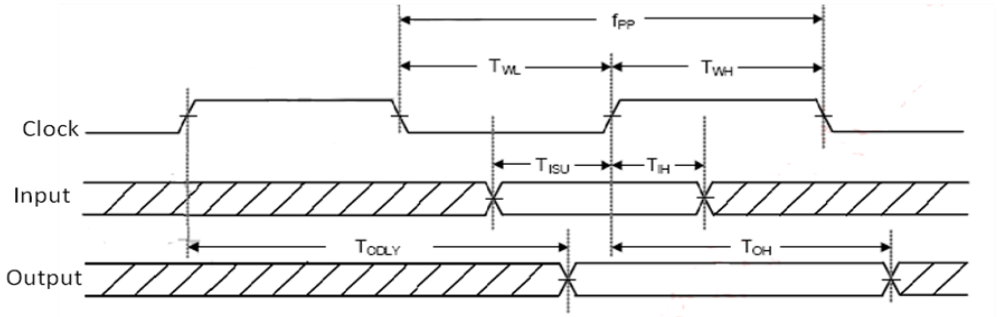
| AW-CM389NF SDIO Pin Name | Type | Description |
|---|---|---|
| **SDIO_CLK** | I/O | SDIO 4-bit mode: Clock<br>SDIO 1-bit mode: Clock |
| **SDIO_CMD** | I/O | SDIO 4-bit mode: Command line<br>SDIO 1-bit mode: Command line |
| **SDIO_DAT[3]** | I/O | SDIO 4-bit mode: Data line Bit[3]<br>SDIO 1-bit mode: Not used |
| **SDIO_DAT[2]** | I/O | SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional)<br>SDIO 1-bit mode: Read Wait (optional) |
| **SDIO_DAT[1]** | I/O | SDIO 4-bit mode: Data line Bit[1]<br>SDIO 1-bit mode: Interrupt |
| **SDIO_DAT[0]** | I/O | SDIO 4-bit mode: Data line Bit[0]<br>SDIO 1-bit mode: Data line |

### 3.4.2 SDIO Protocol Timing

#### 3.4.2.1 Default Speed, High-Speed Modes (3.3V)




SDIO protocol timing Diagram - Default Speed Mode. (3.3V)



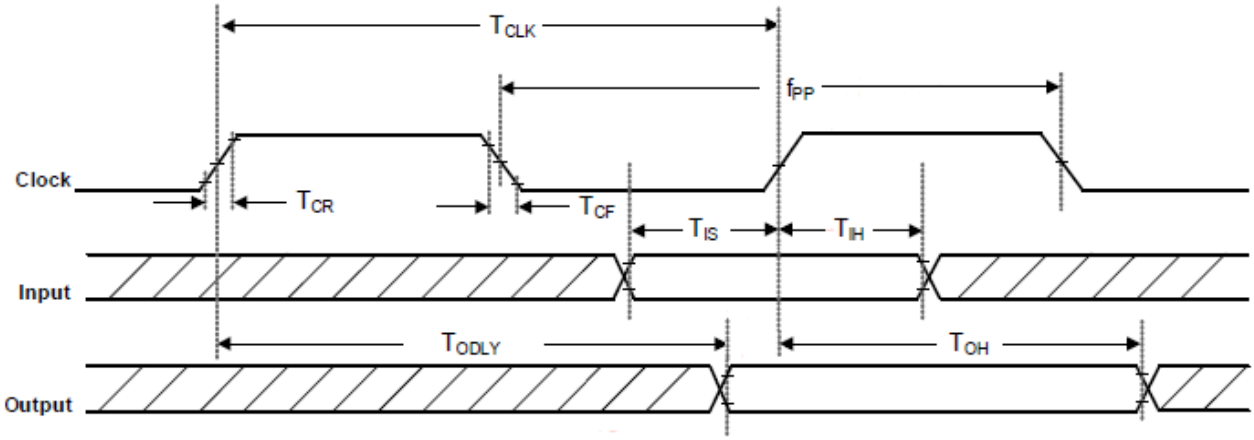

SDIO protocol timing Diagram - High Speed Mode. (3.3V)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{pp}$ | CLK Frequency | Normal | 0 | -- | 25 | MHz |
| | | High Speed | 0 | -- | 50 | MHz |
| $T_{WH}$ | CLK High Time | Normal | 10 | -- | -- | ns |
| | | High Speed | 7 | -- | -- | ns |
| $T_{WL}$ | CLK Low Time | Normal | 10 | -- | -- | ns |
| | | High Speed | 7 | -- | -- | ns |
| $T_{ISU}$ | Input Setup Time | Normal | 5 | -- | -- | ns |
| | | High Speed | 6 | -- | -- | ns |
| $T_{IH}$ | Input Hold Time | Normal | 5 | -- | -- | ns |
| | | High Speed | 2 | -- | -- | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| $T_{ODLY}$ | Output Delay Time | Normal | -- | -- | 14 | ns |
| | CL ≦ 40pF (1 card) | High Speed | -- | -- | 14 | ns |
| $T_{OH}$ | Output Hold Time | High Speed | 2.5 | -- | -- | ns |

SDIO Timing Data – Default Speed / High-Speed Modes. (3.3V)

### 3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

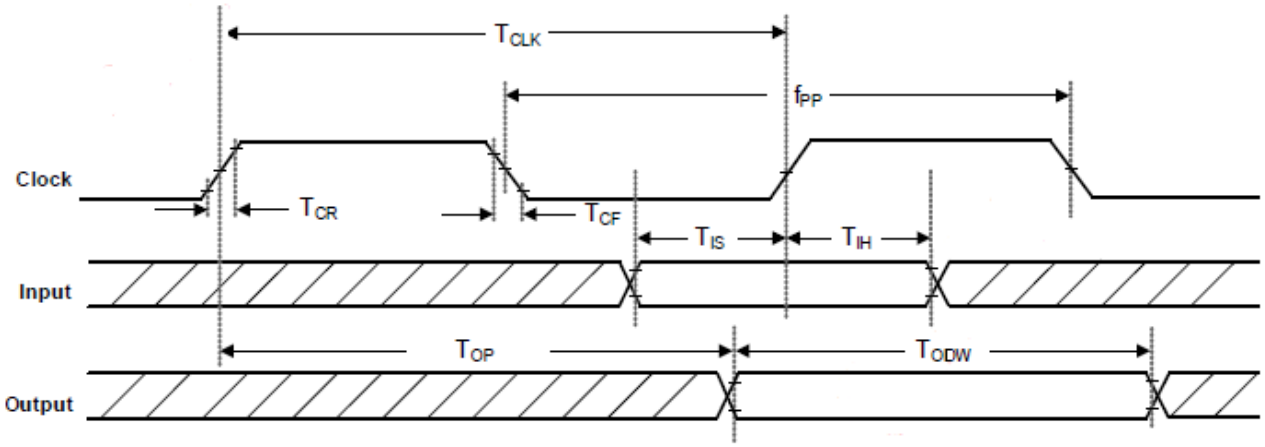



SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes. (up to 100 MHz)(1.8V)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{pp}$ | CLK Frequency | SDR12/25/50 | 25 | - | 100 | MHz |
| $T_{CLK}$ | Clock Time | SDR12/25/50 | 10 | - | 40 | ns |
| $T_{IS}$ | Input Setup Time | SDR12/25/50 | 3 | - | - | ns |
| $T_{IH}$ | Input Hold Time | SDR12/25/50 | 0.8 | - | - | ns |
| $T_{CR}$ ,$T_{CF}$ | Rise time, fail time<br>TCR ,TCF <2ns(max) at 100 MHz<br>CCARD =10pF | SDR12/25/50 | - | - | 0.2*$T_{CLK}$ | ns |
| $T_{ODLY}$ | Output Delay Time<br>CL ≦ 30pF | SDR12/25/50 | - | - | 7.5 | ns |
| $T_{OH}$ | Output Hold Time<br>CL =15pF | SDR12/25/50 | 1.5 | - | - | ns |

SDIO Timing Data - SDR12/25/50 Modes. (1.8V)

### 3.4.2.3 SDR104 Mode (208 MHz) (1.8V)




SDIO protocol timing Diagramed SDR104 Mode (208 MHz)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **fpp** | CLK Frequency | SDR104 | 0 | - | 208 | MHz |
| **TCLK** | Clock Time | SDR104 | 4.8 | - | - | ns |
| **TIS** | Input Setup Time | SDR104 | 1.4 | - | - | ns |
| **TIH** | Input Hold Time | SDR104 | 0.8 | - | - | ns |
| **TCR, TCF** | Rise time, fail time<br>$T_{CR}$ ,$T_{CF}$ <0.96ns(max) at 208 MHz<br>$C_{CARD}$ =10pF | SDR104 | - | - | 0.2 *$T_{CLK}$ | ns |
| **TOP** | Card output phase | SDR104 | 0 | - | 10 | ns |
| **TODW** | Output timing of variable data window | SDR104 | 2.88 | - | - | ns |

SDIO Timing Data - SDR104 Mode. (208 MHz)

### 3.4.3 PCI Express Interface

#### 3.4.3.1 Differential Tx Output Electricals

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **UI** | Unit interval<br>Each UI is 400 ps ±300 ppm.<br>UI does not account for SSC dictated variations. | 399.98 | 400 | 400.12 | ps |
| **$V_{Tx\_DIFFpp}$** | Different peak-to-peak output voltage<br>$V_{Tx\_DIFFpp}=2*\|V_{TX-D+} - V_{TX-D-}\|$ | 0.800 | -- | 1.2 | V |
| **$V_{Tx\_DE\_RATIO}$** | De-emphasized differential output voltage (ratio) | -3.0 | -3.5 | -4.0 | db |
| **$T_{Rx\_EYE}$** | Minimum Tx eye width | 0.75 | -- | -- | UI |
| **$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$** | Maximum time between jitter median and maximum deviation from median | -- | -- | 0.125 | UI |
| **$T_{Tx\_RISE}$, $T_{Tx\_FALL}$** | D+/D- Tx output rise/fall time | 0.125 | -- | -- | UI |
| **$V_{Tx\_CM\_DC\_ACTIVE\_IDLE\_DELTA}$** | Absolute delta of DC common mode voltage during L0 and electrical idle | 0 | -- | 100 | mV |
| **$V_{Tx\_CM\_DC\_LINE\_DELTA}$** | Absolute delta of DC common mode voltage between D+ and D- | 0 | -- | 25 | mV |
| **$V_{Tx\_IDLE\_DIFFp}$** | Electrical idle differential peak output voltage | 0 | -- | 20 | mV |
| **$V_{Tx\_RCV\_DETECT}$** | Voltage change allowed during receiver detection | -- | -- | 600 | mV |
| **$V_{Tx\_DC\_CM}$** | Tx DC common mode voltage | -- | -- | 3.6 | V |
| **$I_{Tx\_SHORT}$** | Tx short circuit current limit | -- | -- | 90 | mA |
| **$T_{Tx\_IDLE\_MIN}$** | Minimum time spent in electrical idle | 50 | -- | -- | UI |
| **$T_{Tx\_IDLE\_SET\_TO\_IDLE}$** | Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set | -- | -- | 20 | UI |
| **$T_{Tx\_IDLE\_TO\_DIFF\_DATA}$** | Maximum time to transition to valid Tx specifications after leaving an electrical idle condition | -- | -- | 20 | UI |
| **$RL_{Tx\_DIFF}$** | Differential return loss | 10 | -- | -- | dB |
| **$RL_{Tx\_CM}$** | Common mode return loss | 6 | -- | -- | dB |

| | | | | | |
|---|---|---|---|---|---|
| $C_{Tx}$ | AC coupling capacitor | 75 | -- | 200 | nF |
| $T_{Crosstalk}$ | Crosstalk random timeout | 0 | -- | 1 | ms |

### 3.4.3.2 Differential Rx Output Electricals

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **UI** | Unit interval<br>Each UI is 400 ps ±300 ppm.<br>UI does not account for SSC dictated variations. | 399.98 | 400 | 400.12 | ps |
| $V_{Rx\_DIFFpp}$ | Different peak-to-peak output voltage<br>$V_{Tx\_DIFFpp}=2*\|V_{TX-D+} - V_{TX-D-}\|$ | 0.175 | -- | 1.2 | V |
| $T_{Rx\_EYE}$ | Minimum Tx eye width | 0.4 | -- | -- | UI |
| $T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$ | Maximum time between jitter median and maximum deviation from median | -- | -- | 0.3 | UI |
| $V_{Rx\_CM\_ACp}$ | AC peak common mode input voltage | -- | -- | 150 | mV |
| $RL_{Rx\_DIFF}$ | Differential return loss | 10 | -- | -- | dB |
| $RL_{Rx\_CM}$ | Common mode return loss | 6 | -- | -- | dB |
| $Z_{Rx\_DIFF\_DC}$ | DC differential input impedance | 80 | 100 | 120 | Ω |
| $Z_{Rx\_DC}$ | DC input impedance | 40 | 50 | 60 | Ω |
| $Z_{Rx\_HIGH\_IMP\_DC\_POS}$ | Powered down DC input impedance positive | 50 | -- | -- | KΩ |
| $Z_{Rx\_HIGH\_IMP\_DC\_NEG}$ | Powered down DC input impedance negative | 1 | -- | -- | kΩ |
| $V_{Rx\_IDLE\_DET\_DIFFpp}$ | Electrical idle detect threshold | 65 | -- | 175 | mV |
| $T_{Rx\_IDLE\_DET\_DIFF\_ENTERTIME}$ | Unexpected electrical idle enter detect threshold integration time | -- | -- | 10 | ms |
| $L_{Rx\_SKEW}$ | Total skew | -- | -- | 20 | ns |

### 3.4.4 USB Interface

The USB device interface is compliant with the Universal Serial Bus Specification, Revision 2.0, April 27, 2000. A USB host uses the USB cable bus and the USB 2.0 device interface to communicate with the chip.

The main features of the USB device interface include:

- High/full speed operation (480/12 Mbps).
- Suspend/host resume/device resume (remote wake-up).
- Built-in DMA engine that reduces interrupt loads on the embedded processor and reduces the system bus bandwidth requirement for serving the USB device operation.
- The USB 2.0 device interface is designed with 3.3V signal level pads.

#### 3.4.4.1 USB 2.0 Device Interface Description

Table shows the signal mapping between the AW-CM389NF and the USB Specification, Revision 2.0.

| AW-CM389NF Pin Name | USB 2.0 Specification Pin Name | Description |
|---|---|---|
| **Pin72/ 3V3_USB** | VBUS | USB Bus Power Supply<br>On-board regulator regulates voltage from VBUS level to voltage levels used by USB PHY. |
| **--** | GND | USB Bus Ground<br>Common ground on SoC device. |
| **Pin70/ USB_DP** | D+ | USB Bus Data Positive<br>One of the different data pair. |
| **Pin69/ USB_DN** | D- | USB Bus Data Negative.<br>One of the different data pair. |

#### 3.4.4.2 USB 2.0 Device Functional Description

The device controller uses internal Scatter/Gather DMA engine to transfer the transmit packet from internal SRAM to USB and the receive packet from USB to internal SRAM. The Device IN Endpoint DMA (DIEPDMAn) and Device OUT Endpoint DMA (DOEPDMAn) registers are used by the DMA engine to access the base descriptor. The application is interrupted after the programmed transfer size extracted from the descriptors is transmitted or received. By using registers, interrupts, and special data structures, the device controller can communicate with the device controller driver (application/software) about bus states, host request, and data transfer status. The device controller

driver also has all of the routines to respond to the device framework commands issued by a USB host, so it controls the attachment, configuration, operation, and detachment of the device.

### 3.4.5 High-Speed UART Interface

The AW-CM389NF supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data. Table shows the rates supported.

The UART interface features include:

- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit and receive operations
- Two flow control pins

Interrupt triggers for low-power, high throughput operation.

- The UART interface operation includes:
- Upload boot code to the internal CPU (for debug purposes)
- Support diagnostic tests
- Support data input/output operations for peripheral devices connected through a standard UART interface

Tables shows UART Baud Rates supported.

| Baud Rate | | | | |
|---|---|---|---|---|
| **1200** | 38400 | 460800 | 1500000 | 3000000 |
| **2400** | 57600 | 500000 | 1843200 | 3250000 |
| **4800** | 76800 | 921600 | 2000000 | 3692300 |
| **9600** | 115200 | 1000000 | 2100000 | 4000000 |
| **19200** | 230400 | 1382400 | 2764800 | |

### 3.4.5.1 UART Interface Signal Description

Table shows the standard UART signal names on the device.

| Signal Name | 16550 Standard Pin Name | Description |
|---|---|---|
| **Data Bus** | | |
| **UART_SIN** | SIN | Serial data input from modem, data set, or peripheral device |
| **UART_SOUT** | SOUT | Serial data output from modem, data set, or peripheral device |
| **Modem Control** | | |
| **UART_RTSN** | RTS | Request To Send output to modem, data set, or peripheral device (active low) |
| **UART_CTSN** | CTS | Clear To Send input from modem, data set, or peripheral device (active low) |

### 3.4.5.2 UART Interface Functional Description

#### 3.4.5.2.1 Booting from UART

When booting from the UART, the AW-CM389NF device has the following requirements:

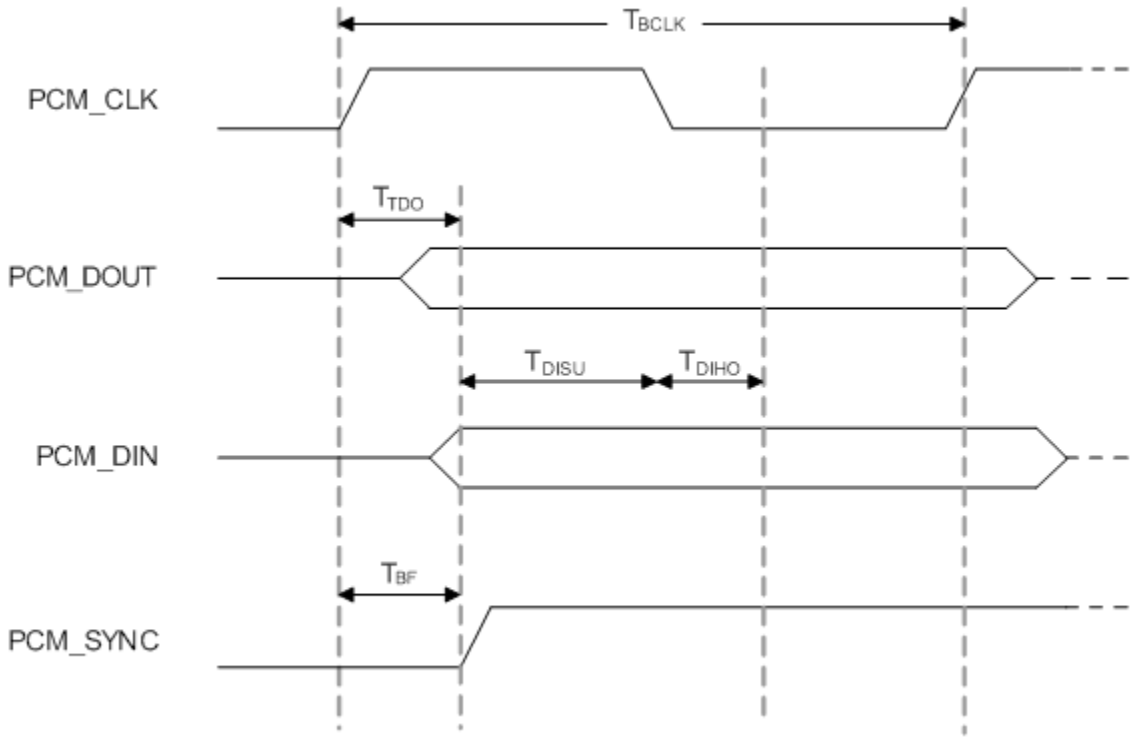
| System Requirement | Description |
|---|---|
| **Number of data bits** | 8 bits |
| **Stop bits** | 1 bit |
| **Parity** | No parity |
| **Baud Rate** | 115200 |

#### 3.4.5.2.2 UART as Test Port

Test diagnostic programs may be uploaded to the CPU through the UART interface. During execution, the diagnostic program transmits performance and status information through the UART by performing a write to the PBU address space designated to the UART.

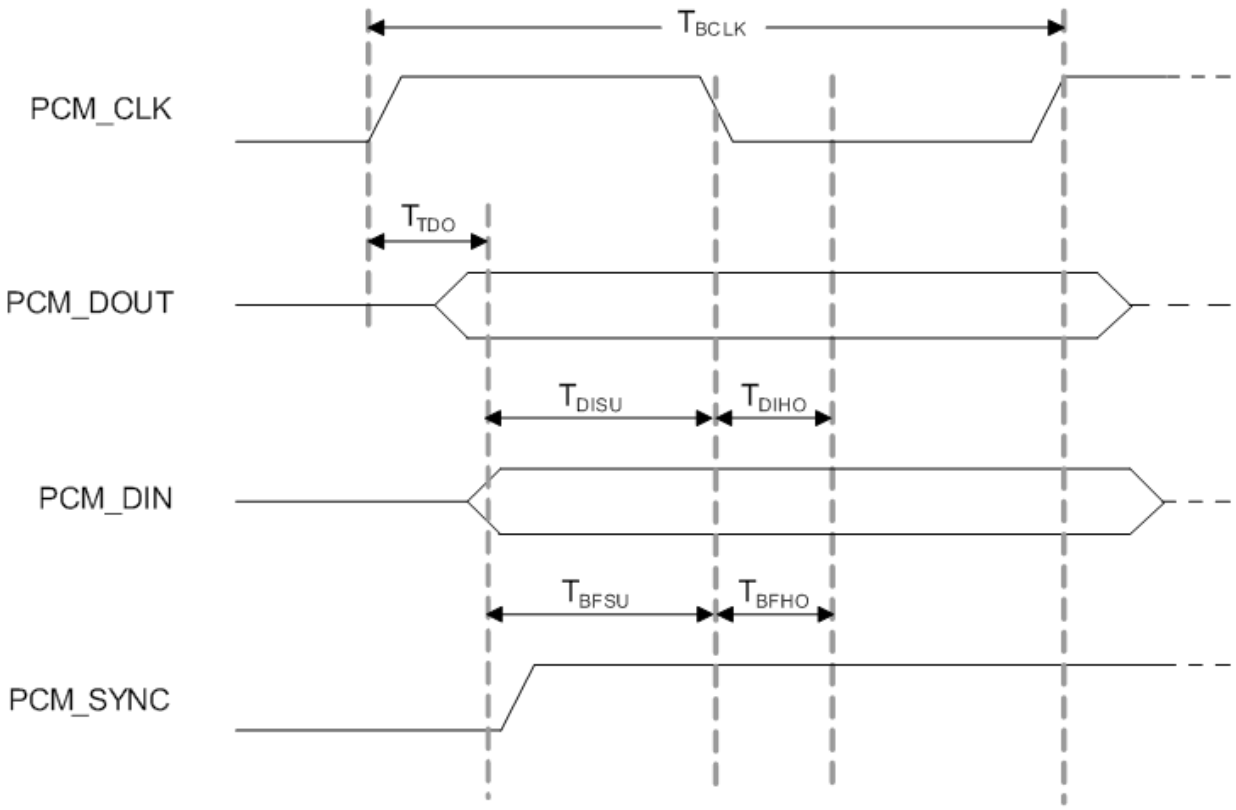
## 3.4.6 PCM Interface

### 3.4.3.1 PCM Timing Specification – Master Mode




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **$F_{BCLK}$** | -- | -- | -- | 2/2.048 | -- | MHz |
| **Duty $Cycle_{BCLK}$** | -- | -- | 0.4 | 0.5 | 0.6 | -- |
| **$T_{BCLK\ rise/fall}$** | -- | -- | -- | 3 | -- | ns |
| **$T_{DO}$** | -- | -- | -- | -- | 15 | ns |
| **$T_{DISU}$** | -- | -- | 20 | -- | -- | ns |
| **$T_{DIHO}$** | -- | -- | 15 | -- | -- | ns |
| **$T_{BF}$** | -- | -- | -- | -- | 15 | ns |

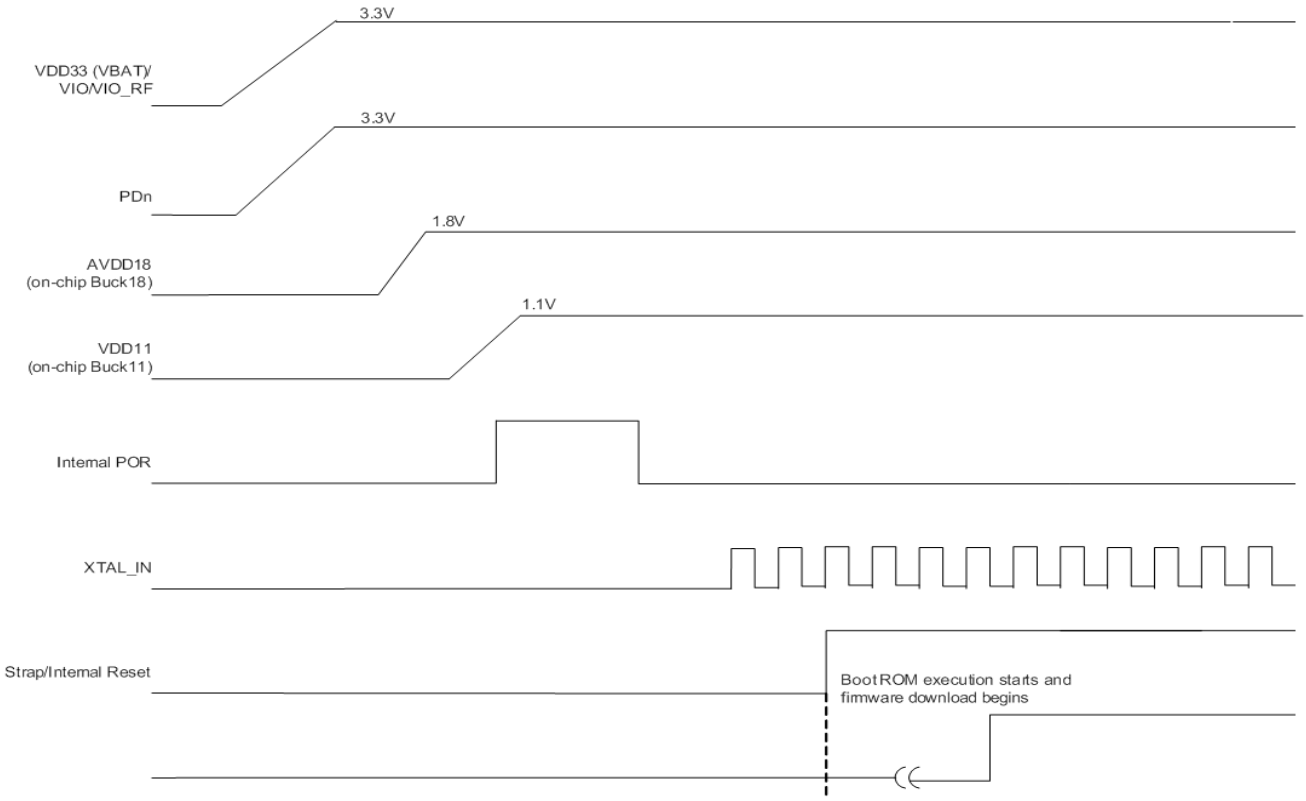
### 3.4.3.2 PCM Timing Specification – Slave Mode




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **$F_{BCLK}$** | -- | -- | -- | 2/2.048 | -- | MHz |
| **Duty $Cycle_{BCLK}$** | -- | -- | 0.4 | 0.5 | 0.6 | -- |
| **$T_{BCLK\ rise/fall}$** | -- | -- | -- | 3 | -- | ns |
| **$T_{DO}$** | -- | -- | -- | -- | 30 | ns |
| **$T_{DISU}$** | -- | -- | 15 | -- | -- | ns |
| **$T_{DIHO}$** | -- | -- | 10 | -- | -- | ns |
| **$T_{BFSU}$** | -- | -- | 15 | -- | -- | ns |
| **$T_{BFHO}$** | | | 10 | | -- | ns |

## 3.5 Timing Sequence

### AW-CM389NF power up timing sequence.



## 3.6 Power Consumption*

### 3.6.1 WLAN

| | Item | | | VBAT=3.3V | | | | |
|---|---|---|---|---|---|---|---|---|
| Band (GHz) | Mode | BW (MHz) | RF Power (dBm) | Transmit | | | Receive | |
| | | | | Max. (mA) | Avg. (mA) | Duty (%) | Max. (mA) | Avg. (mA) |
| 2.4G | 11b@1Mbps | 20 | 16 | 318 | 174 | 50.0 | 103 | 77 |
| | 11g@54Mbps | 20 | 14 | 292 | 102 | 21.0 | N/A | N/A |
| | 11n@MCS7 | 20 | 13 | 283 | 74 | 4.6 | 106 | 79 |
| | 11n@MCS15 | 20 | 13 | 494 | 91 | 2.7 | N/A | N/A |
| | 11n@MCS15 | 40 | 11 | 500 | 100 | 1.7 | 106 | 86 |
| 5G | 11a@54Mbps | 20 | 13 | 359 | 129 | 20.8 | 125 | 100 |
| | 11n@MCS15 | 20 | 12 | 611 | 132 | 2.7 | N/A | N/A |
| | 11n@MCS15 | 40 | 10 | 586 | 129 | 1.7 | N/A | N/A |
| | 11ac@MCS9 NSS1 | 80 | 8 | 419 | 121 | 1.5 | 179 | 129 |
| | 11ac@MCS9 NSS2 | 80 | 8 | 785 | 178 | 1.4 | 250 | 188 |

* The power consumption is based on Azurewave test environment, these data for reference only.

### 3.6.2 Bluetooth

| No. | Mode | VBAT=3.3V | | | |
|---|---|---|---|---|---|
| | | Transmit | | Receive | |
| | | Max. (mA) | Avg. (mA) | Max. (mA) | Avg. (mA) |
| 1 | DH5 | 43.8 | 42.8 | N/A | N/A |
| 2 | 3DH5 | N/A | N/A | 20.2 | 20.1 |

* The power consumption is based on Azurewave test environment, these data for reference only.

## 3.7 External Sleep Clock Timing

**External Sleep Clock is necessary for two reasons:**

1. Auto frequency Detection.

   This is where the internal logic will bin the Ref clock source to figure out what is the reference clock frequency is. This is done so no strapping is needed for telling 8897 what the ref clock input is.

2. Allow low current modes for BT to enter sleep modes such as sniff modes.

   The AW-CM389NF external sleep clock pin is powered from the 3.3V voltage supply.

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **CLK** | Clock Frequency Range | 32 or 32.768 -50ppm | 32 or 32.768 | 32 or 32.768 +50ppm | KHz |
| **$T_{HIGH}$** | Clock high time | 40 | -- | -- | ns |
| **$T_{LOW}$** | Clock low time | 40 | -- | -- | ns |
| **$T_{RISE}$** | Clock rise time | -- | -- | 5 | ns |
| **$T_{FALL}$** | Clock fall time | -- | -- | 5 | ns |

## 3.8 Reset Configuration

The AW-CM389NF is reset to its default operating state under the following conditions:

- Power-on reset (POR)
- Software/Firmware reset
- External pin reset (RESETn)

### 3.8.1 Internal Reset

The AW-CM389NF device is reset, and the internal CPU begins the boot sequence when any of the following internal reset events occur:

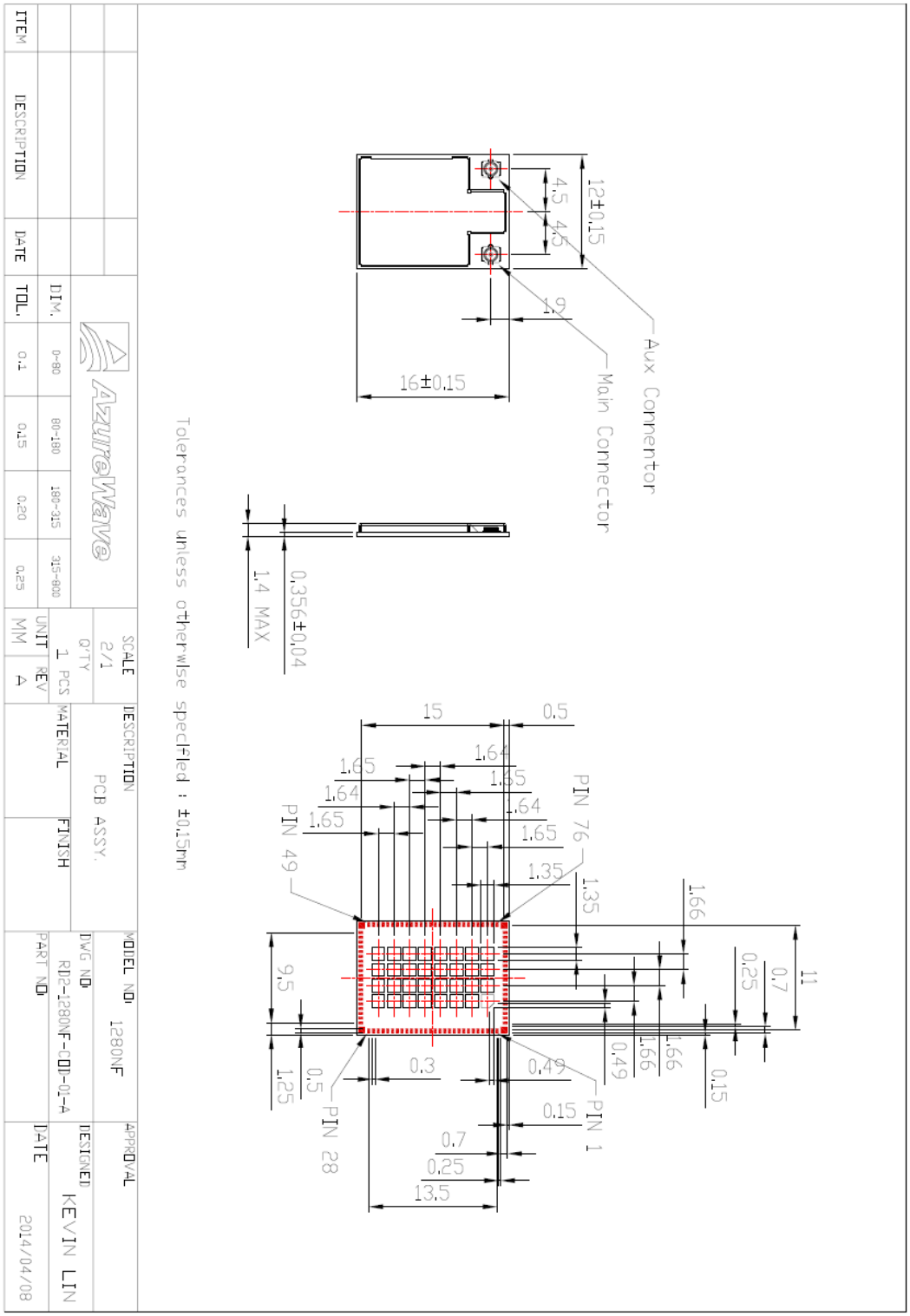
- Device receives power and VDDL supplies rise (triggers internal POR circuit)
- External pin (PDn) assertion will generate POR

### 3.8.2 External Reset

The AW-CM389NF is reset when PDn pin is asserted low and the internal CPU begins the boot sequence when the PDn pin transitions from low to high.

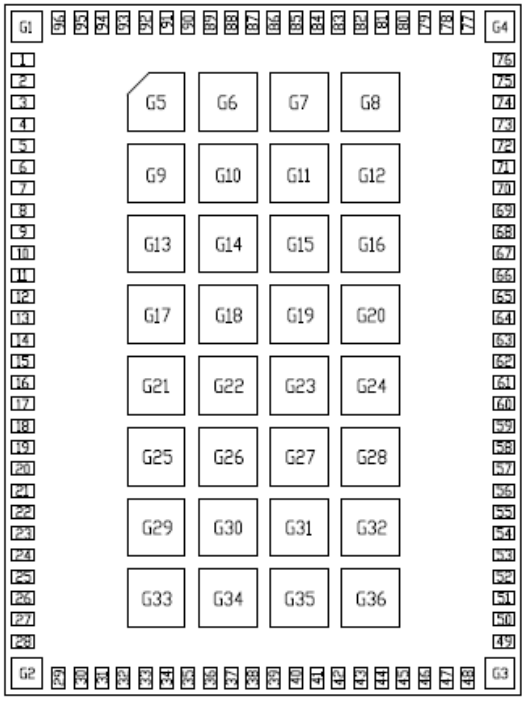
# 4. Mechanical Information

## 4.1 Mechanical Drawing

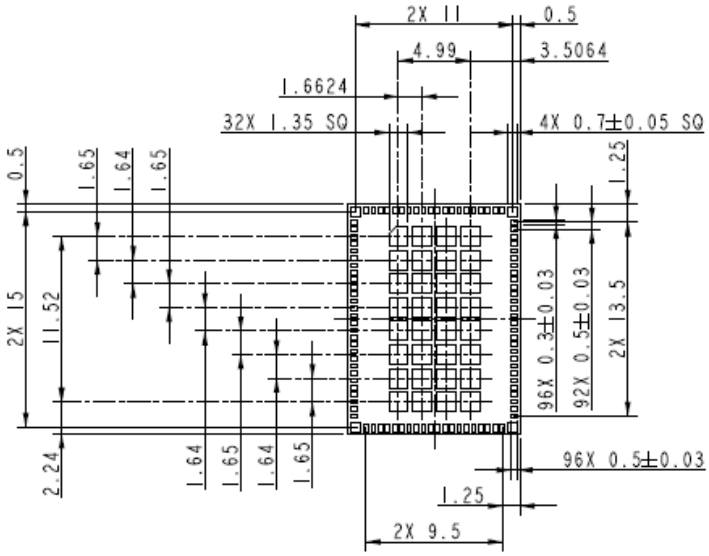


## 4.2 Module Footprint

AW-CM389NF PCB Layout Footprint



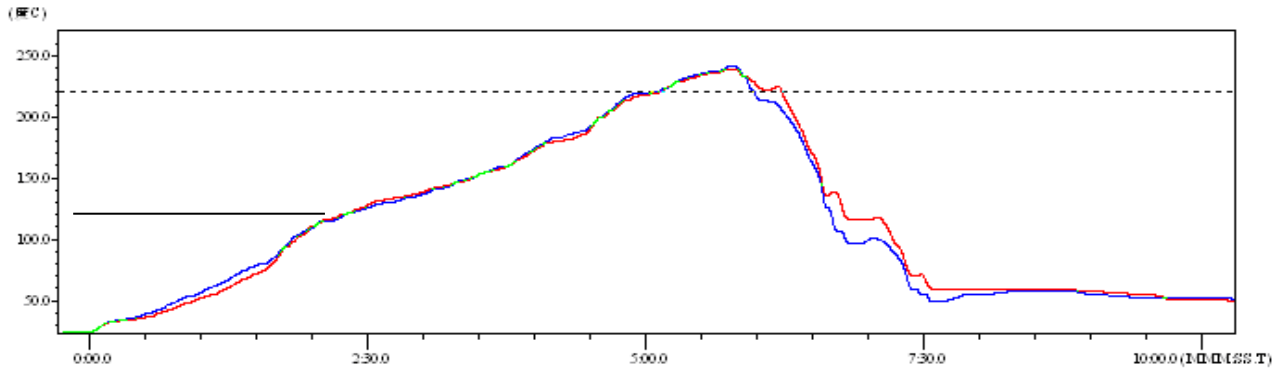

TOP VIEW



# 5. Packaging Information

## 5.1 Recommended Reflow Profile

**Reflow Soldering Profile**



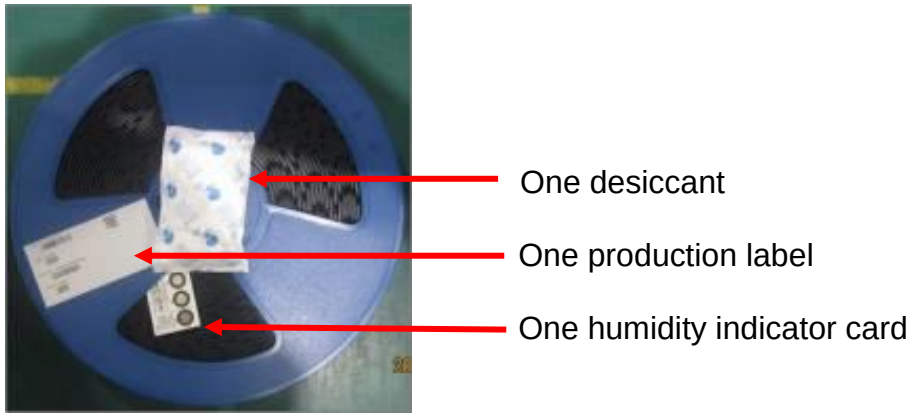

| No | Item | Temperature(°C) | Time(sec) |
|---|---|---|---|
| 1 | Reflow Time | Time of above 220 °C | 35~55sec |
| 2 | Peak-Temp | 260 °C max | |

**Note:**

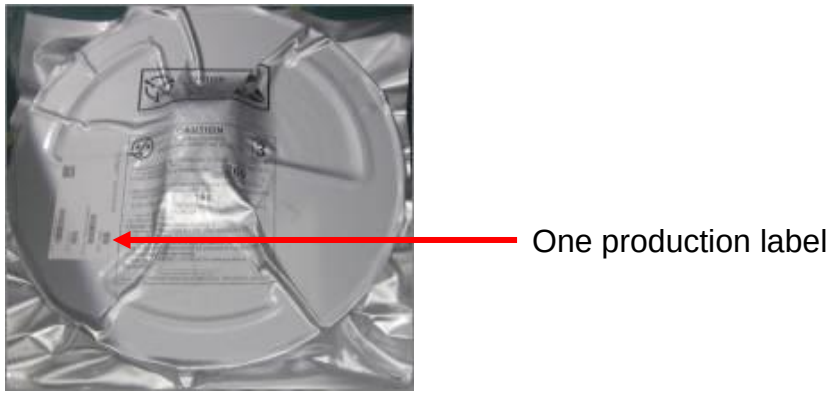
1. **Recommend to supply $N_2$ for reflow oven**
2. **$N_2$ atmosphere during reflow ($O_2$<300ppm)**

## 5.2 Shipping Information

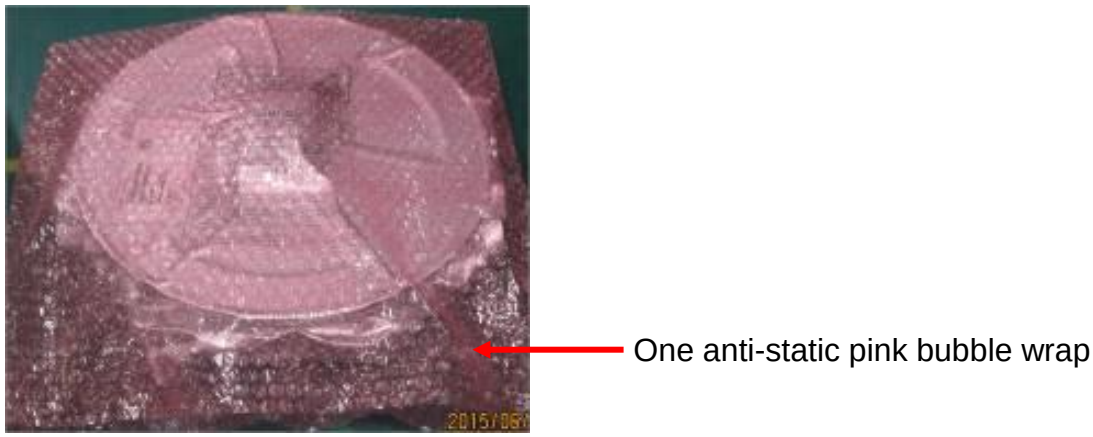
1. One reel can pack 1,500pcs M.2 1216 modules
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel




3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag




4. A bag is put into the anti-static pink bubble wrap



5. A bubble wrap is put into the inner box and then one label is pasted on the inner box


One production label

6. **5 inner boxes** could be put into one carton


7. Sealing the carton by AzureWave tape

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label will be pasted on the carton


| | |
|---|---|
| **Example of carton label** | AzureWave Technologies Inc.<br>AzureWave P/N<br>Customer: 由業務提供<br>Customer P/N: 由業務提供<br>Customer PO: 由業務提供<br>Description: AW-XXXXXX<br>QTY: 1200 pcs<br>C/N<br>N.W. G.W.<br>RoHS COMPLIANT |
| **Example of box label** | BOX0012018 |
| **Example of production label** | P/N:<br>D/C: 1309<br>PCK NO.: PCKNO0069097<br>QTY: 294<br>BAG SEAL DATE: _____ |
| **Example of balance label** | 尾 数<br>Balance |