# AW-CH397

## IEEE 802.11 2X2 MIMO ac/a/b/g/n Wireless LAN + Bluetooth SIP Module



## Datasheet

**Version 0.7**

| Document release | Date | Modification | Initials | Approved |
|---|---|---|---|---|
| Version0.1 | 2013/11/11 | Initial version | Kai Wu | Chihhao Liao |
| Version0.2 | 2014/01/20 | Add pin define & outline drawing | Peter Chen | Chihhao Liao |
| Version0.3 | 2014/03/17 | Modify module height | Peter Chen | Chihhao Liao |
| Version0.4 | 2014/04/07 | Modify Mechanical Information<br>Modify Package Outline Drawing<br>Modify Recommended Operating Conditions of Vio/Vio_SD/Vio_RF | Peter Chen | Chihhao Liao |
| Version0.5 | 2014/10/20 | Add WiFi Tx power & Sensitivity | Peter Chen | Chihhao Liao |
| Version0.6 | 2015/10/21 | support to BT4.2 | Peter Chen | Chihhao Liao |
| Version0.7 | 2018/08/20 | 1. Update Operating Temperature<br>2. Remove NFC function<br>3. Update support interface configuration | Peter Chen | NC Chen |

# 1. General Description

## 1-1. Product Overview and Functional Description

**AzureWave Technologies, Inc.** introduces the IEEE 802.11ac/a/b/g/n 2X2 MIMO WLAN & Bluetooth SIP module --- **AW-CH397**. The module is targeted to mobile devices including **Notebook, TV, Tablet and Gaming Device** which need small package module, low power consumption, multiple interfaces and OS support. By using AW-CH397, the customers can easily enable the Wi-Fi, and BT embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11ac/a/b/g/n standard, the AW-CH397 uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CH397. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, the AW-CH397 also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP)**, Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms.

For the video, voice and multimedia applications the AW-CH397 support **802.11e Quality of Service** (**QoS).** The device also supports **802.11h Dynamic Frequency Selection (DFS)** for detecting radar pulses when operating in the 5GHz range.

For Bluetooth operation, AW-CH397 is **Bluetooth 4.2 (supports Low Energy).**

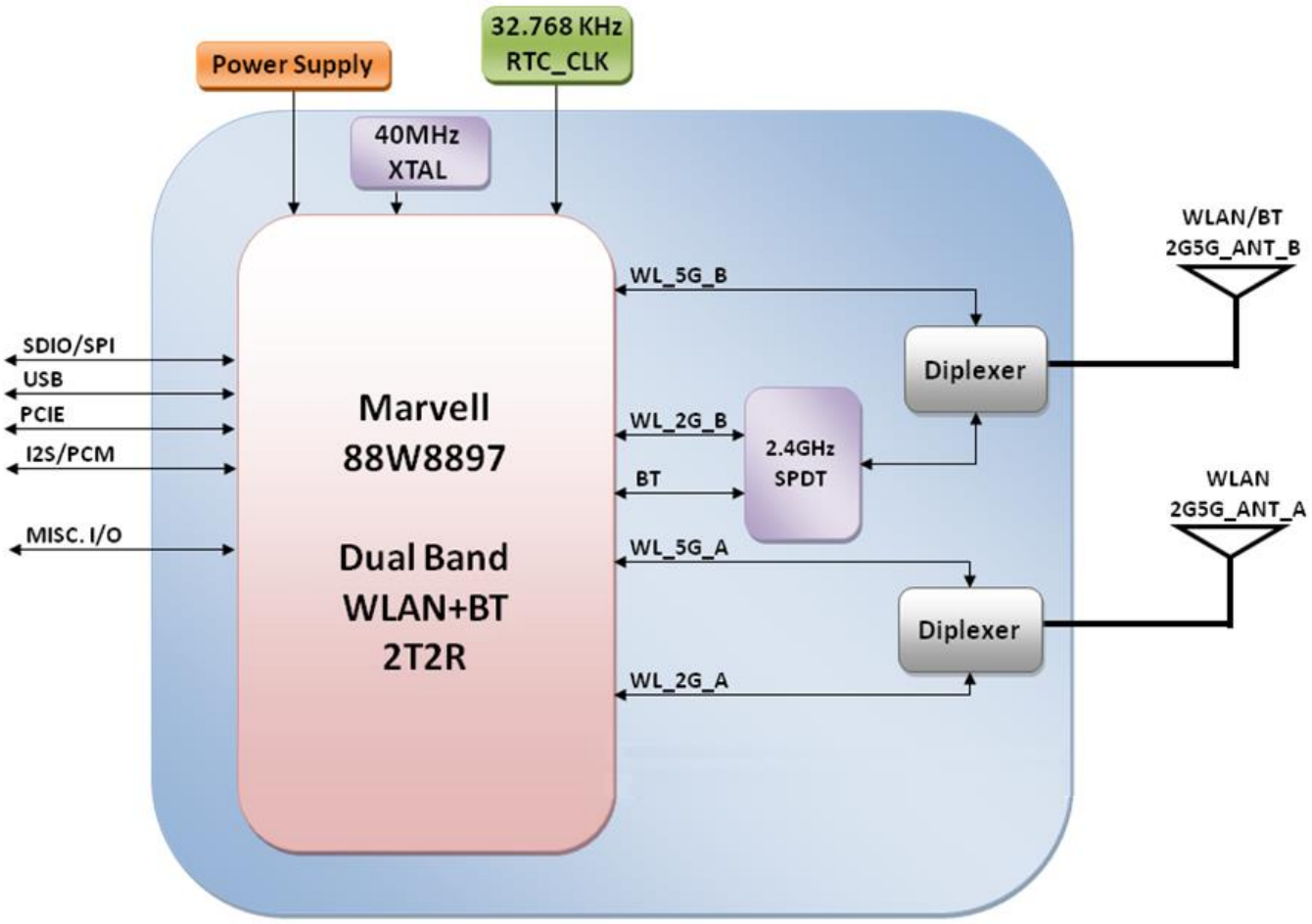
AW-CH397 supports **SDIO, PCIE, USB,** and high speed **UART interfaces** for WLAN and Bluetooth to the host processor.

AW-CH397 is suitable for multiple mobile processors for different applications with the support **cellular phone co-existence including LTE**.

AW-CH397 module adopts Marvell's latest highly-integrated dual-band WLAN & Bluetooth SoC---**88W8897**. All the other components are implemented by all means to reach the mechanical specification required.

## 1-2. Block Diagram

A simplified block diagram of the AW-CH397 module is depicted in the figure below.




AW-CH397 BLOCK DIAGRAM

## Note: Interface supports and combinations as shown below:

| Scenario | WLAN | BT | BT_AMPS | Firmware Download I/F | Firmware Download Mode | Configuration* |
|---|---|---|---|---|---|---|
| 1 | SDIO | SDIO | -- | SDIO | Serial | CON[3:0]=b'0001 |
| 2 | SDIO | SDIO | SDIO | SDIO | Serial | CON[3:0]=b'0111 |
| 3 | PCIe | UART | -- | PCIe + UART | Parallel | CON[3:0]=b'1111 |
| 4 | PCIe | UART | -- | PCIe or UART | Serial | CON[3:0]=b'1100 |
| 5 | PCIe | USB | USB | PCIe | Serial | CON[3:0]=b'1110 |

***Configuration pins:**

| Configuration | Pin No | Pin Name |
|---|---|---|
| CON[3] | K8 | CONFIG_HOST[3] |
| CON[2] | K7 | CONFIG_HOST[2] |
| CON[1] | K5 | CONFIG_HOST[1] |
| CON[0] | K6 | CONFIG_HOST[0] |

## 1-3.Key feature:

- **Small footprint: 10.0mm(L) x 12.3mm(W) x 1.0mm(H)Max**
- **SDIO3.0, G-SPI, USB interfaces support for WLAN**
- **High speed UART,PCM/Inter-IC Sound(I2S) and SDIO3.0, USB for Bluetooth**
- **Bluetooth 4.2 also complaint with Bluetooth 2.1 + Enhanced Data Rate (EDR)**
- **Audio Codec interface support**
- **Cellular phone co-existence support**
- **Multiple power saving modes for low power consumption**
- **IEEE 802.11i for advanced security**
- **Quality of Service (QoS) support for multimedia applications**
- **Drip-in WLAN Linux drivers are Android ready and validated on Android based systems.**
- **Support for Linux kernel versions up to 2.6.32.**
- **Support for BlueZ v4.47 Bluetooth profiles stack used in Android Éclair**
- **Simultaneous AP-STA**
- **Support China WAPI**
- **Lead-free design**

## 1-4. Specifications Table

| Model Name | AW-CH397 |
|---|---|
| **Product Description** | **2x2 MIMO Wireless LAN + Bluetooth Combo Module** |
| WLAN Standard | IEEE 802.11ac/a/b/g/n, Wi-Fi compliant |
| Bluetooth Standard | Bluetooth 4.2 complaint with Bluetooth 2.1+Enhanced Data Rate (EDR) |
| Host Interface | ◆ SDIO 3.0 device interface (SPI, 1-bit SDIO, 4-bit SDIO transfer modes at full clock range up to 208 MHz)<br>◆ PCIe v3.0 (2.5 Gbps) interface<br>◆ USB 2.0 interface with LPM support<br>◆ High-Speed UART interface |
| Major Chipset | Marvell 88W8897 |
| Dimension | 10.0mm x 12.3mm x 1.0mm(Max) |
| Weight | 0.34g |
| Package | LGA |
| **Operating Conditions** | |
| Voltage | 3.3V+- 10% |
| Temperature | Operating: -30 ~ +85 °C ; Storage: -40 ~ 85°C |
| **Electrical Specifications** | |
| Frequency Range | 2.4 GHz ISM radio band / 5 GHz Unlicensed National Information Infrastructure (U-NII) band |
| Number of Channels | 802.11a: USA, Taiwan – 12/4<br>Most European Countries –19<br>Japan – 4<br>802.11b: USA, Canada and Taiwan – 11<br>Most European Countries – 13<br>France – 4<br>802.11g: USA, Canada and Taiwan – 11<br>Most European Countries – 13<br>Japan – 13<br>802.11n(HT20): Channel 1~13(2412~2472)<br>802.11n(HT40): Channel 1~7(2422~2472) |
| Modulation | DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM for WLAN<br>GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps) for Bluetooth |
| Output Power | WLAN G band:<br>11b:15dBm +/- 2dBm(11M)<br>11g:13dBm +/- 2dBm (54M)<br>11n:HT20 12dBm +/- 2dBm(MCS7)<br>HT40 11dBm +/- 2dBm(MCS7)<br>WLAN A band:<br>11a:13dBm +/- 2dBm(54M)<br>11n HT20:12dBm +/- 2dBm(MCS7)<br>11n HT40:11dBm +/- 2dBm(MCS7)<br>11ac VHT_20:11dBm +/- 2dBm(MCS8)<br>11ac VHT_40:10dBm +/- 2dBm(MCS9)<br>11ac VHT_80: 8dBm +/- 2dBm(MCS9)<br><br>Bluetooth:<br>Class 2 |

| | |
|---|---|
| | |
| **Receive Sensitivity** | **WLAN G band :**<br>**11b:-86dBm (11M)**<br>**11g:-71dBm (54M)**<br>**11n:HT20 -70dBm (MCS7)**<br>**HT40 -68dBm (MCS7)**<br>**WLAN A band:**<br>**11a: -71dBm (54M)**<br>**11n HT20 -70dBm (MCS7)**<br>**11n HT40 -68dBm(MCS7)**<br>**11ac VHT_20: -66dBm(MCS8)**<br>**11ac VHT_40: -64dBm(MCS9)**<br>**11ac VHT_80: -58dBm(MCS9)**<br><br>**Bluetooth:**<br>**TBD** |
| **Medium Access Protocol** | **CSMA/CA with ACK** |
| **Data Rates** | **WLAN**<br>**802.11b: 1, 2, 5.5, 11Mbps**<br>**802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps**<br>**802.11n: up to 150Mbps-single**<br>**802.11n: up to 300Mbps-2x2 MIMO**<br>**802.11ac:up to 192.6Mbps (20MHz channel)**<br>**802.11ac:up to 400Mbps (40MHz channel)**<br>**802.11ac:up to 866.7Mbps (80MHz channel)**<br>**Bluetooth**<br>**Bluetooth 2.1+EDR data rates of 1,2, and 3Mbps** |
| **Power Consumption** | **Please refer to Power Consumption report.** |
| **Operating Range** | **Open Space: ~300m ; Indoor: ~100m for WLAN**<br>**Minimum 10 m indoor for Bluetooth**<br>**The transmission speed may vary according to the environment)** |
| **Security** | ◆ **WAPI**<br>◆ **WEP 64-bit and 128-bit encryption with H/W TKIP processing**<br>◆ **WPA/WPA2 (Wi-Fi Protected Access)**<br>◆ **AES-CCMP hardware implementation as part of 802.11i security standard** |
| **Operating System Compatibility** | **Linux, More information please contact Azurewave FAE.** |
| **Co-Existence** | **Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence** |

# 2. Electrical Characteristic

## 2-1.Absolute Maximum Ratings

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VBAT_IN | LDO VBAT input | -- | -- | 3.3 | 5.0 | V |
| 3V3_USB_IN | LDO USB 3.33V input | -- | -- | 3.3 | 4.0 | V |
| 3V3_RF_IN | LDO RF 3.3V input | -- | -- | 3.3 | 4.0 | V |
| 3V3_IN | LDO 3.3V input | -- | -- | 3.3 | 4.0 | V |
| VBUCK11_OUT | Internal power supply | -- | -- | 1.1 | 1.26 | V |
| VBUCK18_OUT | Internal power supply | -- | -- | 1.8 | 2.2 | V |
| VIO | Host I/O power supply | -- | -- | 3.3 | 4.0 | V |
| | | | | 2.5 | 3.0 | |
| | | | | 1.8 | 2.2 | |
| VIO_SD | SDIO power supply | -- | -- | 3.3 | 4.0 | V |
| | | | | 1.8 | 2.2 | |
| VIO_RF | RF I/O power supply | -- | -- | 3.3 | 4.0 | V |
| | | | | 1.8 | 2.2 | |

## 2-2.Recommanded Operating Conditions

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VBUCK11_OUT | Internal power supply | -- | -- | 1.1 | 1.21 | V |
| VBUCK18_OUT | Internal power supply | -- | 1.62 | 1.8 | 1.98 | V |
| VIO | 1.8V/2.5V/3.3V digital I/O power supply | -- | 2.97 | 3.3 | 3.63 | V |
| | | | 2.25 | 2.5 | 2.75 | |
| | | | 1.62 | 1.8 | 1.98 | |
| VIO_SD | 1.8V/3.3V digital I/O SDIO power supply | -- | 2.97 | 3.3 | 3.63 | V |
| | | | 1.62 | 1.8 | 1.98 | |
| VIO_RF | 1.8V/3.3V I/O power supply | -- | 2.97 | 3.3 | 3.63 | V |
| | | | 1.62 | 1.8 | 1.98 | |
| AVDD33 | 3.3V Analog power supply | -- | 2.97 | 3.3 | 3.63 | V |
| VBAT_IN | LDO VBAT input | -- | 2.7 | 3.3 | 5.0 | V |
| 3V3_USB_IN | LDO USB 3.3V input | | 2.97 | 3.3 | 3.63 | V |
| 3V3_RF_IN | LDO RF 3.3V input | | 2.97 | 3.3 | 3.63 | V |
| 3V3_IN | LDO 3.3V input | | 2.97 | 3.3 | 3.63 | V |

# 2-3.Clock Specifications

## 2-3-1 External Sleep Clock Timing

**External Sleep Clock is necessary for two reasons:**

1. Auto frequency Detection.
   This is where the internal logic will bin the Ref clock source to figure out what is the reference clock frequency is. This is done so no strapping is needed for telling 8897 what the ref clock input is.
2. Allow low current modes for BT to enter sleep modes such as sniff modes.
   The AW-CH397 external sleep clock pin is powered from the 3.3V voltage supply.

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| CLK | Clock Frequency Range | 32 or 32.768 -50ppm | 32 or 32.768 | 32 or 32.768 +50ppm | KHz |
| $T_{HIGH}$ | Clock high time | 40 | -- | -- | ns |
| $T_{LOW}$ | Clock low time | 40 | -- | -- | ns |
| $T_{RISE}$ | Clock rise time | -- | -- | 5 | ns |
| $T_{FALL}$ | Clock fall time | -- | -- | 5 | ns |

# 2-4. Reset Configuration

The AW-CH397 is reset to its default operating state under the following conditions:

- Power-on reset (POR)
- Software/Firmware reset
- External pin reset (RESETn)

## 2-4-1. Internal Reset

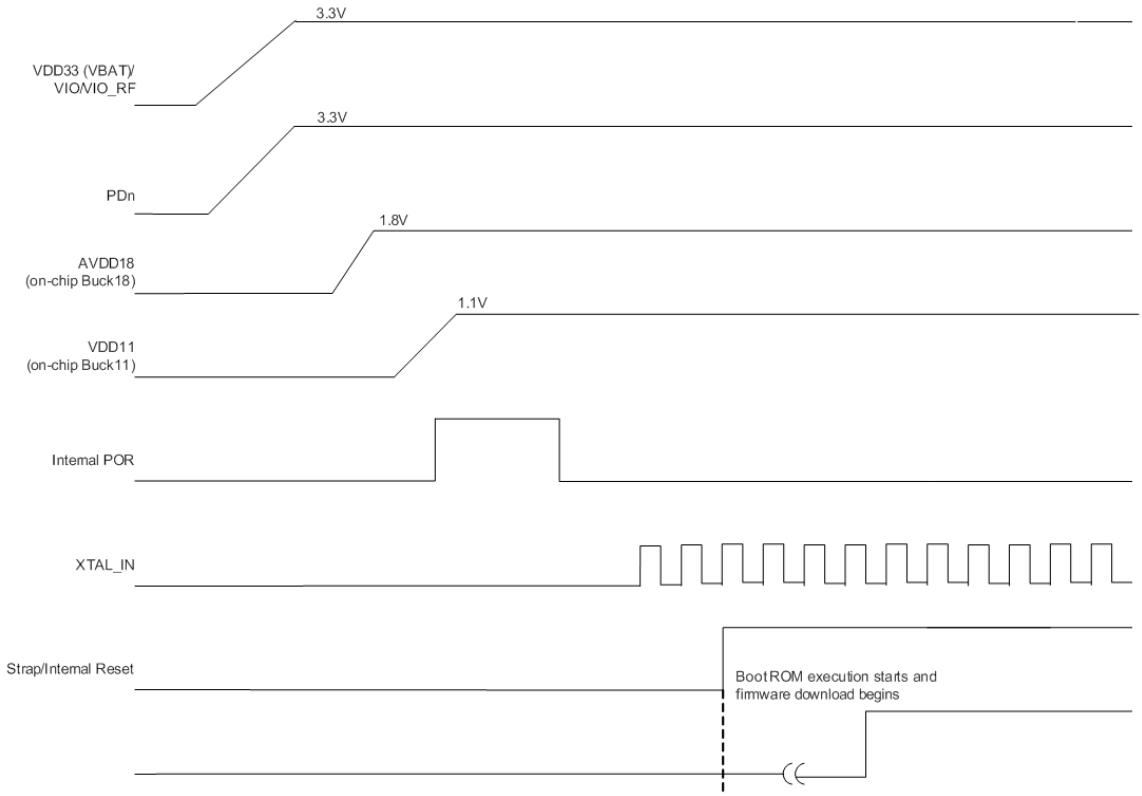
The AW-CH397 device is reset, and the internal CPU begins the boot sequence when any of the following internal reset events occur:

- Device receives power and VDDL supplies rise (triggers internal POR circuit)
- External pin (PDn) assertion will generate POR

## 2-4-2. External Reset

The AW-CH397 is reset when PDn pin is asserted low and the internal CPU begins the boot sequence when the PDn pin transitions from low to high.

## 2-5. Power up Timing Sequence




# 3. Host Interfaces

## 3-1. SDIO Interface

The AW-CH397 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless module device.

The AW-CH397 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

Supports SDIO 3.0 Standard

On-chip memory used for CIS

Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes

Special interrupt register for information exchange

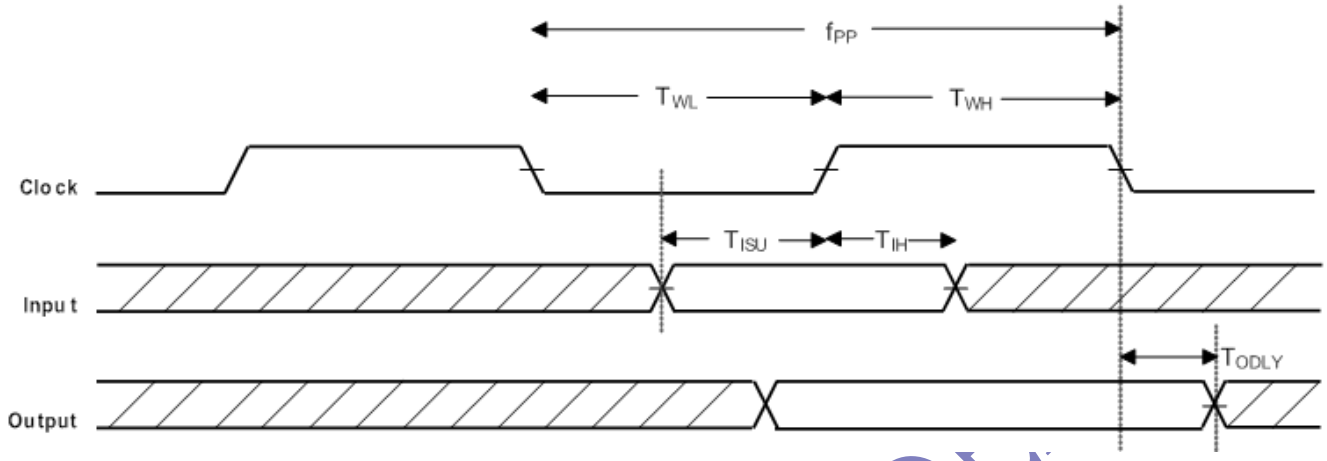
Allows card to interrupt host

### 3-1-1. SDIO Interface Signal Description

| Pin Name | Signal Name | Type | Description |
|---|---|---|---|
| SD_CLK | CLK | I/O | SDIO 1-bit mode: Clock<br>SDIO SPI mode: Clock |
| SD_CMD | CMD | I/O | SDIO 1-bit mode: Command line<br>SDIO SPI mode: Data input |
| SD_DAT[3] | DAT3 | I/O | SDIO 4-bit mode: Data line bit [3]<br>SDIO 1-bit mode: Not used<br>SDIO SPI mode: Chip select (active low) |
| SD_DAT[2] | DAT2 | I/O | SDIO 4-bit mode: Data line bit [2] or Read Wait (optional)<br>SDIO 1-bit mode: Read Wait (optional)<br>SDIO SPII mode: Reserved |
| SD_DAT[1] | DAT1 | I/O | SDIO 4-bit mode: Data line bit [1]<br>SDIO 1-bit mode: Interrupt<br>SDIO SPI mode: Interrupt |
| SD_DAT[0] | DAT0 | I/O | SDIO 4-bit mode: Data line bit [0]<br>SDIO 1-bit mode: Data line<br>SDIO SPI mode: Data output |

## 3-1-2. Default Speed, High Speed Modes (3.3V)

**SDIO Protocol Timing Diagram – Default Speed Mode (3.3V)**




**SDIO Protocol Timing Diagram – HighSpeed Mode (3.3V)**

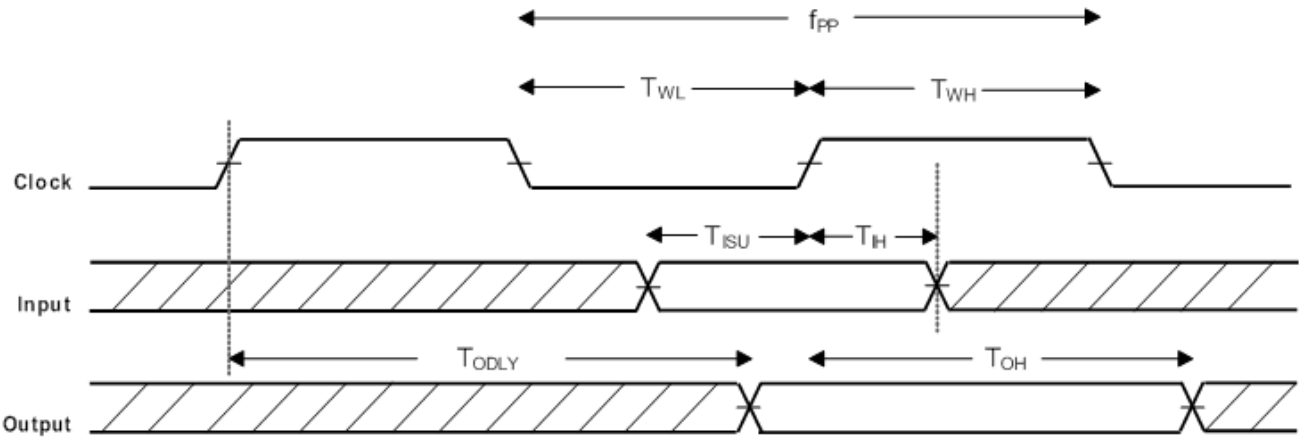



Table shows SDIO Timing Data—Default Speed, High Speed Modes (3.3V)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{PP}$ | Clock Frequency | Default Speed | 0 | -- | 25 | MHz |
| | | High Speed | 0 | -- | 50 | MHz |
| $T_{WL}$ | Clock Low Time | Default Speed | 10 | -- | -- | ns |
| | | High Speed | 7 | -- | -- | ns |
| $T_{WH}$ | Clock High Time | Default Speed | 10 | -- | -- | ns |
| | | High Speed | 7 | -- | -- | ns |
| $T_{ISU}$ | Input Setup Time | Default Speed | 5 | -- | -- | ns |
| | | High Speed | 6 | -- | -- | ns |
| $T_{IH}$ | Input Hold Time | Default Speed | 5 | -- | -- | ns |
| | | High Speed | 2 | -- | -- | ns |
| $T_{ODLY}$ | Output Delay Time<br>CL ≤ 40 pF (1 card) | Default Speed | -- | -- | 14 | ns |
| | | High Speed | --- | -1 | 4 | ns |
| $T_{OH}$ | Output Hold Time | High Speed | 2.5 | -- | -- | ns |

## 3-2. PCI Express Interface

The PCI Express host interface pins are powered from the AVdd18 voltage supply.

## 3-2-1 Differential Tx Output Electricals

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| UI | Unit interval<br>Each UI is 400 ps ±300 PPM.<br>UI does not account for SSC dictated variations. | 399.98 | 400 | 400.12 | ps |
| $V_{Tx\_DIFFpp}$ | Differential peak-to-peak output voltage<br>$V_{Tx\_DIFFpp} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ | 0.800 | -- | 1.2 | V |
| $V_{Tx\_DE\_RATIO}$ | De-emphasized differential output voltage (ratio) | -3.0 | -3.5 | -4.0 | db |
| $T_{Rx\_EYE}$ | Minimum Tx eye width | 0.75 | -- | -- | UI |
| $T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$ | Maximum time between jitter median and maximum deviation from median | -- | -- | 0.125 | UI |
| $T_{Tx\_RISE}$, $T_{Tx\_FALL}$ | D+/D- Tx output rise/fall time | 0.125 | -- | -- | UI |
| $V_{Tx\_CM\_DC\_ACTIVE\_IDLE\_DELTA}$ | Absolute delta of DC common mode voltage during L0 and electrical idle | 0- | - | 100 | mV |
| $V_{Tx\_CM\_DC\_LINE\_DELTA}$ | Absolute delta of DC common mode voltage between D+ and D- | 0- | - | 25 | mV |
| $V_{Tx\_IDLE\_DIFFp}$ | Electrical idle differential peak output voltage | 0 | -- | 20 | mV |
| $V_{Tx\_RCV\_DETECT}$ | Voltage change allowed during receiver detection | -- | -- | 600 | mV |
| $V_{Tx\_DC\_CM}$ | Tx DC common mode voltage | -- | -- | 3.6 | V |
| $I_{Tx\_SHORT}$ | Tx short circuit current limit | -- | -- | 90 | mA |
| $T_{Tx\_IDLE\_MIN}$ | Minimum time spent in electrical idle | 50 | -- | -- | UI |
| $T_{Tx\_IDLE\_SET\_TO\_IDLE}$ | Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set | -- | -- | 20 | UI |
| $T_{Tx\_IDLE\_TO\_DIFF\_DATA}$ | Maximum time to transition to valid Tx specifications after leaving an electrical idle condition | -- | -- | 20 | UI |
| $RL_{Tx\_DIFF}$ | Differential return loss | 10 | -- | -- | dB |
| $RL_{Tx\_CM}$ | Common mode return loss | 6 | -- | -- | dB |
| $C_{Tx}$ | AC coupling capacitor | 75 | -- | 200 | nF |
| $T_{Crosstalk}$ | Crosstalk random timeout | 0 | -- | 1 | ms |

### 3-2-2 Differential Rx Output Electricals

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| UI | Unit interval<br>Each UI is 400 ps ±300 ppm.<br>UI does not account for SSC dictated variations. | 399.98 | 400 | 400.12 | ps |
| $V_{Rx\_DIFFpp}$ | Differential peak-to-peak voltage<br>$V_{Rx\_DIFFpp} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ | 0.175 | -- | 1.2 | V |
| $T_{Rx\_EYE}$ | Minimum receiver eye width | 0.4 | -- | -- | UI |
| $T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$ | Maximum time between jitter median and maximum deviation from median | -- | -- | 0.3 | UI |
| $V_{Rx\_CM\_ACp}$ | AC peak common mode input voltage | -- | -- | 150 | mV |
| $RL_{Rx\_DIFF}$ | Differential return loss | 10 | -- | -- | dB |
| $RL_{Rx\_CM}$ | Common mode return loss | 6 | -- | -- | dB |
| $Z_{Rx\_DIFF\_DC}$ | DC differential input impedance | 80 | 100 | 120 | Ω |
| $Z_{Rx\_DC}$ | DC input impedance | 40 | 50 | 60 | Ω |
| $Z_{Rx\_HIGH\_IMP\_DC\_POS}$ | Powered down DC input impedance positive | 50 | -- | -- | k |
| $Z_{Rx\_HIGH\_IMP\_DC\_NEG}$ | Powered down DC input impedance negative | 1 | -- | -- | kΩ |
| $V_{Rx\_IDLE\_DET\_DIFFpp}$ | Electrical idle detect threshold | 65 | -- | 175 | mV |
| $T_{Rx\_IDLE\_DET\_DIFF\_ENTERTIME}$ | Unexpected electrical idle enter detect threshold integration time | -- | -- | 10 | ms |
| $L_{Rx\_SKEW}$ | Total skew | --- | -2 | 0 | ns |

## 3-3. USB Interface

The USB device interface is compliant with the Universal Serial Bus Specification, Revision 2.0, April 27, 2000. A USB host uses the USB cable bus and the USB 2.0 device interface to communicate with the chip.

The main features of the USB device interface include:

High/full speed operation (480/12 Mbps)

Suspend/host resume/device resume (remote wake-up)

Built-in DMA engine that reduces interrupt loads on the embedded processor and reduces the system bus bandwidth requirement for serving the USB device operation

The USB 2.0 device interface is designed with 3.3V signal level pads.

### 3-3-1. USB 2.0 Device Interface Description

Table shows the signal mapping between the AW-CH397 and the USB Specification, Revision 2.0.

| Pin Name | USB 2.0 Specification Pin Name | Description |
|---|---|---|
| B11<br>VBAT_USB_IN | VBUS | USB Bus Power Supply<br>On-board regulator regulates voltage from VBUS level to voltage levels used by USB PHY. |
| -- | GND | USB Bus Ground<br>Common ground on SoC device. |
| D11<br>USB_DP | D+ | USB Bus Data Plus<br>One of the differential data pair. |
| C11<br>USB_DM | D- | USB Bus Data Minus<br>One of the differential data pair. |

### 3-3-2. USB 2.0 Device Functional Description

The device controller uses internal Scatter/Gather DMA engine to transfer the transmit packet from internal SRAM to USB and the receive packet from USB to internal SRAM. The Device IN Endpoint DMA (DIEPDMAn) and Device OUT Endpoint DMA (DOEPDMAn) registers are used by the DMA engine to access the base descriptor. The application is interrupted after the programmed transfer size extracted from the descriptors is transmitted or received. By using registers, interrupts, and special data structures, the device controller can communicate with the device controller driver (application/software) about bus states, host request, and data transfer status. The device controller driver also has all of the routines to respond to the device framework commands issued by a USB host, so it controls the attachment, configuration, operation, and detachment of the device.

## 3-4. High-Speed UART Interface

The AW-CH397 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data. Table shows the rates supported.

The UART interface features include:

FIFO mode permanently selected for transmit and receive operations

Two pins for transmit and receive operations

Two flow control pins

Interrupt triggers for low-power, high throughput operation

The UART interface operation includes:

Upload boot code to the internal CPU (for debug purposes)

Support diagnostic tests

Support data input/output operations for peripheral devices connected through a standard UART interface

**UART Baud Rates Supported**

| Baud Rate | | | | |
|---|---|---|---|---|
| 1200 | 38400 | 460800 | 1500000 | 3000000 |
| 2400 | 57600 | 500000 | 1843200 | 3250000 |
| 4800 | 76800 | 921600 | 2000000 | 3692300 |
| 9600 | 115200 | 1000000 | 2100000 | 4000000 |
| 19200 | 230400 | 1382400 | 2764800 | -- |

### 3-4-1. UART Interface Signal Description

Table shows the standard UART signal names on the device.

| Signal Name | 16550 Standard Pin Name | Description |
|---|---|---|
| ***Data Bus*** | | |
| UART_SIN | SIN | Serial data input from modem, data set, or peripheral device |
| UART_SOUT | SOUT | Serial data output from modem, data set, or peripheral device |
| ***Modem Control*** | | |
| UART_RTSN | RTS | Request To Send output to modem, data set, or peripheral device (active low) |
| UART_CTSN | CTS | Clear To Send input from modem, data set, or peripheral device (active low) |

## 3-4-2. UART Interface Functional Description

### 3-4-2-1. Booting from UART

When booting from the UART, the AW-CH397 device has the following requirements:

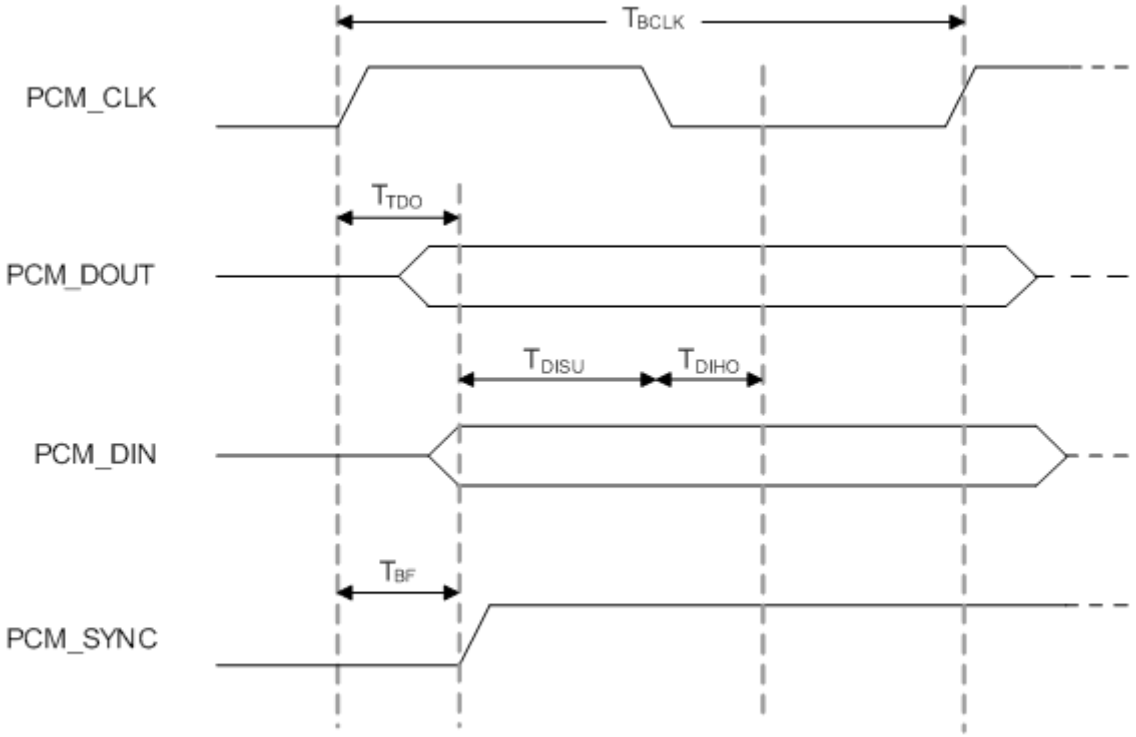
| System Requirement | Description |
|---|---|
| Number of data bits | 8 bits |
| Stop bits | 1 bit |
| Parity | No parity |
| Baud Rate | 115200 |

### 3-4-2-2. UART as Test Port

Test diagnostic programs may be uploaded to the CPU through the UART interface. During execution, the diagnostic program transmits performance and status information through the UART by performing a write to the PBU address space designated to the UART.

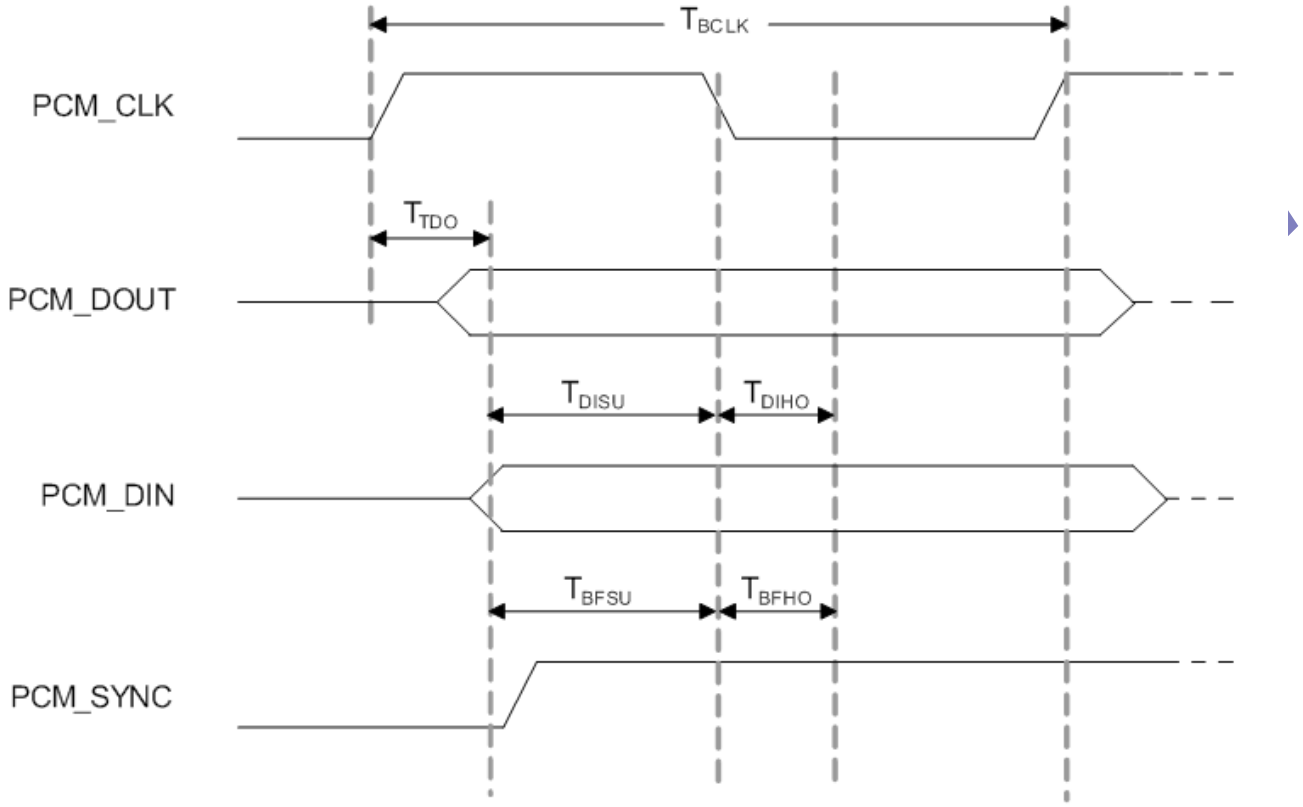
## 3-5. PCM Interface

### 3-5-1. PCM Timing Specification – Master Mode




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{BCLK}$ | -- | -- | -- | 2/2.048 | -- | MHz |
| Duty $Cycle_{BCLK}$ | -- | -- | 0.4 | 0.5 | 0.6 | -- |
| $T_{BCLK\ rise/fall}$ | -- | -- | -- | 3 | -- | ns |
| $T_{DO}$ | -- | -- | -- | -- | 15 | ns |
| $T_{DISU}$ | -- | -- | 20 | -- | -- | ns |
| $T_{DIHO}$ | -- | -- | 15 | -- | -- | ns |
| $T_{BF}$ | -- | -- | -- | -- | 15 | ns |

## 3-5-2. PCM Timing Specification – Slave Mode




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{BCLK}$ | -- | -- | -- | 2/2.048 | -- | MHz |
| Duty $Cycle_{BCLK}$ | -- | -- | 0.4 | 0.5 | 0.6 | -- |
| $T_{BCLK\ rise/fall}$ | -- | -- | -- | 3 | -- | ns |
| $T_{DO}$ | -- | -- | -- | -- | 30 | ns |
| $T_{DISU}$ | -- | -- | 15 | -- | -- | ns |
| $T_{DIHO}$ | -- | -- | 10 | -- | -- | ns |
| $T_{BFSU}$ | -- | -- | 15 | -- | -- | ns |
| $T_{BFHO}$ | -- | -- | 10 | -- | -- | ns |

# 4. Pin Definition

| PIN No. | Name | Description | Type |
|---|---|---|---|
| A1 | VBAT_IN | VBAT power supply for LDO input internal | I |
| A2 | GND | Ground | |
| A3 | VBUCK11_IN | 1.1V core power supply | I |
| A4 | VBUCK11_OUT | 1.1V LDO Voltage Output | O |
| A5 | 3V3_USB_IN | 3.3V Analog Power Supply for USB | I |
| A6 | SD_CMD | SDIO Command/response (input/output) | I/O |
| A7 | SD_CLK | SDIO Clock input | I |
| A8 | SD_DAT[2] | SDIO Data line Bit[2] | I/O |
| A9 | SD_DAT[3] | SDIO Data line Bit[3] | I/O |
| A10 | SLP_CLK_IN | Sleep Clock Input.<br>Used for WLAN and Bluetooth low-power modes.<br>External sleep clock of 32.768 KHz must be used for auto reference clock calibration and for WLAN/Bluetooth low power operation. | I |
| B1 | GND | Ground | |
| B2 | GND | Ground | |
| B3 | GND | Ground | |
| B4 | VIO_SD | 1.8V/3.3V Digital I/O SDIO Power Supply | |
| B5 | GND | Ground | |
| B6 | PCIE_TX_P | PCI Express Transmit Data—Positive | |
| B7 | PCIE_TX_N | PCI Express Transmit Data—Negative | |
| B8 | SD_DAT[0] | SDIO Data line Bit[0] | I/O |
| B9 | SD_DAT[1] | SDIO Data line Bit[1] | I/O |
| B10 | GPIO[3] | 1. GPIO Mode: GPIO[3] (input/output)<br>2. USB Mode: VBUS_ON (input) | I |
| C1 | VBUCK18_IN | 1.8V analog power supply | I |
| C2 | GND | Ground | |
| C3 | GND | Ground | |
| C4 | GND | Ground | |
| C5 | PCIE_RX_P | PCI Express Receive Data—Positive | |
| C6 | PCIE_RCLK_P | PCI Express Differential Clock Input—Positive | |
| C7 | GPIO[13] | 1. PCIe Mode: PCIe host indication to disable the WLAN function of the device (input) (active low)<br>2. GPIO Mode: GPIO[13] | I/O |
| C8 | GPIO[14] | GPIO[14] (input/output) | I/O |
| C9 | GPIO[2]/LTE_SIN | 1. GPIO Mode: GPIO[2] (input/output)<br>2. LTE Mode: UART_LTE_SIN (input) | I |
| C10 | VIO | 1.8V/2.5V/3.3V Digital I/O Power Supply | I |
| D1 | VBUCK18_OUT | 1.8V LDO Voltage Output | O |

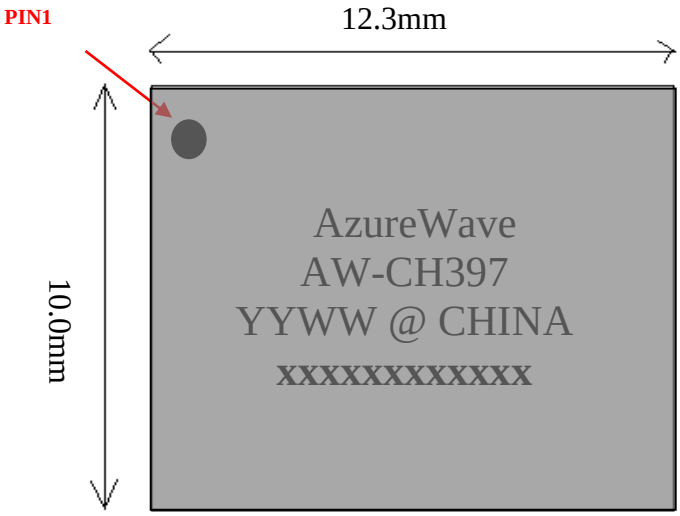
| PIN No. | Name | Description | Type |
|---|---|---|---|
| D2 | PDn | Full Power Down (input) (active low)<br>0 = full power down mode<br>1 = normal mode<br>• Connect to power down pin of host or VBAT<br>• External host required to drive this pin high for normal operation<br>Internal pull-up to VBAT_IN with a 51K ohm. | I |
| D3 | NC | No Connect | |
| D4 | NC | No Connect | |
| D5 | PCIE_RX_N | PCI Express Receive Data—Negative | |
| D6 | PCIE_RCLK_N | PCI Express Differential Clock Input—Negative | |
| D7 | GPIO[22] | 1. GPIO Mode: GPIO[22] (input/output)<br>2. I2S Mode: I2S_LRCLK (input/output)<br>• Output if master<br>• Input if slave<br>3. PCM Mode: PCM_SYNC (input/output)<br>• Output if master<br>• Input if slave | I/O |
| D8 | GPIO[21] | 1. GPIO Mode: GPIO[21] (input/output)<br>2. I2S Mode: I2S_BCLK (input/output)<br>• Output if master<br>• Input if slave<br>3. PCM Mode: PCM_CLK (input/output)<br>• Output if master<br>• Input if slave | I |
| D9 | NC | No Connect | |
| D10 | NC | No Connect | |
| E1 | 3V3_IN | 3.3V Analog Power Supply | |
| E2 | NC | No Connect | |
| E3 | NC | No Connect | |
| E4 | NC | No Connect | |
| E5 | GPIO[12] | 1. GPIO Mode: GPIO[12] (input/output)<br>2. PCIe Mode: PCIE_PERSTn (input) (active low)<br>3. PCIe host indication to reset the device. | |
| E6 | PCIE_CLKREQ_N | PCIe clock request (input/output) (active low) | I/O |
| E7 | GPIO[19] | 1. GPIO Mode: GPIO[19] (input/output)<br>2. I2S Mode: I2S_DIN (input)<br>3. PCM Mode: PCM_DIN (input) | I/O |
| E8 | GPIO[0] | 1. GPIO Mode: GPIO[0] (input/output)<br>2. Oscillator Mode: XOSC_EN/CLK_REQ (output) (active high)<br>0 = disable external oscillator<br>1 = enable external oscillator | O |
| E9 | NC | No Connect | |
| E10 | NC | No Connect | |
| F1 | NC | No Connect | |
| F2 | NC | No Connect | |
| F3 | NC | No Connect | |
| F4 | NC | No Connect | |

| PIN No. | Name | Description | Type |
|---|---|---|---|
| F5 | GPIO[4] | 1. GPIO Mode: GPIO[4] (input/output)<br>2. UART Mode: UART_SOUT (output) | O |
| F6 | PCIE_WAKEUP_N | PCIe wake signal (output) (active low) | I/O |
| F7 | GPIO[20] | 1. GPIO Mode: GPIO[20] (input/output)<br>2. I2S Mode: I2S_DOUT (output)<br>3. PCM Mode: PCM_DOUT (output) | I/O |
| F8 | GPIO[1]/LTE_SOUT | 1. GPIO Mode: GPIO[1] (input/output)<br>2. LTE Mode: UART_LTE_SOUT (output) | I |
| F9 | SER_CLK | EEPROM Mode: SER_CLK | O |
| F10 | USB_DP | USB Serial Differential Data Positive | I/O |
| G1 | NC | No Connect | |
| G2 | TDI | JTAG test data (input) | I |
| G3 | TDO | JTAG test data (output) | O |
| G4 | GPIO[6] | 1. GPIO Mode: GPIO[6] (input/output)<br>2. UART Mode: UART_CTSn (input) (active low) | I |
| G5 | GPIO[5] | 1. GPIO Mode: GPIO[5] (input/output)<br>2. UART Mode: UART_SIN (input) | I |
| G6 | GPIO[10] | 1. GPIO Mode: GPIO[10] (input/output)<br>2. EEPROM Mode: SER_WB<br>3. I2S Mode: I2S_CCLK (input/output)<br>• Output if master<br>• Input if slave<br>4. PCM Mode: PCM_MCLK (optional, output)<br>• Output if master<br>• Input if slave<br>5. Optional clock used for some codecs. | I/O |
| G7 | GND | Ground | |
| G8 | GND | Ground | |
| G9 | SER_DAT | EEPROM Mode: SER_DAT | O |
| G10 | USB_DM | USB Serial Differential Data Negative | I/O |
| H1 | NFC_VDDANT | Decoupling of internal supply | |
| H2 | TCK | JTAG test clock (input) | I |
| H3 | GPIO[9] | 1. GPIO Mode: GPIO[9] (input/output)<br>2. LED Mode: LED_OUT_BT (output) | I |
| H4 | GPIO[11] | 1. GPIO Mode: GPIO[11] (input/output)<br>2. LED Mode: LED_OUT_NFC (output) | I/O |
| H5 | GPIO[7] | 1. GPIO Mode: GPIO[7] (input/output)<br>2. UART Mode: UART_RTSn (output) (active low) | O |
| H6 | GND | Ground | |
| H7 | GND | Ground | |
| H8 | GND | Ground | |
| H9 | SER_CSN | EEPROM Mode: SER_CSn | I/O |
| H10 | 3V3_RF_IN | 3.3V Analog Power Supply for RF | I |

| PIN No. | Name | Description | Type |
|---|---|---|---|
| J1 | VIO_RF | 1.8V/3.3V Analog I/O RF Power Supply | I |
| J2 | TMS | JTAG controller select (input) | I |
| J3 | GPIO[8] | 1. GPIO Mode: GPIO[8] (input/output)<br>2. LED Mode: LED_OUT_WLAN (output) | |
| J4 | GND | Ground | |
| J5 | GND | Ground | |
| J6 | GND | Ground | |
| J7 | GND | Ground | |
| J8 | GND | Ground | |
| J9 | GND | Ground | |
| J10 | GND | Ground | |
| K1 | NC | No Connect | |
| K2 | RF_CNTL1_P | RF Control 1—RF Control Output High (output) | |
| K3 | RF_CNTL0_N | RF Control 0—RF Control Output Low (output) | |
| K4 | GND | Ground | |
| K5 | CONFIG_HOST[1] | Configuration Pins.<br>Firmware Boot Options<br>No hardware impact. Software reads and boots accordingly. | I |
| K6 | CONFIG_HOST[0] | Configuration Pins.<br>Firmware Boot Options<br>No hardware impact. Software reads and boots accordingly. | I |
| K7 | CONFIG_HOST[2] | Configuration Pins.<br>Firmware Boot Options<br>No hardware impact. Software reads and boots accordingly. | I |
| K8 | CONFIG_HOST[3] | Configuration Pins.<br>Firmware Boot Options<br>No hardware impact. Software reads and boots accordingly. | I |
| K9 | GND | Ground | |
| K10 | ANT_2G5G_A | Antenna-A IO port for WLAN (50 ohms, 2.4GHz/5GHz band) | I/O |
| L1 | GND | Ground | |
| L2 | GND | Ground | |
| L3 | GND | Ground | |
| L4 | GND | Ground | |
| L5 | GND | Ground | |
| L6 | GND | Ground | |
| L7 | GND | Ground | |
| L8 | GND | Ground | |
| L9 | GND | Ground | |
| L10 | GND | Ground | |
| M1 | GND | Ground | |
| M2 | GND | Ground | |

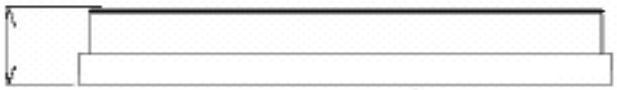
| PIN No. | Name | Description | Type |
|---|---|---|---|
| M3 | GND | Ground | |
| M4 | GND | Ground | |
| M5 | GND | Ground | |
| M6 | GND | Ground | |
| M7 | GND | Ground | |
| M8 | GND | Ground | |
| M9 | GND | Ground | |
| M10 | GND | Ground | |
| N1 | GND | Ground | |
| N2 | GND | Ground | |
| N3 | GND | Ground | |
| N4 | GND | Ground | |
| N5 | GND | Ground | |
| N6 | ANT_2G5G_B_BT | Antenna-B IO port for WLAN/BT (50 ohms, 2.4GHz/5GHz band) | I/O |
| N7 | GND | Ground | |
| N8 | GND | Ground | |
| N9 | GND | Ground | |
| N10 | GND | Ground | |

# 5. Mechanical Information




Dimension Tolerance: ±0.1mm

1.00mm(Max)



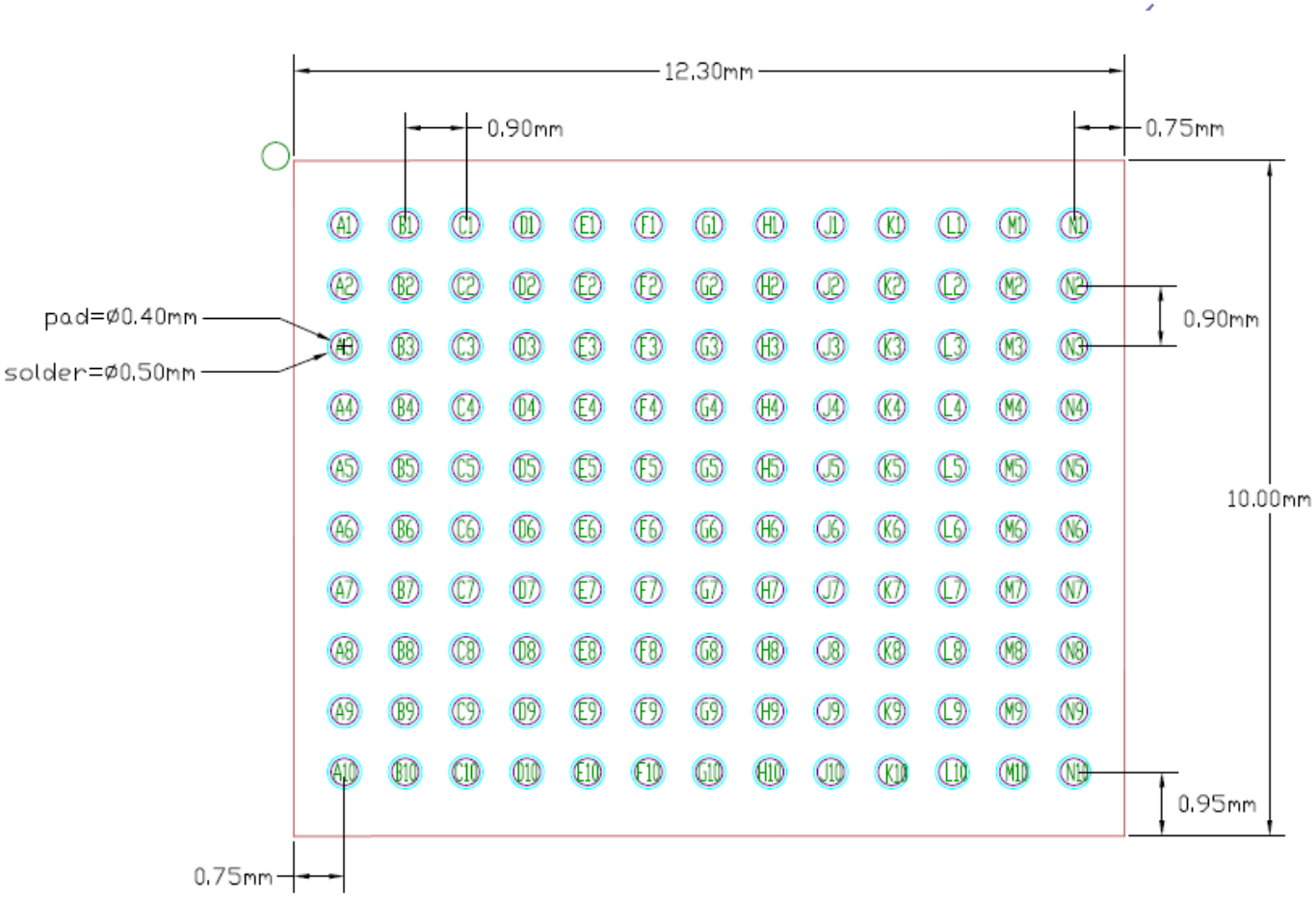
Side View

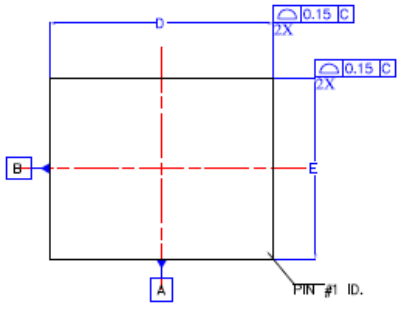
## 5-1. Package Outline Drawing

## 5-2. MODULE FOOTPRINT

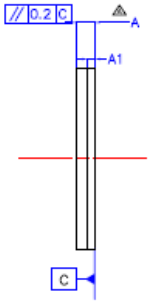
AW-CH397 TOP VIEW PCB LAYOUT FOOTPRINT

Unit: mm

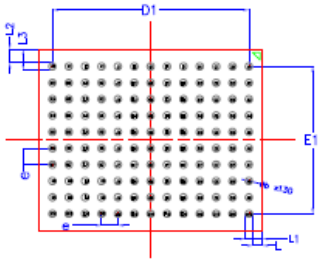





TOP VIEW




SIDE VIEW




BOTTOM VIEW

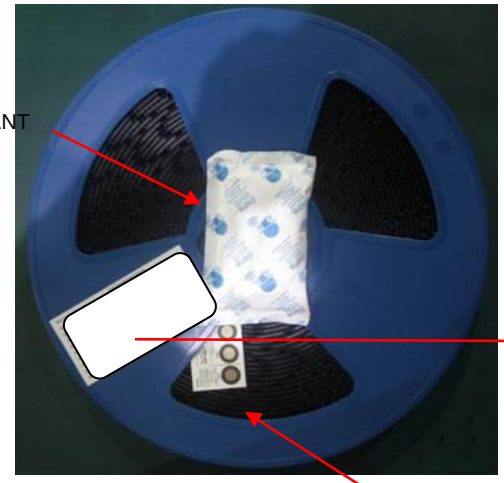
ALL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.920 | 0.960 | 1.000 | 0.036 | 0.038 | 0.039 |
| A1 | 0.320 | 0.360 | 0.400 | 0.013 | 0.014 | 0.016 |
| D | 12.200 | 12.300 | 12.400 | 0.480 | 0.484 | 0.488 |
| D1 | – | 10.800BSC | – | – | 0.425BSC | – |
| E | 9.900 | 10.000 | 10.100 | 0.390 | 0.394 | 0.398 |
| E1 | – | 8.100BSC | – | – | 0.319BSC | – |
| b | 0.350 | 0.400 | 0.450 | 0.014 | 0.016 | 0.018 |
| L | 0.500 | 0.550 | 0.600 | 0.020 | 0.022 | 0.024 |
| L1 | 0.900 | 0.950 | 1.000 | 0.035 | 0.037 | 0.039 |
| L2 | 0.700 | 0.750 | 0.800 | 0.028 | 0.030 | 0.031 |
| L3 | 1.100 | 1.150 | 1.200 | 0.043 | 0.045 | 0.047 |
| e | – | 0.90BSC | – | – | 0.035 | – |

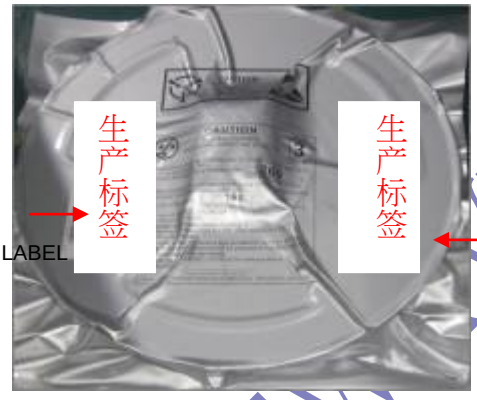
| | | | | | | |
|---|---|---|---|---|---|---|
| AzureWave | AzureWave Technologies(Shanghai) Inc. | | | | | NR.TOL |
| TITLE | LGA 12.3x10.0x1.00(MAX)130PIN PACKAGE OUTLINE DWG | | | DRN | Merry Pan | 05/Mar/14 |
| | | | | DEN | Merry Pan | 05/Mar/14 |
| DWG NO. | PO-12851-01 | | REV. 01 | CHK | | |
| UNIT | mm | SCALE 1:1 | PAGE 2/2 | APD | | |

# 6. Shipping Information

## 6-1




## 6-2




## 6-3

## 6-4


## 6-5

1 Carton= 5 Boxes


## 6-6


**Note: 1 tape reel = 1 box = 2,000pcs**

**1 carton = 5 boxes = 5 * 2,000pcs=10,000pcs**