

AW-AM510

**IEEE 802.11 1X1 a/b/g/n Wireless LAN
+ Bluetooth 5.2 Combo
12 x 12 LGA Module**

Datasheet

Rev. F

DF

For Standard

Features

WLAN

- ◆ Support 802.11 a/b/g/n
- ◆ Dual bands: 2.4 GHz and 5 GHz
- ◆ Single stream 802.11n with 20/40 MHz channels for 5G and 20 MHz only for 2.4G
- ◆ Up to MCS7 data rates (150 Mbps)
- ◆ Support 802.11mc for location
- ◆ Dynamic Rapid Channel Switching (DRCS) for simultaneous and power efficient operation in 2.4 GHz and 5 GHz bands
- ◆ Interface to coexist with 802.15.4, LTE, or

other radios.

- ◆ Security: WPA3, WPA2, WPA2 and WPA mix mixed mode, WEP

Bluetooth

- ◆ Full Bluetooth 5.2 features
- ◆ Long range - 4x coverage
- ◆ 2 Mbps data rate - 2x faster
- ◆ Improved advertisement capacity- enables more IoT services
- ◆ Audio interface: I2S and PCM
- ◆ Security: AES

Revision History

Document NO: R2-2510-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/09/17	DCN018312	<ul style="list-style-type: none"> ● Draft version 	Renton Tao	N.C Chen
B	2021/04/19	DCN021490	<ul style="list-style-type: none"> ● Modify pin table ● Modify datasheet form ● Modify block diagram ● Modify spec. table 	Roger Liu	N.C Chen
C	2021/09/02	DCN023371	<ul style="list-style-type: none"> ● Add ESD information ● Modify spec. table ● Add power consumption 	Roger Liu	N.C Chen
D	2021/11/03	DCN024024	<ul style="list-style-type: none"> ● Modify host interface ● Modify pin table pin37/40 description 	Roger Liu	N.C Chen
E	2021/12/24	DCN025066	<ul style="list-style-type: none"> ● Update pin table detail ● Update block diagram ● Update BT feature to 5.2 	Roger Liu	N.C Chen
F	2022/12/16	DCN028498	<ul style="list-style-type: none"> ● Update power consumption format ● Update SUSCLK voltage level from VDDIO to 1.8V 	Roger Liu	N.C Chen

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the IEEE 802.11a/b/g/n WLAN, BT, combo module – **AW-AM510**. With four advanced radio technologies integrated into a module, AW-AM510 provides the best and most convenient SMT process. The module is targeted to mobile devices including, Tablet PC, Portable Media Players (PMPs), Portable Navigation Devices (PNDs), Personal Digital Assistants (PDAs), Tracking Devices, Gaming Devices which need convenient SMT process, low power consumption.

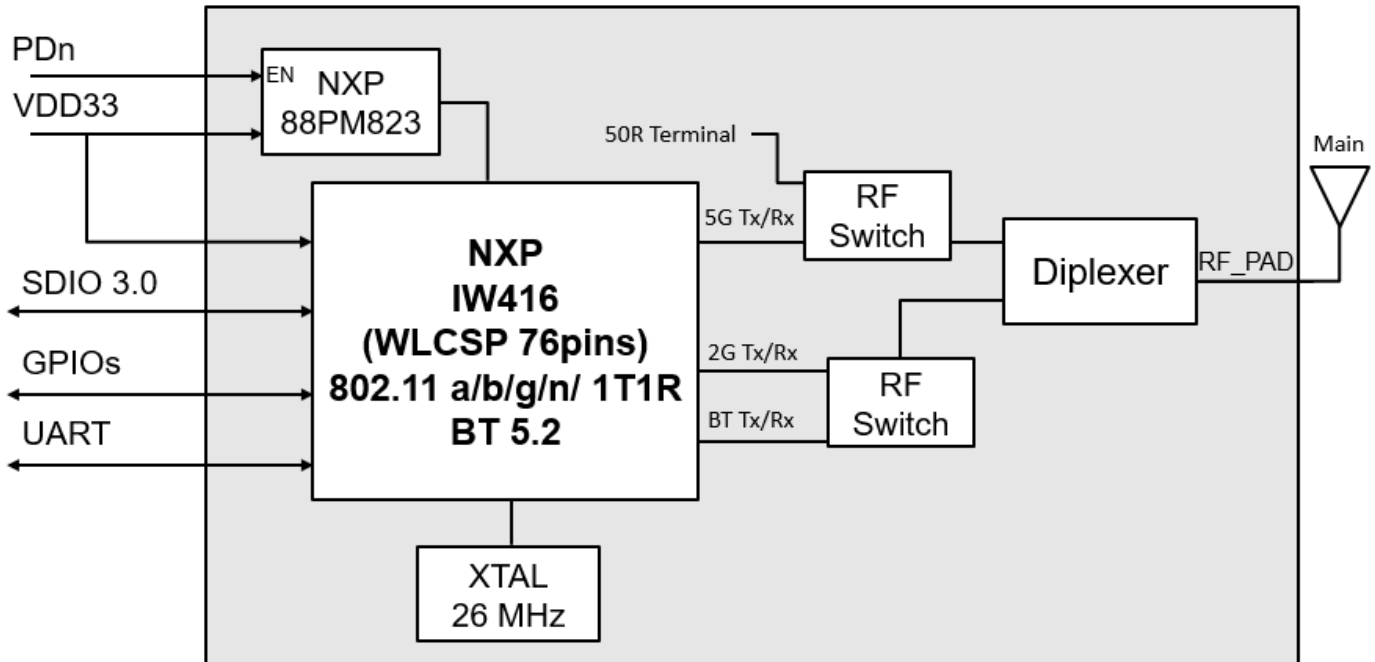
By using AW-AM510, the customers can easily integrate the Wi-Fi, BT, by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11a/b/g/n standard, the AW-AM510 uses **DSSS, OFDM, DBPSK, DQPSK, CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-AM510.

The AW-AM510 supports standard interface **SDIO3.0 for WLAN, UART for BT**. AW-AM510 is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the AW-AM510 is the best solution for the consumer electronics and the tablet PC.

1.2 Block Diagram

A simplified block diagram of the AW-AM510 module is depicted in the figure below.



AW-AM510 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n Wi-Fi with Bluetooth 5.2 Combo Module
Major Chipset	NXP IW416 WLCSP (76p)
Host Interface	WiFi + BT <ul style="list-style-type: none"> ● SDIO + UART
Dimension	12 mm X 12 mm x 2 mm(Max)
Form Factor	LGA module, 44 pins
Antenna	ANT(Main) : WiFi/Bluetooth → TX/RX
Weight	0.2g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n Wi-Fi with Bluetooth 5.2 Combo Module
WLAN VID/PID	NA
WLAN SVID/SPID	NA
Frequency Range	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM

<p>Number of Channels</p>	<p>2.4GHz:</p> <ul style="list-style-type: none"> ■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11 ■ China, Australia, Most European Countries - 1 ~ 13 ■ Japan, 1 ~ 13 <p>5GHz:</p> <ul style="list-style-type: none"> ■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165 ■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140 ■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165 																																								
<p>Output Power (Board Level Limit)*</p>	<p>2.4G</p> <table border="1" data-bbox="500 789 1482 1052"> <thead> <tr> <th></th> <th>Min</th> <th>Typ</th> <th>Max</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td>11b (11Mbps) @EVM<35%</td> <td>15.5</td> <td>17</td> <td>18.5</td> <td>dBm</td> </tr> <tr> <td>11g (54Mbps) @EVM≤-27 dB</td> <td>14.5</td> <td>16</td> <td>17.5</td> <td>dBm</td> </tr> <tr> <td>11n (HT20 MCS7) @EVM≤-28 dB</td> <td>12.5</td> <td>14</td> <td>15.5</td> <td>dBm</td> </tr> </tbody> </table> <p>5G</p> <table border="1" data-bbox="500 1115 1482 1377"> <thead> <tr> <th></th> <th>Min</th> <th>Typ</th> <th>Max</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td>11a (54Mbps) @EVM≤-25 dB</td> <td>14</td> <td>16</td> <td>18</td> <td>dBm</td> </tr> <tr> <td>11n (HT20 MCS7) @EVM≤-27 dB</td> <td>13</td> <td>15</td> <td>17</td> <td>dBm</td> </tr> <tr> <td>11n (HT40 MCS7) @EVM≤-27 dB</td> <td>12</td> <td>14</td> <td>16</td> <td>dBm</td> </tr> </tbody> </table>		Min	Typ	Max	Unit	11b (11Mbps) @EVM<35%	15.5	17	18.5	dBm	11g (54Mbps) @EVM≤-27 dB	14.5	16	17.5	dBm	11n (HT20 MCS7) @EVM≤-28 dB	12.5	14	15.5	dBm		Min	Typ	Max	Unit	11a (54Mbps) @EVM≤-25 dB	14	16	18	dBm	11n (HT20 MCS7) @EVM≤-27 dB	13	15	17	dBm	11n (HT40 MCS7) @EVM≤-27 dB	12	14	16	dBm
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11n (HT40 MCS7) @EVM≤-27 dB	12	14	16	dBm																																					

Receiver Sensitivity	2.4G				
		Min	Typ	Max	Unit
	11b (11Mbps)	-	-86	-83	dBm
	11g (54Mbps)	-	-73	-70	dBm
	11n (HT20 MCS7)	-	-69	-66	dBm
	5G				
		Min	Typ	Max	Unit
11a (54Mbps)	-	-71	-68	dBm	
11n (HT20 MCS7)	-	-68	-65	dBm	
11n (HT40 MCS7)	-	-66	-63	dBm	
Data Rate	WLAN: 802.11b : 1, 2, 5.5, 11Mbps 802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n : Maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)				
Security	<ul style="list-style-type: none"> ■ WiFi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP ■ BT: AES 				

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	Description
Bluetooth Standard	Full Bluetooth 5.2 features
Frequency Range	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: $\pi/4$ -DQPSK Payload 3M: 8DPSK
Output Power	

	Min	Typ	Max	Unit
BDR	0	2	4	dBm
EDR	0	2	4	dBm
Low Energy	0	2	4	dBm

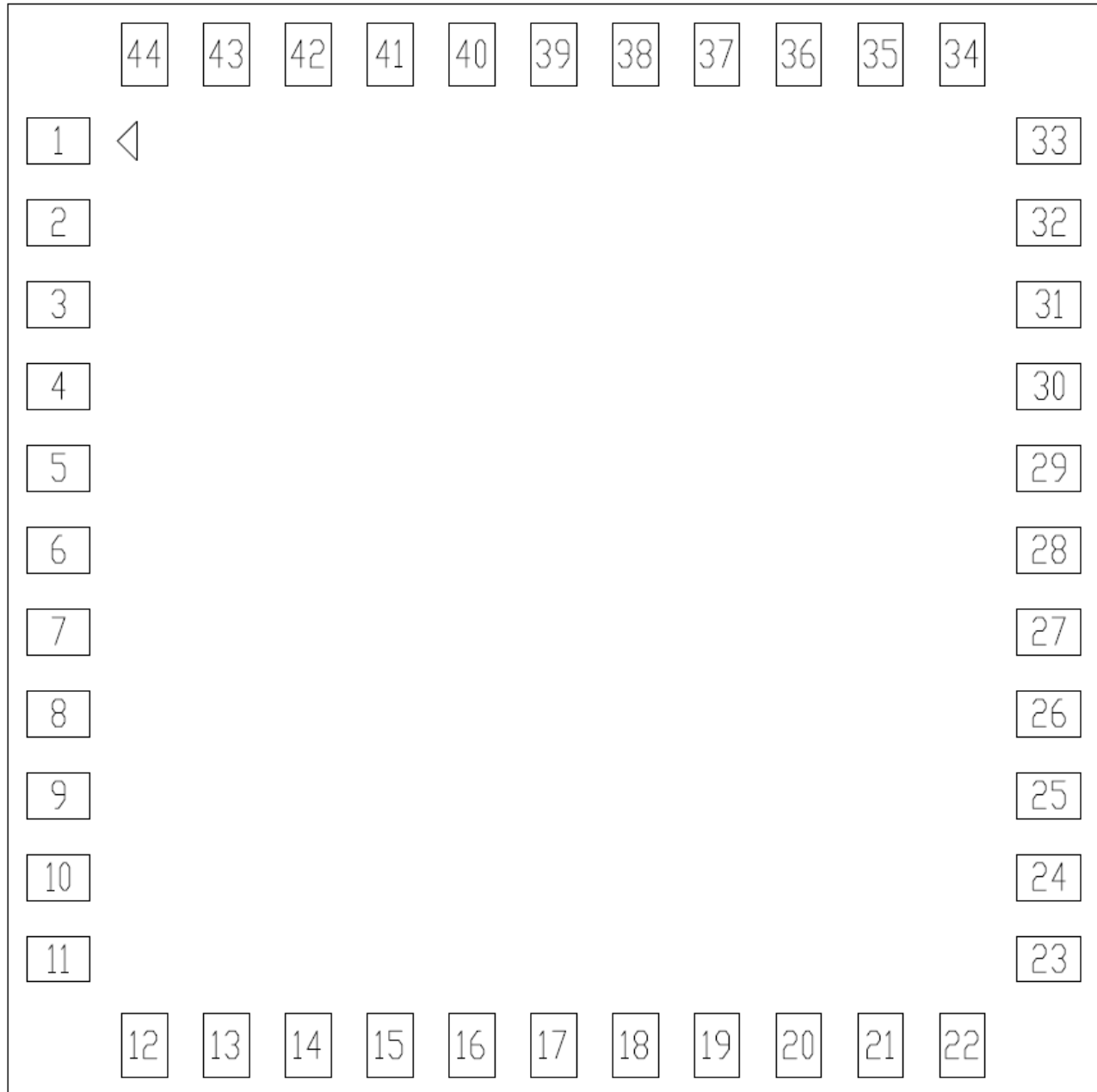
Receiver Sensitivity	BT Sensitivity (BER<0.1%)				
		Min	Typ	Max	Unit
	BDR(DH1)	-	-83	-80	dBm
	EDR(2DH5)	-	-88	-85	dBm
	EDR(3DH5)	-	-83	-80	dBm
Low Energy	-	-96	-93	dBm	

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	0 °C to +70 °C
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 °C to +85 °C
Storage Humidity	Less than 60% R.H.
ESD Protection	
Human Body Model	±2kV
Changed Device Model	±500V

2. Pin Definition

2.1 Pin Map



AW-AM510 Pin Map (top view)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND1	Ground	---	---
2	RF_ANT	Option for RF I/O pin out	---	I/O
3	GND3	Ground	---	---
4	NC4	Floating Pin, No connect to anything.	---	Floating
5	NC5	Floating Pin, No connect to anything.	---	Floating
6	HOST_WAKE_BT	GPIO Mode : GPIO[12]. BT Device Wake	VDDIO	I
7	BT_WAKE_HOST	GPIO Mode : GPIO[0]. BT Host Wake	VDDIO	O
8	NC8	Floating Pin, No connect to anything.	---	Floating
9	VBAT	3.3V power voltage source input	3.3V	P
10	NC10	Floating Pin, No connect to anything.	---	Floating
11	NC11	Floating Pin, No connect to anything.	---	Floating
12	PDn	Full Power-down pin connects to internal PMIC (input) (active low) 0 = full power-down mode 1 = normal mode	3.3V	I
13	WL_WAKE_HOST	GPIO Mode : GPIO[1]. WL Host Wake	VDDIO	I/O
14	SDIO_DATA2	SDIO Data line Bit[2]	VDDIO	I/O
15	SDIO_DATA3	SDIO Data line Bit[3]	VDDIO	I/O
16	SDIO_CMD	SDIO Command	VDDIO	I/O
17	SDIO_CLK	SDIO Clock input	VDDIO	I
18	SDIO_DATA0	SDIO Data line Bit[0]	VDDIO	I/O
19	SDIO_DATA1	SDIO Data line Bit[1]	VDDIO	I/O
20	GND20	Ground	---	---
21	NC21	Floating Pin, No connect to anything.	---	Floating
22	VDDIO	1.8V/3.3V Digital I/O Power Supply	1.8V/3.3V	P
23	NC23	Floating Pin, No connect to anything.	---	Floating
24	SUSCLK_IN	External Low Power Clock input(32.768KHz) (optional)	1.8V	I
25	BT_PCM_OUT	PCM Data output	VDDIO	I/O
26	BT_PCM_CLK	PCM Clock	VDDIO	I/O
27	BT_PCM_IN	PCM data input	VDDIO	I/O
28	BT_PCM_SYNC	PCM sync signal	VDDIO	I/O
29	GPIO[3]	GPIO[3] /JTAG_TDO	VDDIO	I/O
30	GPIO[2]	GPIO[2] /JTAG_TDI	VDDIO	I/O
31	GND31	Ground	---	---
32	NC32	Floating Pin, No connect to anything.	---	Floating
33	GND33	Ground	---	---
34	GPIO[15]	Independent software reset for Bluetooth /	VDDIO	I

		GPIO[15] / JTAG_TMS		
35	NC35	Floating Pin, No connect to anything.	---	Floating
36	GND36	Ground	---	---
37	GPIO[14]	Independent software reset for Wi-Fi / GPIO[14] / JTAG_TCK	VDDIO	I/O
38	MWS_SOUT	WCI-2 MWS coexistence serial transport interface(TX)	1.8V	O
39	MWS_SIN	WCI-2 MWS coexistence serial transport interface(RX)	1.8V	I
40	HOST_WAKE_WL	GPIO Mode : GPIO[13]. Host-to-WLAN wake-up	VDDIO	I/O
41	UART_RTS_N	UART_RTSn (active low)	VDDIO	O
42	UART_TXD	UART_SOUT	VDDIO	O
43	UART_RXD	UART_SIN	VDDIO	I
44	UART_CTS_N	UART_CTSn(active low)	VDDIO	I

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	-	3.3	3.96	V
VDDIO	I/O power supply	-	3.3	4.0	V
		-	1.8	2.2	

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	3.14	3.3	3.46	V
VDDIO	1.8V/3.3V digital I/O power supply	2.97	3.3	3.47	V
		1.62	1.8	1.98	

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V _{IH}	Input high voltage	0.7*V _{IO}	-	V _{IO} +0.4	V

V_{IL}	Input low voltage	-0.4	-	$0.3 \cdot V_{IO}$	
V_{OH}	Output high voltage	$V_{IO} - 0.4$	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	$0.7 \cdot V_{IO}$	-	$V_{IO} + 0.4$	V
V_{IL}	Input low voltage	-0.4	-	$0.3 \cdot V_{IO}$	
V_{OH}	Output High Voltage	$V_{IO} - 0.4$	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.4 Host Interface

3.4.1 SDIO Interface

The AW-AM510 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-AM510 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

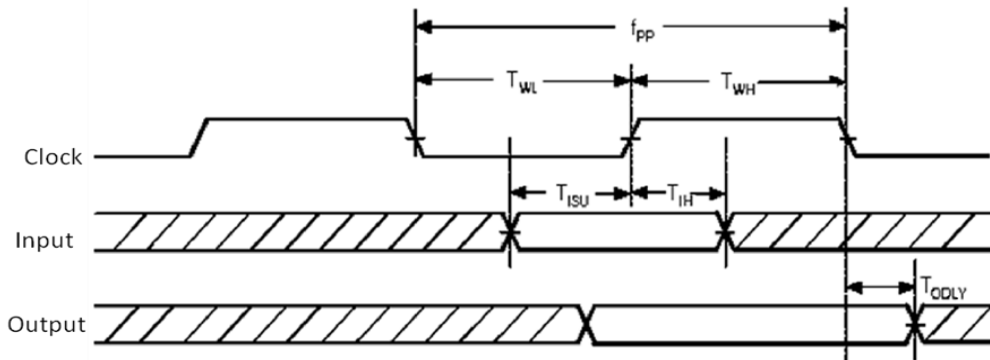
- ◆ Support SDIO 3.0 Standard.
- ◆ On-chip memory used for CIS.
- ◆ Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- ◆ Special interrupt register for information exchange.
- ◆ Allows card to interrupt host.

SDIO Interface Signals

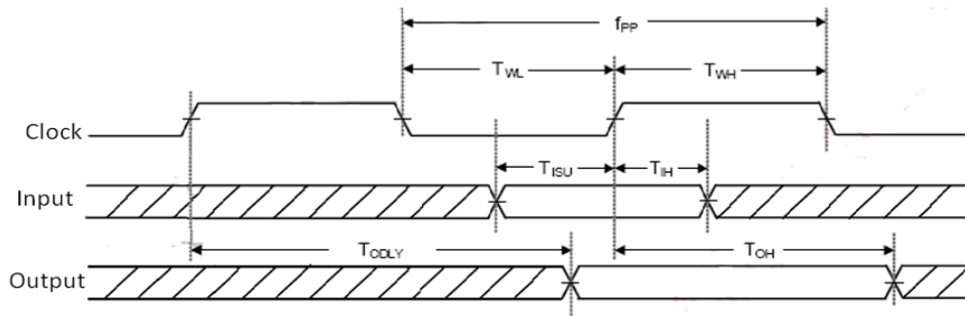
AW-AM510 SDIO Pin Name	Type	Description
SDIO_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

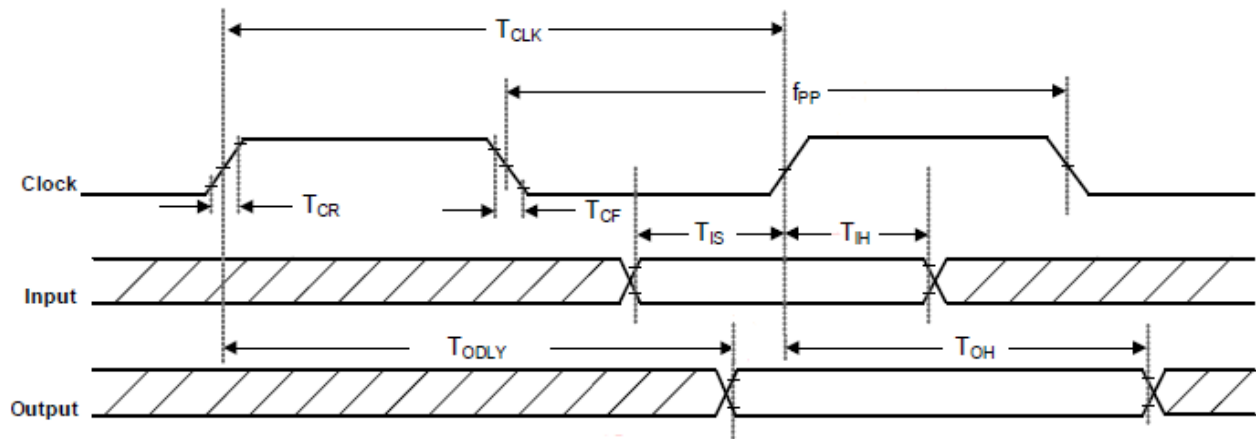


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f _{pp}	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T _{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T _{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T _{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T _{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T _{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≤ 40pF (1 card)	High Speed	--	--	14	ns
T _{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

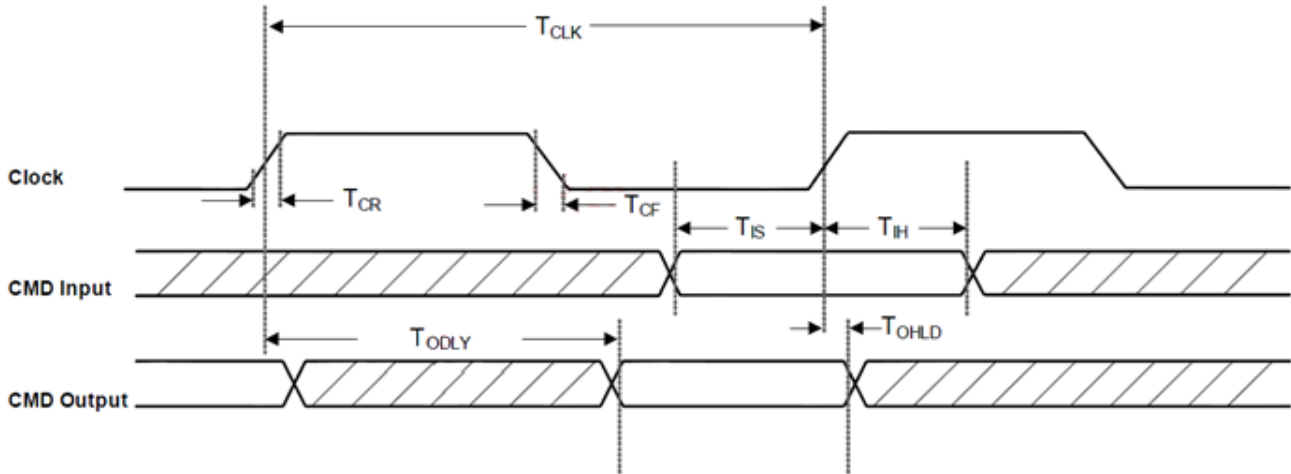


SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

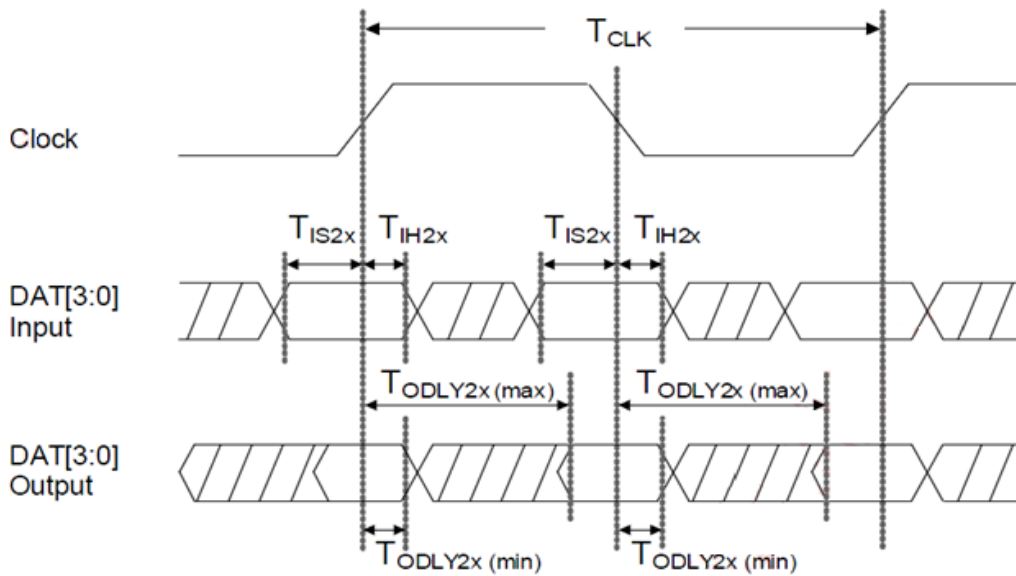
Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR}, T_{CF}	Rise time, fall time TCR, TCF < 2ns(max) at 100MHz CCARD = 10pF	SDR12/25/50	-	-	$0.2 * T_{CLK}$	ns
T_{ODLY}	Output Delay Time CL ≤ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL = 15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

3.4.2.3 DDR50 Mode (50MHz) (1.8V)



SDIO CMD Timing Diagram - DDR50 Mode (50 MHz)



SDIO DAT[3:0] Timing Diagram - DDR50 Mode¹ (50 MHz)

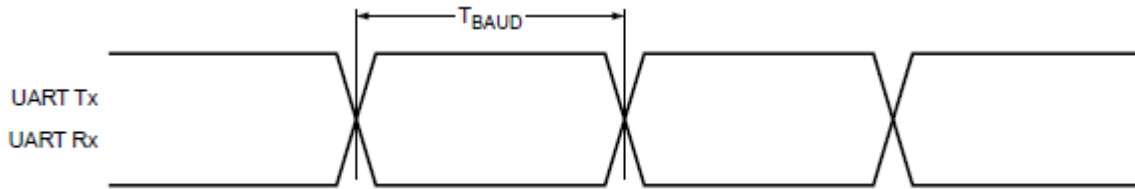
¹ In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T _{CLK}	Clock time	DDR50	20	-	-	ns
T _{CR} , T _{CF}	Rise time, fall time	DDR50	-	-	0.2*T _{CLK}	Ns
Clock Duty		DDR50	45	-	55	%
CMD Input						
T _{IS}	Input setup time	DDR50	6	-	-	ns
T _{IH}	Input hold time	DDR50	0.8	-	-	ns
CMD Output						
T _{ODLY}	Output delay time during data transfer mode	DDR50	-	-	13.7	ns
T _{OHLd}	Output hold time	DDR50	1.5	-	-	ns
DAT [3:0] Input						
T _{IS2X}	Input setup time	DDR50	3	-	-	ns
T _{IH2X}	Input hold time	DDR50	0.8	-	-	ns
DAT [3:0] Output						
T _{ODLY2X(max)}	Output delay time during data transfer mode	DDR50	-	-	7	ns
T _{ODLY2X(min)}	Output hold time	DDR50	1.5	-	-	ns

SDIO Timing Data - DDR50 Mode (50MHz)

3.4.3.High-Speed UART Interface

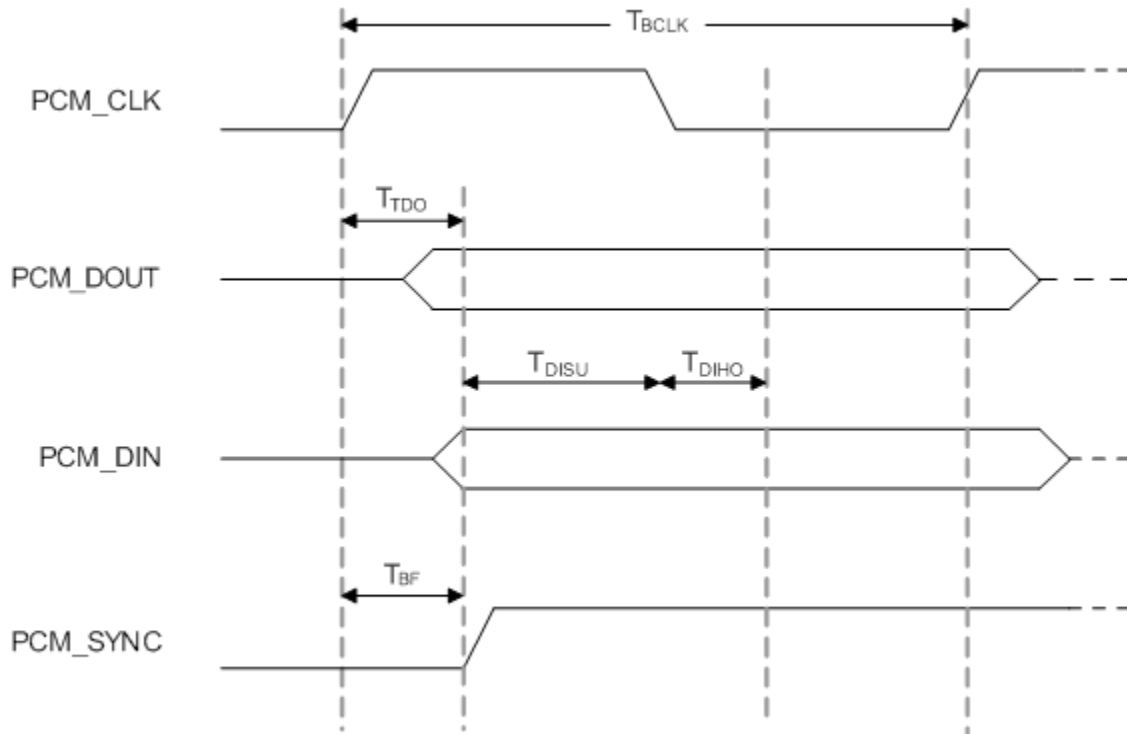
The AW-AM510 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz or 40MHz input clock	250	-	-	ns

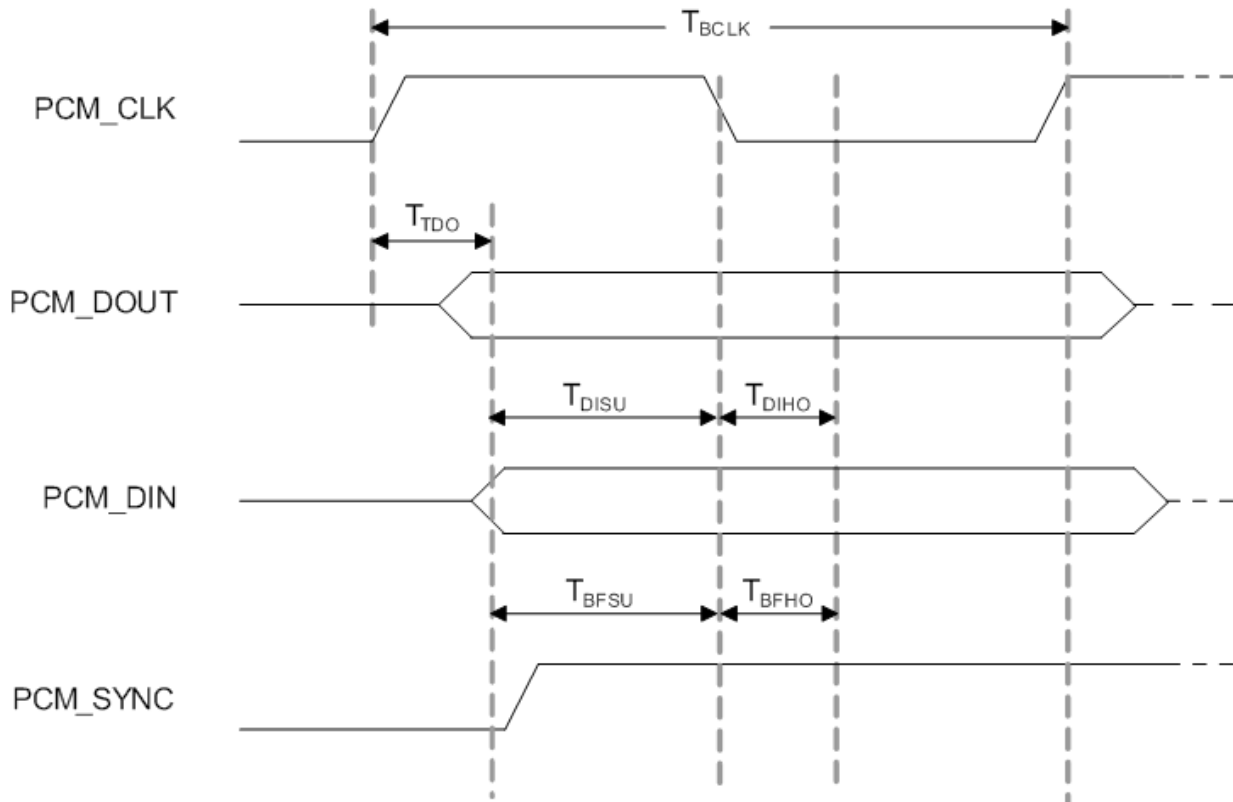
3.4.4 PCM Interface

3.4.4.1 PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty Cycle $_{BCLK}$	--	--	0.4	0.5	0.6	--
T_{BCLK} rise/fall	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

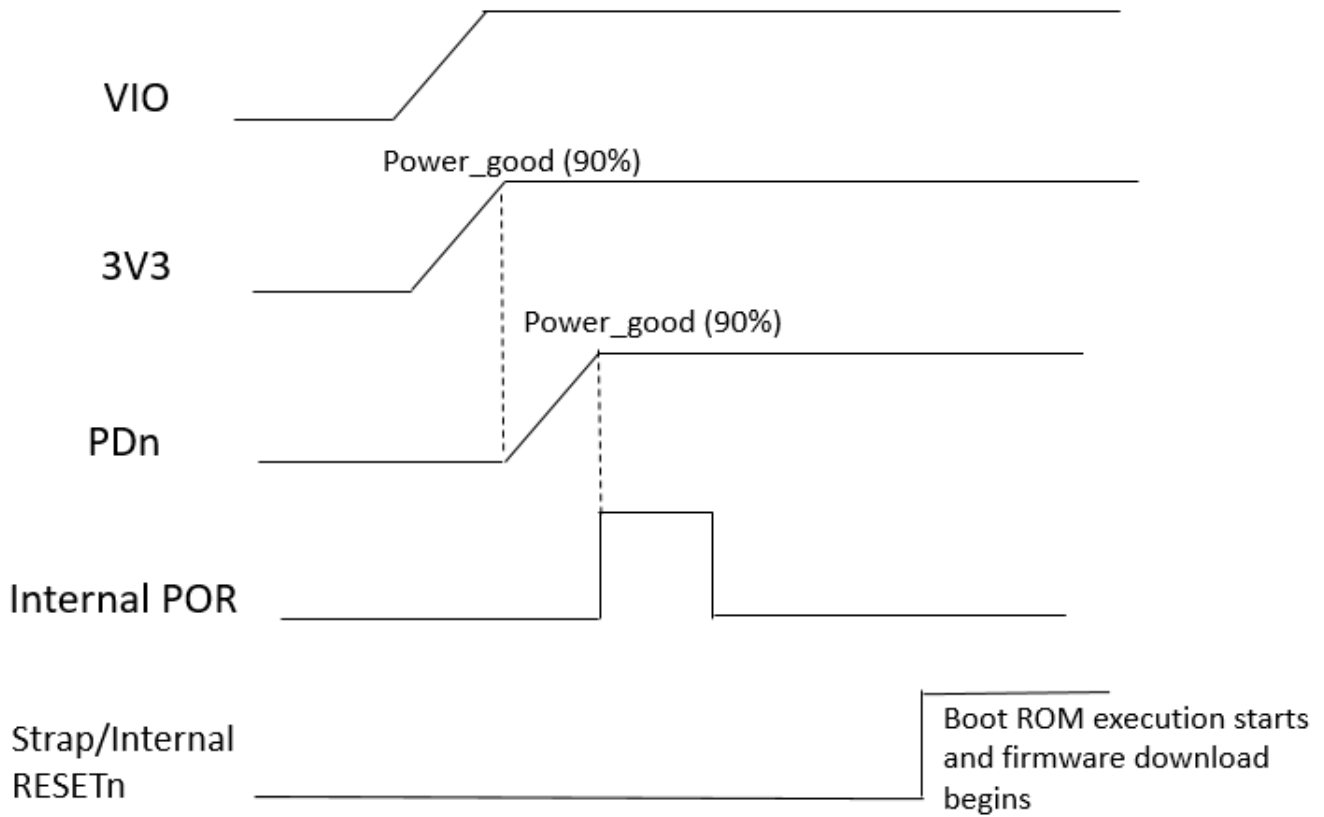
3.4.4.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty Cycle $_{BCLK}$	--	--	0.4	0.5	0.6	--
T_{BCLK} rise/fall	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}	--	--	10	--	--	ns

3.5 Timing Sequence

AW-AM510 power up timing sequence.



3.6 Power Consumption

3.6.1 WLAN

No.	Item			VBAT_IN=3.3V(mA)		
				Max.	Avg.	
1	Power Down			0.082		
2	DeepSleep (Not associated with AP)			0.253	0.239	
3	Power Save (2.4GHz)			52	2.9	
4	Power Save (5GHz)			63	3.4	
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit		
				Max.	Avg.	Duty Mean (%)
2.4	11b@1Mbps	20	17	277	238	46
	11b@11Mbps	20	17	267	243	46
	11g@6Mbps	20	16	171	159	43
	11g@54Mbps	20	16	97	94	24
	11n@MCS0	20	14	141	131	39
	11n@MCS7	20	14	47	45	5
5	11a@6Mbps	20	16	204	188	42
	11a@54Mbps	20	16	119	116	24
	11n@MCS0	20	15	181	169	39
	11n@MCS7	20	15	66	63	5
	11n@MCS	40	14	119	108	19
	11n@MCS7	40	14	64	63	3
Band (GHz)	Mode	BW(MHz)		Receive		
				Max.	Avg.	
2.4	11b@1Mbps	20		34	34	
	11n@MCS7	20		36	36	
5	11a@6Mbps	20		52	52	
	11n@MCS7	40		61	61	

No.	Item			VDDIO=1.8V(mA)	
				Max.	Avg.
1	Power Down			0.2uA	
2	Sleep (Not associated with AP)			0.079	0.079
3	Power Save (2.4GHz)			0.079	0.076
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit	
				Max.	Avg.
2.4	11b@1Mbps	20	17	0.032	0.032
Band (GHz)	Mode	BW(MHz)		Receive	
				Max.	Avg.

2.4	11b@1Mbps	20	0.032	0.032
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3.6.2 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	VBAT_IN=3.3V(mA)	
				Max.	Avg.
1	Sleep	n/a	n/a	0.253	0.239
2	Transmit	DH5	2	22	21
3	Receive	DH5	n/a	22	21

No.	Mode	Packet Type	RF Power (dBm)	VDDIO=1.8V(mA)	
				Max.	Avg.
1	Sleep	n/a	n/a	0.079	0.079
2	Transmit	DH5	2	0.049	0.049
3	Receive	DH5	n/a	0.049	0.049

3.7 Sleep Clock(Optional)

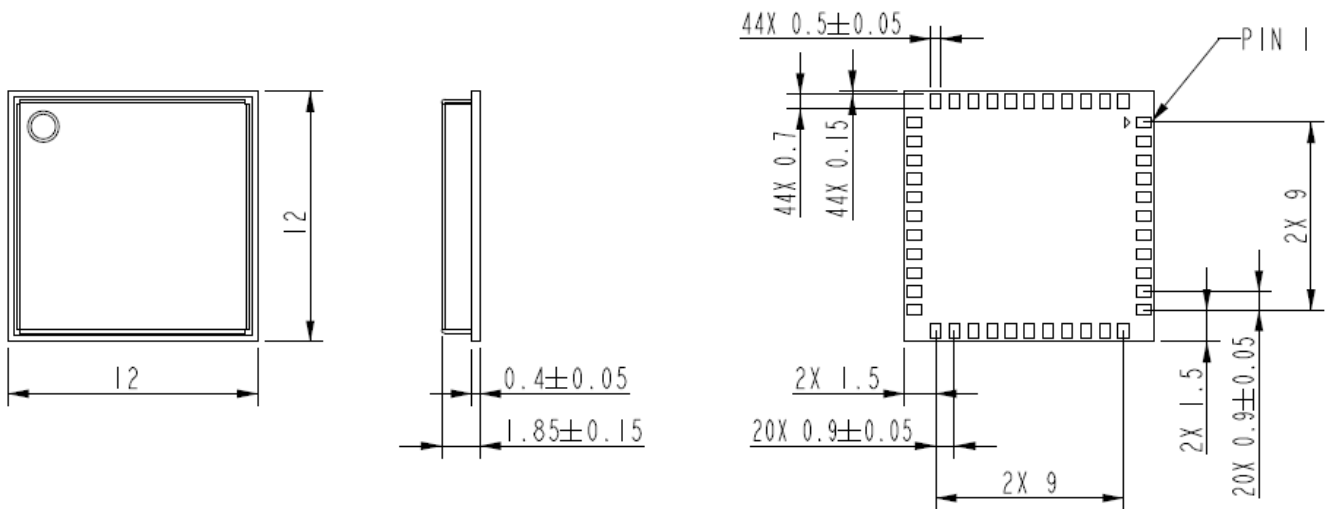
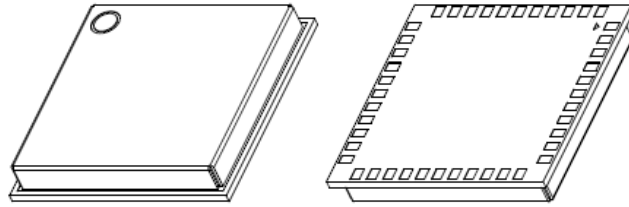
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock frequency range/ accuracy ■ CMOS input clock signal type ■ ± 250 ppm (initial, aging, temperature)	-	32.768	-	kHz
PN	Phase noise requirement (@ 100KHz)	-	-125	-	dBc/Hz
Jc	Cycle jitter	-	1.5	-	ns (RMS)
SR	Slew rate limit (10-90%)	-	-	100	ns
DC	Duty cycle tolerance	20	-	80	%

4. Mechanical Information

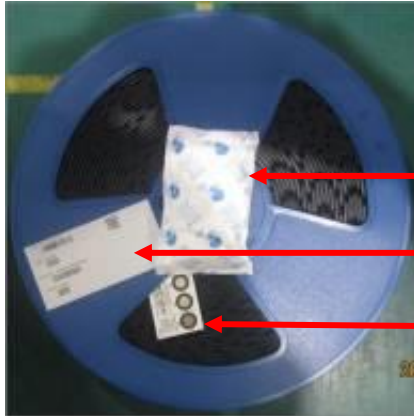
4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.1mm

5. Packing Information

1. One reel can pack 1,500pcs 12x12 LGA modules
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



One desiccant

One production label

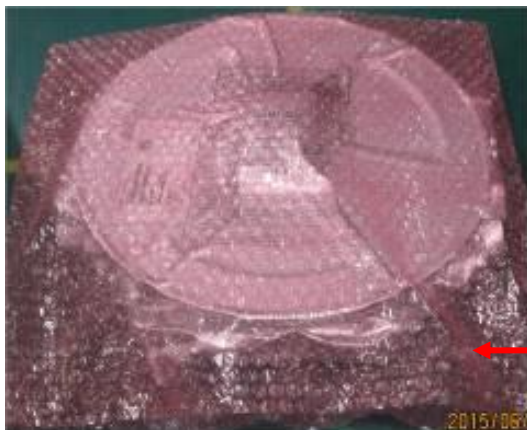
One humidity indicator card

3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



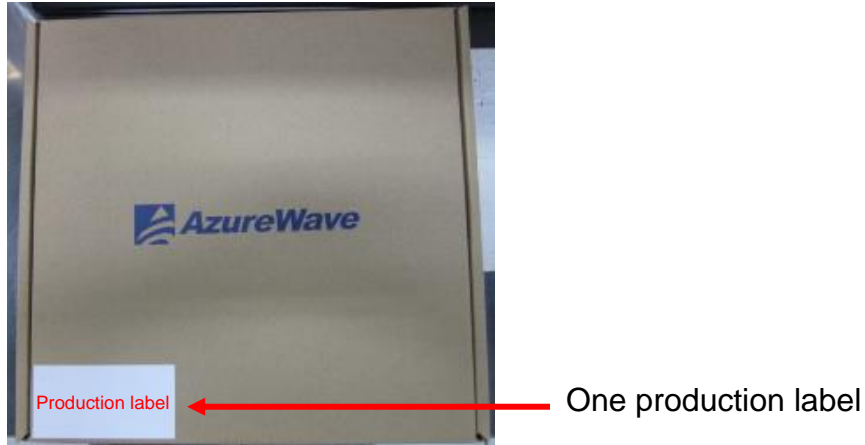
One production label

4. A bag is put into the anti-static pink bubble wrap



One anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box



6. 5 inner boxes could be put into one carton



7. Sealing the carton by AzureWave tape



8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton

One carton label
出貨標籤

One box label
箱號標籤

