AzureWave Technologies, Inc.

AW-AM510AN

IEEE 802.11 1X1 a/b/g/n Wireless LAN + Bluetooth 5.2 Combo LGA Module with Printed Antenna

Datasheet

Rev. B

DF

For Standard

Features

WLAN

- Support 802.11 a/b/g/n standards.
- Operates on Dual bands: 2.4 GHz and 5 GHz
- Provides single-stream 802.11n with 20/40 MHz channels for 5G and 20 MHz only for 2.4G
- Achieves data rates up to MCS7 (150 Mbps).
- Supports 802.11mc for location services.
- Features Dynamic Rapid Channel Switching (DRCS) for simultaneous and power-efficient operation in the 2.4 GHz and 5 GHz bands.
- Includes interfaces for coexistence with 802.15.4, LTE, or other radio technologies.
- Offers robust security options: WPA3, WPA2, WPA2/WPA mixed mode, and WEP.

Bluetooth

- Incorporates full Bluetooth 5.2 functionality.
- Provides extended range with 4x coverage.
- Offers a 2 Mbps data rate, which is 2x faster.
- Enhances advertisement capacity, enabling more IoT services.
- Supports audio interfaces: I2S and PCM.
- Ensures security with AES encryption.

Revision History

Document NO: R2-2510AN-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2023/12/27	DCN030797	• Draft version	Grace Yang	N.C Chen
B	2024/5/13	DCN031885	• Update Mechanical Information	Grace Yang	N.C Chen

AzureWave Technologies, Inc.

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the **AW-AM510AN**, an IEEE 802.11a/b/g/n WLAN and Bluetooth (BT) combo module. This module seamlessly integrates four advanced radio technologies, making AW-AM510AN the ideal choice for achieving the most convenient Surface Mount Technology (SMT) process. The module is designed for mobile devices, including **Tablet PCs**, **Portable Media Players (PMPs)**, **Portable Navigation Devices (PNDs)**, **Personal Digital Assistants (PDAs)**, **Tracking Devices**, and **Gaming Devices**, all of which require a convenient SMT process and low power consumption.

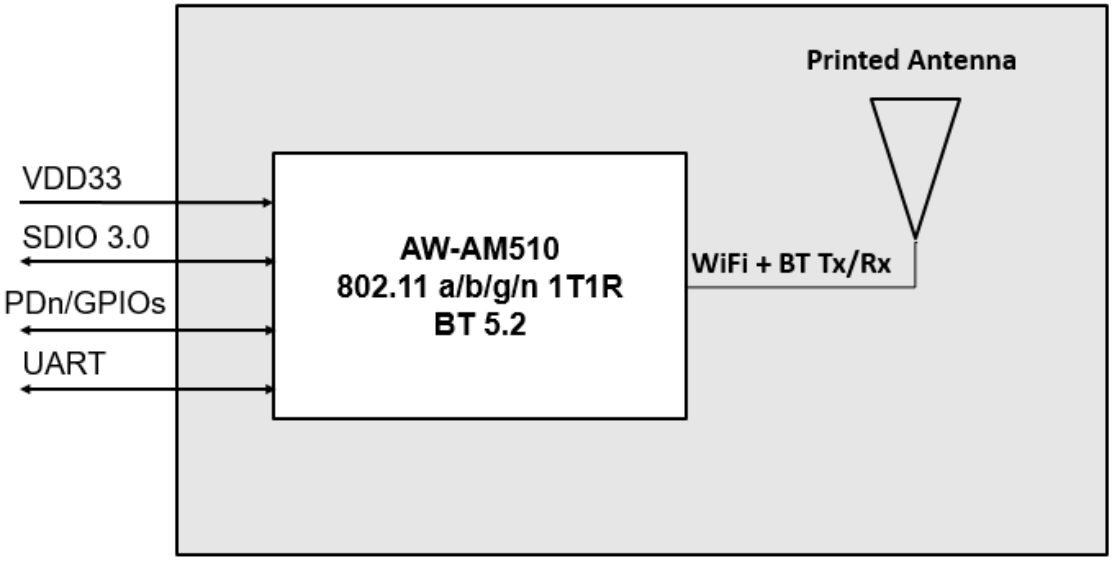
By utilizing the AW-AM510AN, customers can effortlessly integrate Wi-Fi and BT functionalities using a single combo module. This offers several benefits, including **exceptional design flexibility**, **a high success rate in SMT processes**, **shorter development cycles**, and **faster time-to-market**.

In compliance with the IEEE 802.11a/b/g/n standard, the AW-AM510AN utilizes **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK**, and **QAM** baseband modulation technologies. Its high level of integration and comprehensive implementation of power management functions specified in the IEEE 802.11 standard effectively minimize system power requirements when using the AW-AM510AN.

The AW-AM510AN supports standard interfaces, utilizing **SDIO 3.0 for WLAN** and **UART for BT**. It is compatible with multiple mobile processors for various applications. With its combination of versatile features and outstanding performance, the AW-AM510AN stands as the optimal solution for consumer electronics and Tablet PCs.

1.2 Block Diagram

A simplified block diagram of the AW-AM510AN module is depicted in the figure below.



AW-AM510AN Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n Wi-Fi with Bluetooth 5.2 Combo Module with Printed Antenna
Major Chipset	NXP IW416 WLCSP (76p)
Host Interface	WiFi + BT ● SDIO + UART
Dimension	28mm(L) x 18mm(W) x 2.7mm(T)
Form Factor	LGA module, 110 pins
Antenna	ANT(Printed Antenna) ：WiFi/Bluetooth → TX/RX
Weight	TBD

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n Wi-Fi with Bluetooth 5.2 Combo Module
WLAN VID/PID	NA
WLAN SVID/SPID	NA
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM

<table>
<tr><td>Number of Channels</td><td>2.4GHz:
■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11
■ China, Australia, Most European Countries - 1 ~ 13
■ Japan, 1 ~ 13

5GHz:
■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165
■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140
■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power
(Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)
@EVM<35%</td><td>15.5</td><td>17</td><td>18.5</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦-27 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)
@EVM≦-25 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦-27 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)
@EVM≦-27 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-86</td><td>-83</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-73</td><td>-70</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-69</td><td>-66</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-68</td><td>-65</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n : Maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)</td></tr>
<tr><td>Security</td><td>■ WiFi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP
■ BT: AES</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Full Bluetooth 5.2 features</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK
Payload 2M: π/4-DQPSK
Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

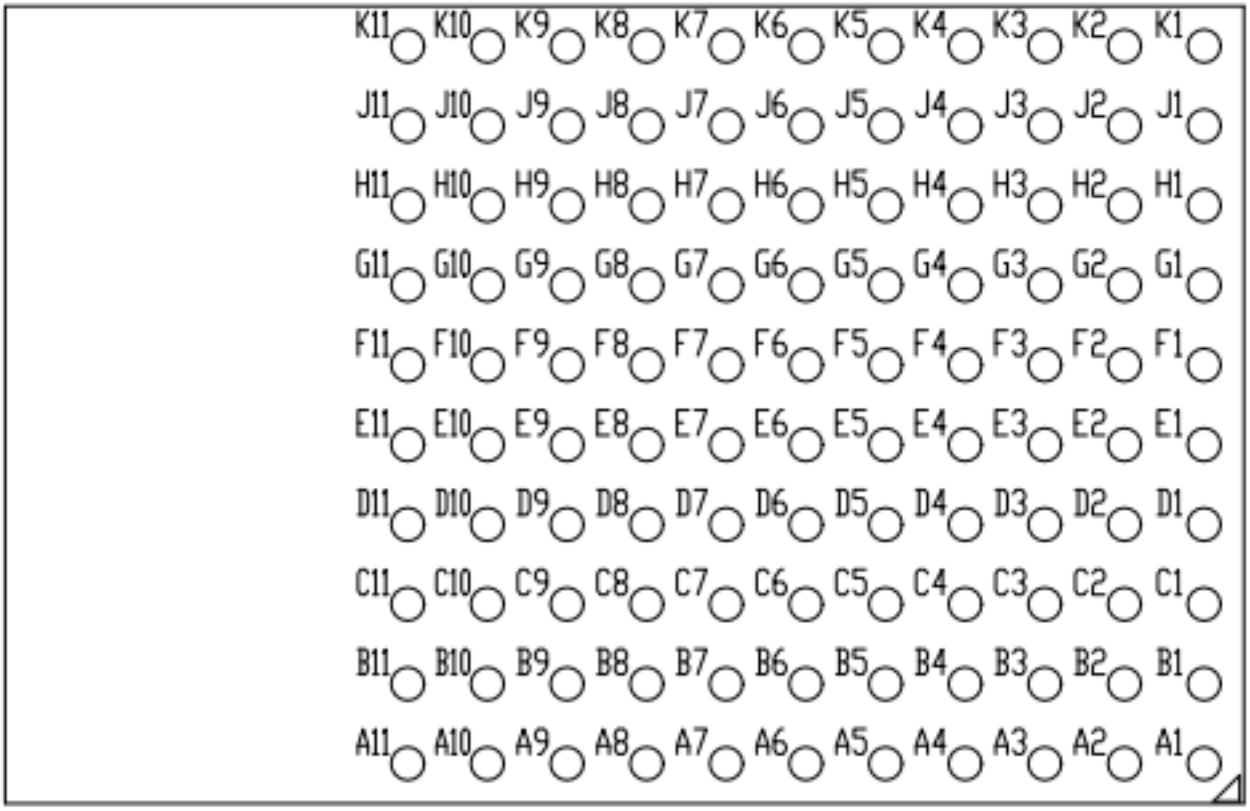
<table>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR(DH1)</td><td>-</td><td>-83</td><td>-80</td><td>dBm</td></tr>
<tr><td>EDR(2DH5)</td><td>-</td><td>-88</td><td>-85</td><td>dBm</td></tr>
<tr><td>EDR(3DH5)</td><td>-</td><td>-83</td><td>-80</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>-</td><td>-96</td><td>-93</td><td>dBm</td></tr>
</table></td></tr>
</table>

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +-5%
Operating Temperature	0 ℃ to +70 ℃
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 ℃ to +85 ℃
Storage Humidity	Less than 60% R.H.
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

2. Pin Definition

2.1 Pin Map



AW-AM510AN Pin Map (top view)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
A1	GND	Ground.		GND
A2	SDIO_DATA1	SDIO Data Line 1.	VDDIO	I/O
A3	SDIO_DATA0	SDIO Data Line 0.	VDDIO	I/O
A4	SDIO_DATA_CLK	SDIO Clock Input.	VDDIO	I
A5	SDIO_DATA_CMD	SDIO Command Input.	VDDIO	I/O
A6	SDIO_DATA3	SDIO Data Line 3.	VDDIO	I/O
A7	SDIO_DATA2	SDIO Data Line 2.	VDDIO	I/O
A8	WL_HOST_WAKE	GPIO Mode : GPIO[1]. WL Host Wake	VDDIO	I/O
A9	PDn	Power up/ down internal regulators. 0 = full power-down mode 1 = normal mode Default pull high in module internal	3.3V	I
A10	VBAT	3.3V power pin	3.3V	VCC
A11	VBAT	3.3V power pin	3.3V	VCC
B1	NC22	Floating Pin, No connect to anything		Floating
B2	NC22	Floating Pin, No connect to anything		Floating
B3	GND	Ground.		GND
B4	GND	Ground.		GND
B5	GND	Ground.		GND
B6	GND	Ground.		GND
B7	GND	Ground.		GND
B8	GND	Ground.		GND
B9	NC8	Floating Pin, No connect to anything		Floating
B10	GND	Ground.		GND
B11	GND	Ground.		GND

C1	NC23	Floating Pin, No connect to anything		Floating
C2	NC23	Floating Pin, No connect to anything		Floating
C3	GND	Ground.		GND
C4	GND	Ground.		GND
C5	GND	Ground.		GND
C6	GND	Ground.		GND
C7	GND	Ground.		GND
C8	GND	Ground.		GND
C9	GND	Ground.		GND
C10	GND	Ground.		GND
C11	GND	Ground.		GND
D1	GND	Ground.		GND
D2	GND	Ground.		GND
D3	GND	Ground.		GND
D4	GND	Ground.		GND
D5	GND	Ground.		GND
D6	GND	Ground.		GND
D7	GND	Ground.		GND
D8	GND	Ground.		GND
D9	GND	Ground.		GND
D10	GND	Ground.		GND
D11	GND	Ground.		GND
E1	SUSCLK_IN	External Low Power Clock input(32.768KHz) (optional)	1.8V	I
E2	GND	Ground.		GND
E3	GND	Ground.		GND

E4	GND	Ground.		GND
E5	GND	Ground.		GND
E6	GND	Ground.		GND
E7	GND	Ground.		GND
E8	GND	Ground.		GND
E9	GND	Ground.		GND
E10	GND	Ground.		GND
E11	GND	Ground.		GND
F1	BT_PCM_OUT	PCM data out/ GPIO[4]	VDDIO	I/O
F2	JTAG_TDO	GPIO3/TDO	VDDIO	I/O
F3	GND	Ground.		GND
F4	GND	Ground.		GND
F5	GND	Ground.		GND
F6	GND	Ground.		GND
F7	GND	Ground.		GND
F8	GND	Ground.		GND
F9	GND	Ground.		GND
F10	GND	Ground.		GND
F11	GND	Ground.		GND
G1	PCM_CLK	GPIO6	VDDIO	I/O
G2	GPIO[2] /JTAG_TDI	GPIO2/TDI	VDDIO	I/O
G3	GND	Ground.		GND
G4	GND	Ground.		GND
G5	GND	Ground.		GND
G6	GND	Ground.		GND

G7	GND	Ground.		GND
G8	GND	Ground.		GND
G9	GND	Ground.		GND
G10	GND	Ground.		GND
G11	GND	Ground.		GND
H1	BT_PCM_IN	GPIO5	VDDIO	I/O
H2	GND	Ground.		GND
H3	GND	Ground.		GND
H4	GND	Ground.		GND
H5	GND	Ground.		GND
H6	GND	Ground.		GND
H7	GND	Ground.		GND
H8	GND	Ground.		GND
H9	GND	Ground.		GND
H10	GND	Ground.		GND
H11	GND	Ground.		GND
J1	PCM_SYNC	GPIO7	VDDIO	I/O
J2	GND	Ground.		GND
J3	MWS_SIN	WCI-2 MWS coexistence serial transport interface(RX)	1.8V	I
J4	MWS_SOUT	WCI-2 MWS coexistence serial transport interface(TX)	1.8V	O
J5	WLAN WAKE	Independent software reset for Wi-Fi / GPIO[14]	VDDIO	I/O
J6	NC	Floating Pin, No connect to anything		Floating
J7	NC	Floating Pin, No connect to anything		Floating
J8	NC	Floating Pin, No connect to anything		Floating
J9	BT_WAKE_HOST	Bluetooth device to wake-up Host/GPIO0	VDDIO	I/O

J10	GND	Ground.		GND
J11	GND	Ground.		GND
K1	GND	Ground.		GND
K2	VDDIO	1.8V/3.3V VDDIO supply for WLAN and Bluetooth	1.8V/3.3V	VCC
K3	BT_DIS	Independent software reset for Bluetooth / GPIO[15]	VDDIO	I/O
K4	HOST_WAKE_BT	Host wake-up Bluetooth device/GPIO12	VDDIO	I/O
K5	GPIO[13]	GPIO Mode : GPIO[13]. Host-to-WLAN wake-up	VDDIO	I/O
K6	UART_RTS_N	High-Speed UART RTS	VDDIO	O
K7	UART_TXD	High-Speed UART Data Out	VDDIO	O
K8	UART_RXD	High-Speed UART Data In	VDDIO	I
K9	UART_CTS_N	High-Speed UART CTS	VDDIO	I
K10	GND	Ground.		GND
K11	GND	Ground.		GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	-	3.3	3.96	V
VDDIO	I/O power supply	-	3.3	4.0	V
		-	1.8	2.2	

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the 3.3V input	3.14	3.3	3.46	V
VDDIO	1.8V/3.3V digital I/O power supply	2.97	3.3	3.47	V
		1.62	1.8	1.98	

3.3 Digital IO Pin DC Characteristics

3.3.1 1.8V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output high voltage	VIO-0.4	-	-	
V_{OL}	Output low voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.3.2 3.3V Operation (VDDIO)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	0.7*VIO	-	VIO+0.4	V
V_{IL}	Input low voltage	-0.4	-	0.3*VIO	
V_{OH}	Output High Voltage	VIO-0.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
V_{HYS}	Input Hysteresis	100			mV

3.4 Host Interface

3.4.1 SDIO Interface

The AW-AM510AN supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-AM510AN acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

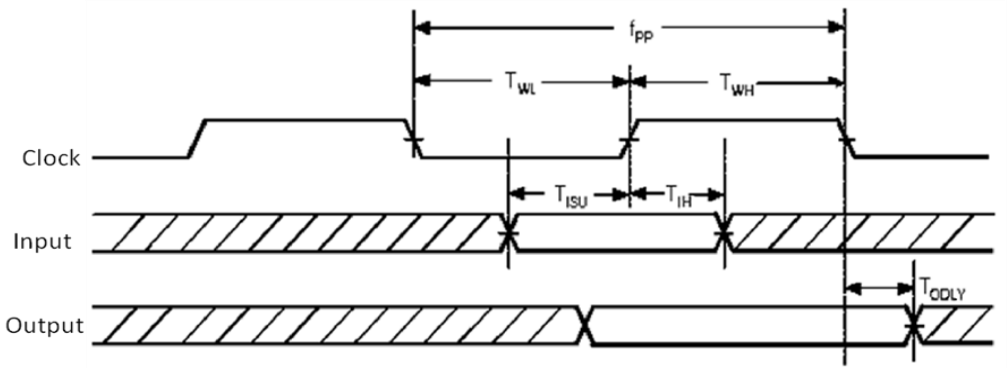
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

SDIO Interface Signals

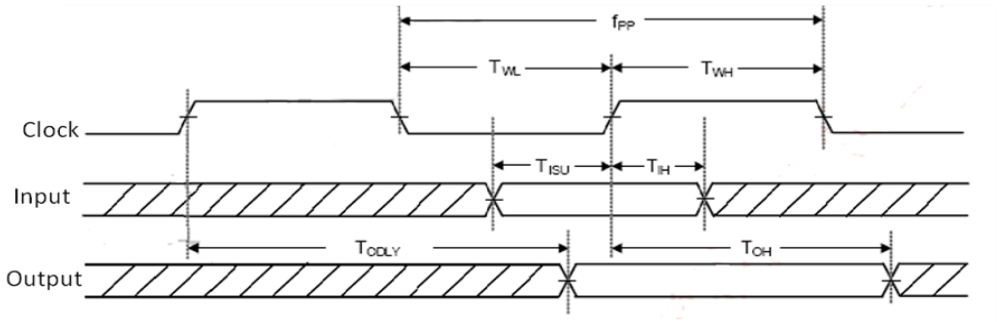
AW-AM510AN SDIO Pin Name	Type	Description
SDIO_CLK	I	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
SDIO_CMD	I/O	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
SDIO_DATA3	I/O	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
SDIO_DATA2	I/O	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
SDIO_DATA1	I/O	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
SDIO_DATA0	I/O	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line

3.4.2 SDIO Protocol Timing

3.4.2.1 Default Speed, High-Speed Modes (3.3V)



SDIO protocol timing Diagram - Default mode. (3.3V)

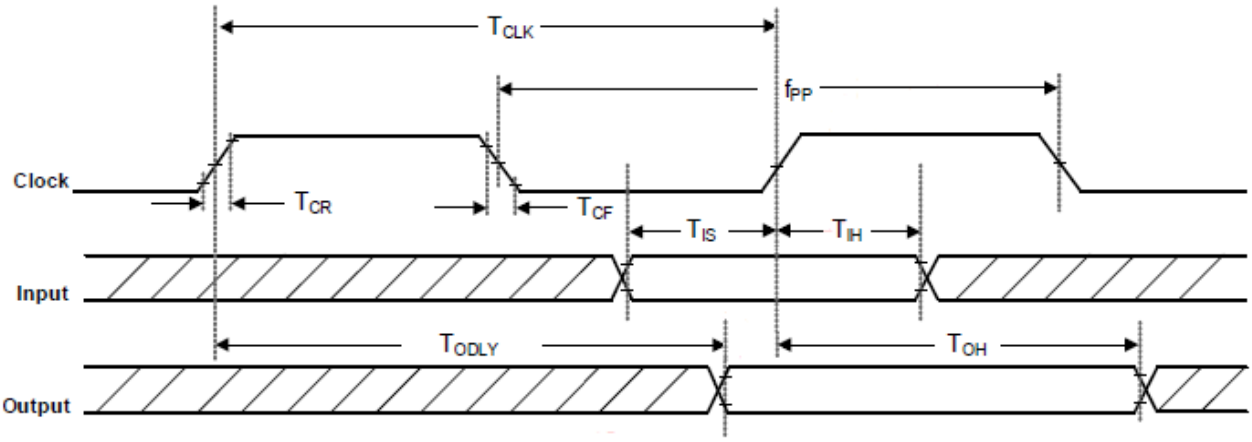


SDIO protocol timing Diagram - High Speed mode. (3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
fpp	CLK Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WH}	CLK High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WL}	CLK Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time	Normal	--	--	14	ns
	CL ≦ 40pF (1 card)	High Speed	--	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

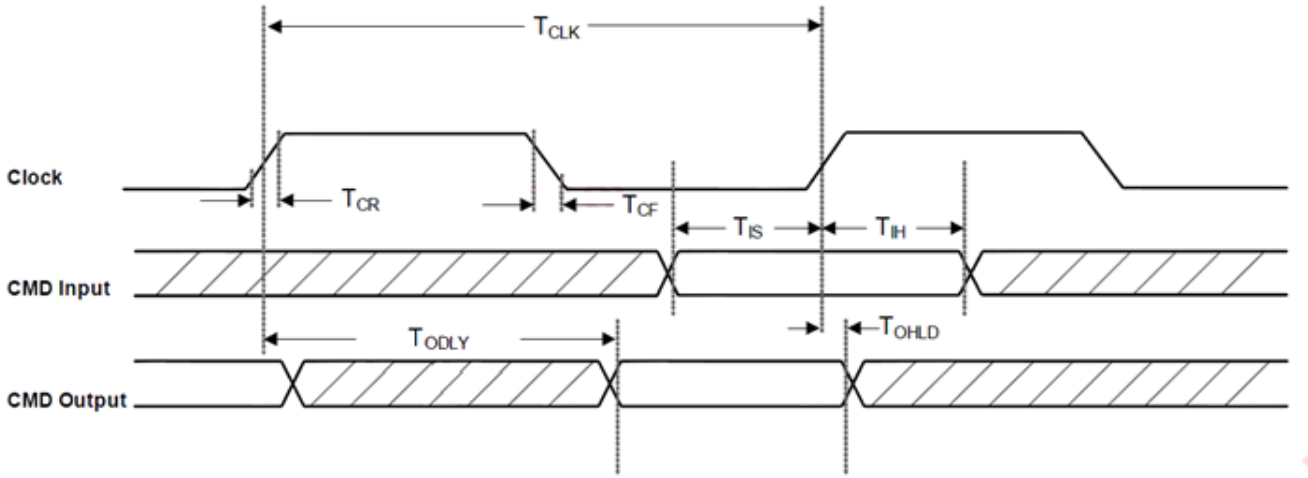


SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

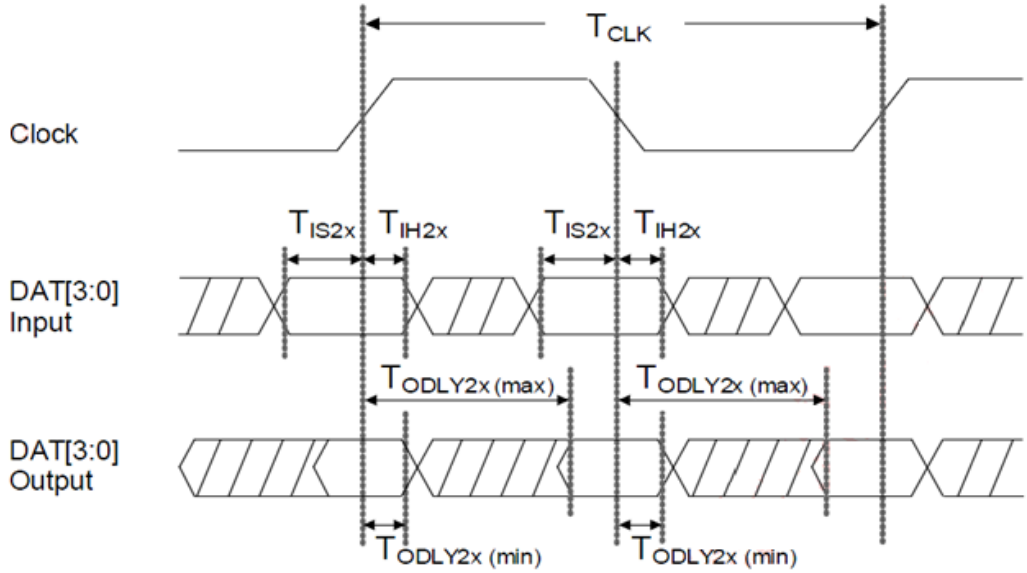
Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{pp}	CLK Frequency	SDR12/25/50	25	-	100	MHz
T_{CLK}	Clock Time	SDR12/25/50	10	-	40	ns
T_{IS}	Input Setup Time	SDR12/25/50	3	-	-	ns
T_{IH}	Input Hold Time	SDR12/25/50	0.8	-	-	ns
T_{CR} ,T_{CF}	Rise time, fail time TCR ,TCF <2ns(max) at 100MHz CCARD =10pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output Delay Time CL ≦ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output Hold Time CL =15pF	SDR12/25/50	1.5	-	-	ns

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

3.4.2.3 DDR50 Mode (50MHz) (1.8V)



SDIO CMD Timing Diagram - DDR50 Mode (50 MHz)



SDIO DAT[3:0] Timing Diagram - DDR50 Mode[1] (50 MHz)

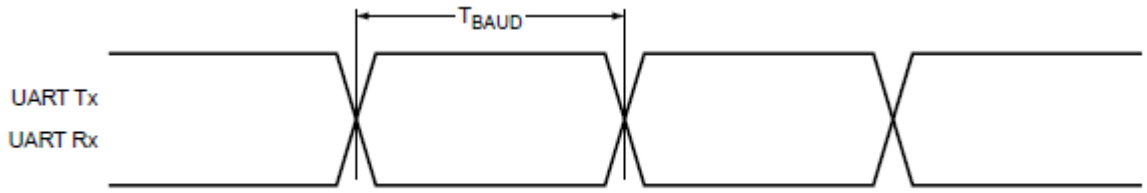
[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time	DDR50	20	-	-	ns
T_{CR}, T_{CF}	Rise time, fall time	DDR50	-	-	0.2*T_{CLK}	Ns
Clock Duty		DDR50	45	-	55	%
CMD Input						
T_{IS}	Input setup time	DDR50	6	-	-	ns
T_{IH}	Input hold time	DDR50	0.8	-	-	ns
CMD Output						
T_{ODLY}	Output delay time during data transfer mode	DDR50	-	-	13.7	ns
T_{OHLD}	Output hold time	DDR50	1.5	-	-	ns
DAT [3:0] Input						
T_{IS2X}	Input setup time	DDR50	3	-	-	ns
T_{IH2X}	Input hold time	DDR50	0.8	-	-	ns
DAT [3:0] Output						
$T_{ODLY2X(max)}$	Output delay time during data transfer mode	DDR50	-	-	7	ns
$T_{ODLY2X(min)}$	Output hold time	DDR50	1.5	-	-	ns

SDIO Timing Data - DDR50 Mode (50MHz)

3.4.3.High-Speed UART Interface

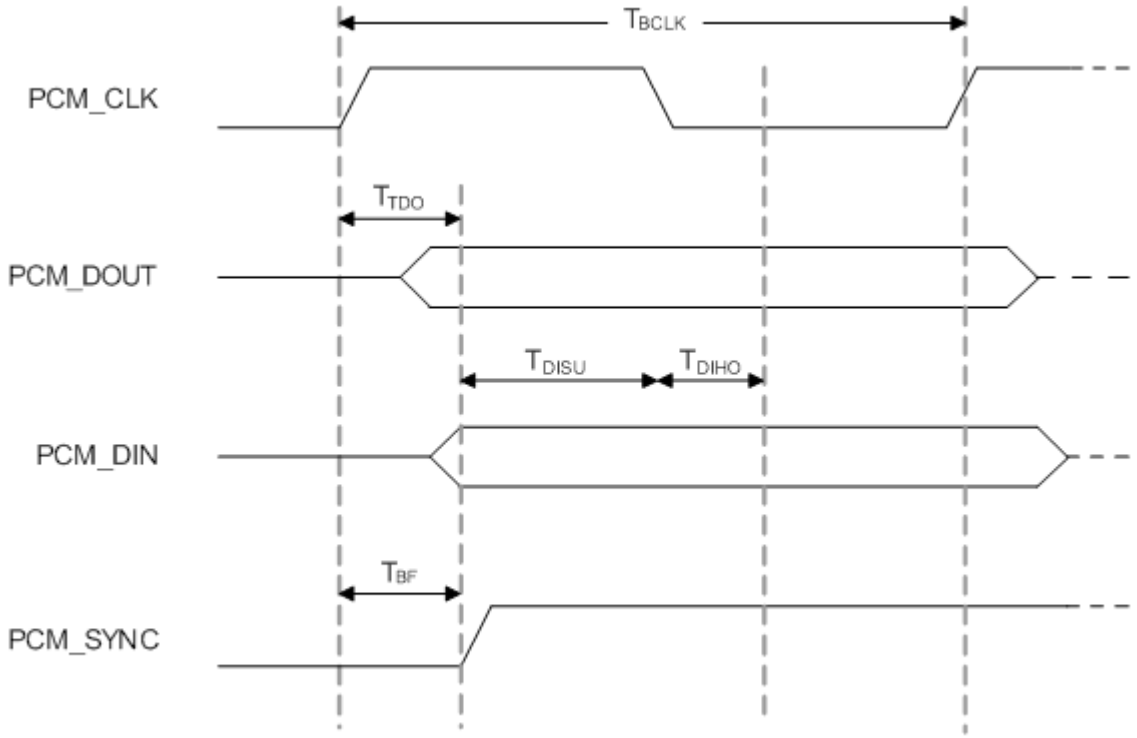
The AW-AM510AN supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.



Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	26MHz or 40MHz input clock	250	-	-	ns

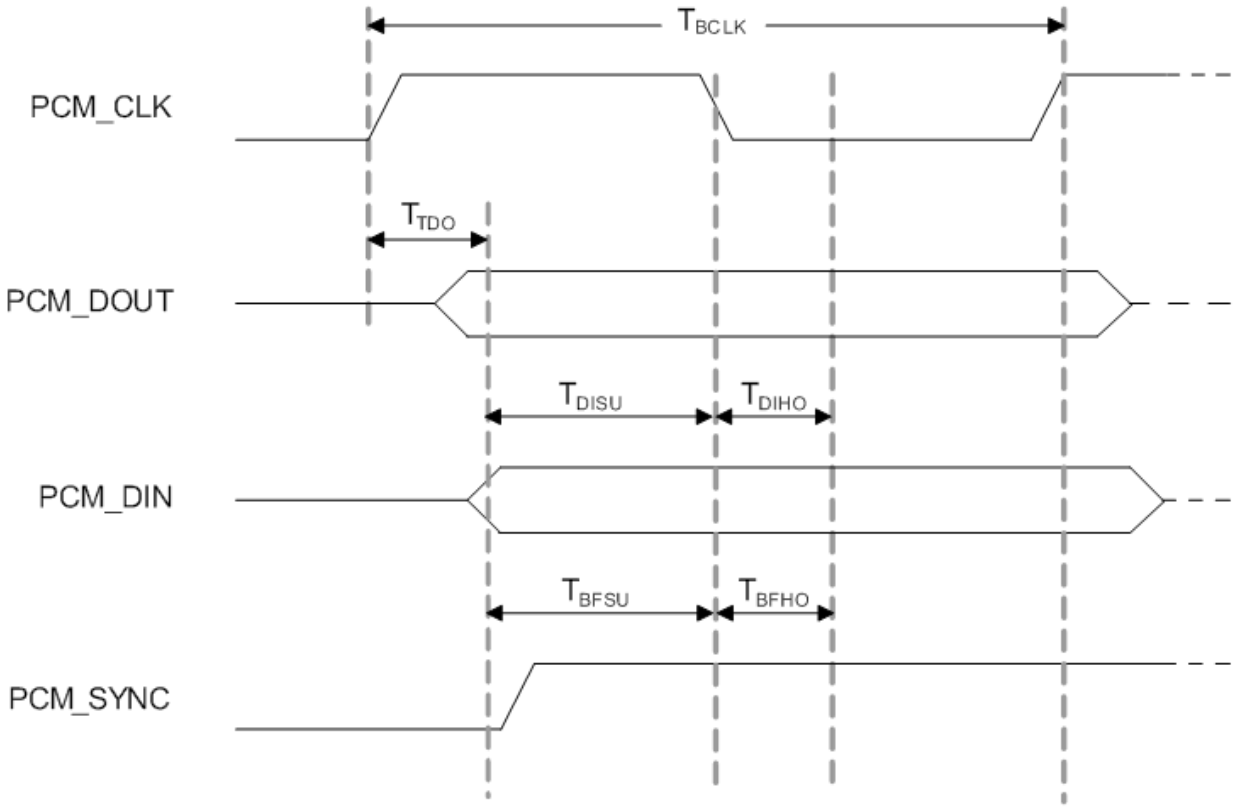
3.4.4 PCM Interface

3.4.4.1 PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

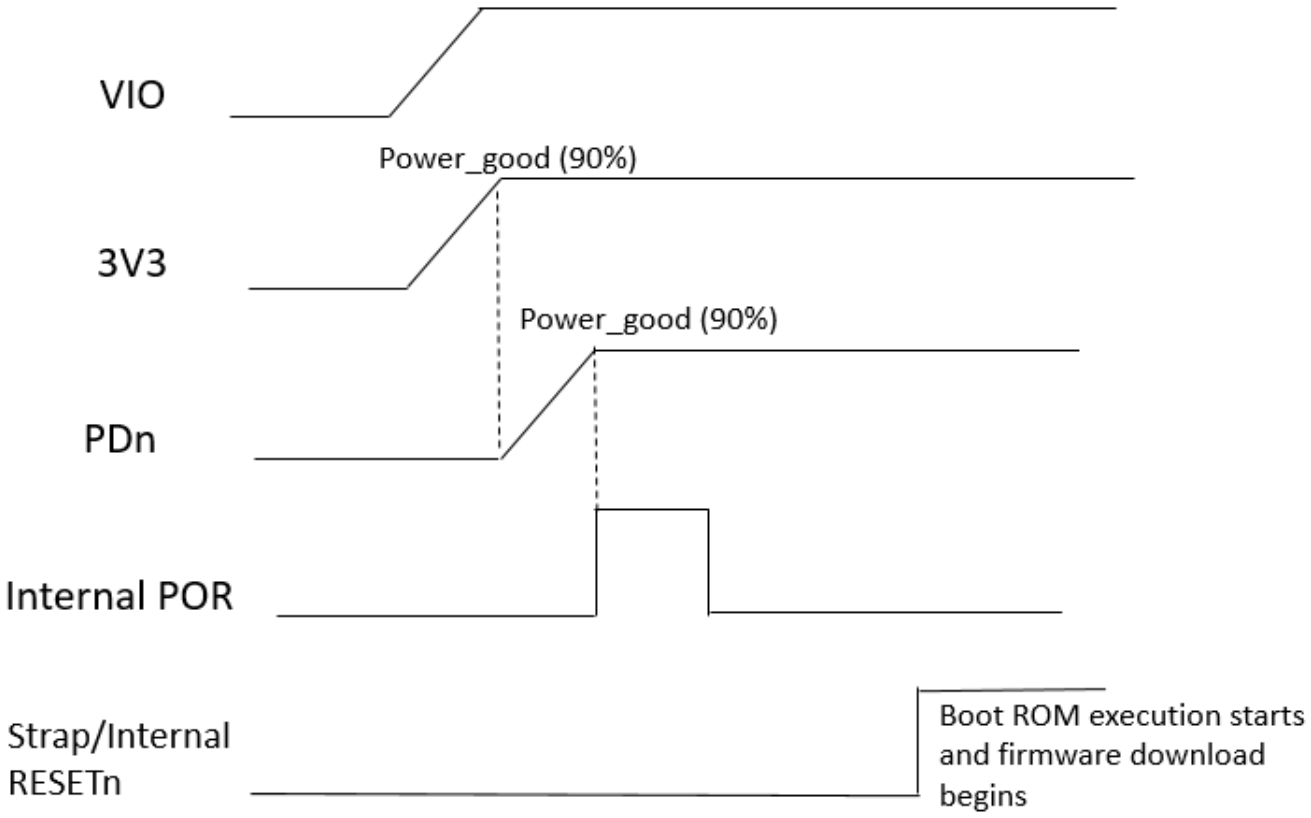
3.4.4.2 PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}			10		--	ns

3.5 Timing Sequence

AW-AM510AN power up timing sequence.



3.6 Power Consumption

TBD

3.6.1 WLAN

TBD

3.6.2 Bluetooth

TBD

3.7 Sleep Clock(Optional)

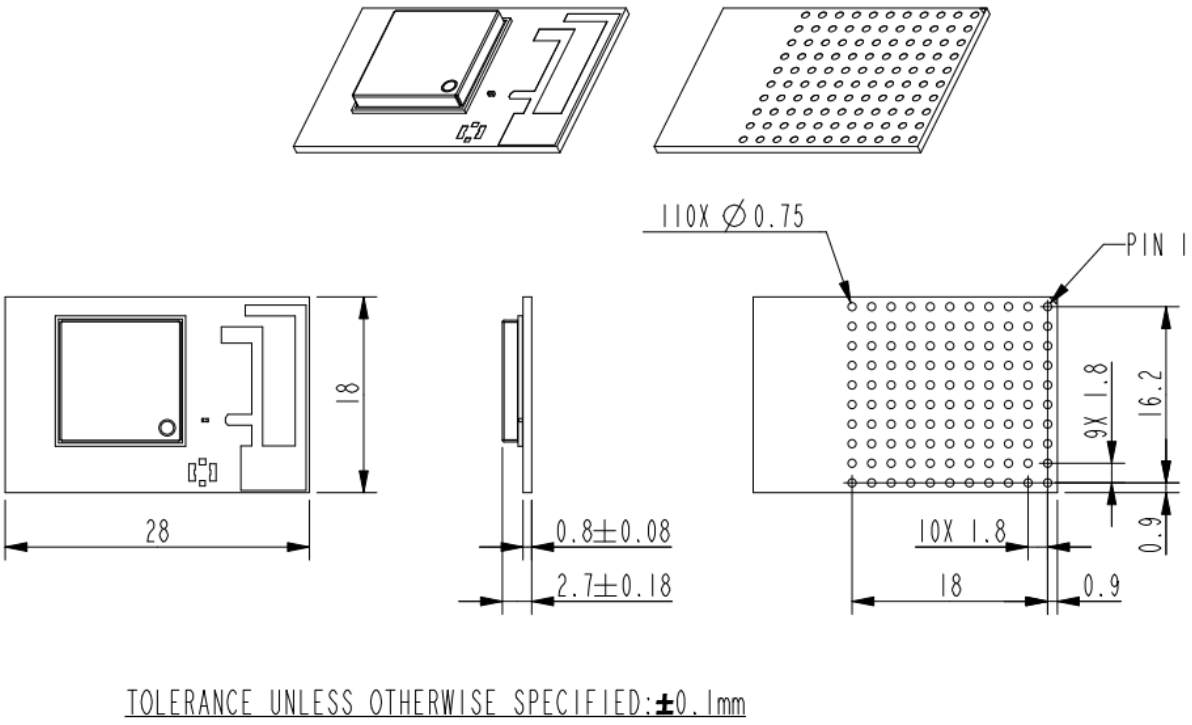
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock frequency range/ accuracy ■ CMOS input clock signal type ■ ±250 ppm (initial, aging, temperature)	-	32.768	-	kHz
PN	Phase noise requirement (@ 100KHz)	-	-125	-	dBc/Hz
J_C	Cycle jitter	-	1.5	-	ns (RMS)
SR	Slew rate limit (10-90%)	-	-	100	ns
DC	Duty cycle tolerance	20	-	80	%

4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.1mm

5. Packing Information

TBD