AzureWave Technologies, Inc.

# AW-AM281SM

## IEEE 802.11 1X1 a/b/g/n Wireless LAN + Bluetooth 5.0 Combo LGA Module

## Datasheet

**Rev. D**

**B1**

**(For Standard)**

# Features

## WLAN

- IEEE 802.11n compliant, 1x1 spatial stream with data rates up to MCS 7 (150 Mbps).
- PHY data rates up to 150 Mbps.
- Backward compatibility with legacy 802.11n/a/g/b technology.
- 20MHz bandwidth/ channel, 40MHz bandwidth/ channel, upper/ lower 20MHz packets in 40MHz channel, 20MHz duplicate legacy packets in 40MHz channel mode operation.
- Dynamic frequency selection (radar detection).
- 20/40 MHz coexistence.
- Multiple power saving modes for low power consumption.

## Bluetooth

- Baseband and radio BDR and EDR packet types – 1Mbps (GFSK), 2Mbps (π/4-DQPSK), and 3Mbps (8DPSK).
- Fully qualified Bluetooth BT4.2 (includes LE) and support Bluetooth 5.
- Enhanced Data Rate (EDR) compliant for both 2Mbps and 3Mbps supported.
- PCM/Inter-IC Sound(I2S) for Bluetooth.
- Standard Bluetooth power saving mechanisms.
- WLAN/Bluetooth Coexistence (BCA) protocol support.

# Revision History

Document NO: R2-2281SM-DST-01

| Version | Revision Date | DCN NO. | Description | Initials | Approved |
|---|---|---|---|---|---|
| A | 2019/10/22 | DCN016159 | ● Initial Version | Grace Liu | N.C Chen |
| B | 2019/12/10 | DCN016424 | ● Update minimum absolute ratings | Grace Liu | N.C Chen |
| C | 2019/12/24 | DCN016524 | ● Modify WLAN RX sensitivity specification<br>● Adjust pin number sequence | Grace Liu | N.C Chen |
| D | 2021/3/21 | DCN021137 | ● Update block diagram<br>● Modify datasheet format | Grace Liu | N.C Chen |
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AzureWave Technologies, Inc.

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# 1. Introduction

## 1.1 Product Overview

**AzureWave Technologies, Inc.** introduces the IEEE 802.11a/b/g/n WLAN, BT, combo LGA module – **AW-AM281SM.** With four advanced radio technologies integrated into a module, AW-AM281SM provides the best and most convenient SMT process. The module is targeted to mobile devices including**,** Tablet PC, Portable Media Players (PMPs), Portable Navigation Devices (PNDs), Personal Digital Assistants (PDAs), Tracking Devices, Gaming Devices which need convenient SMT process, low power consumption.

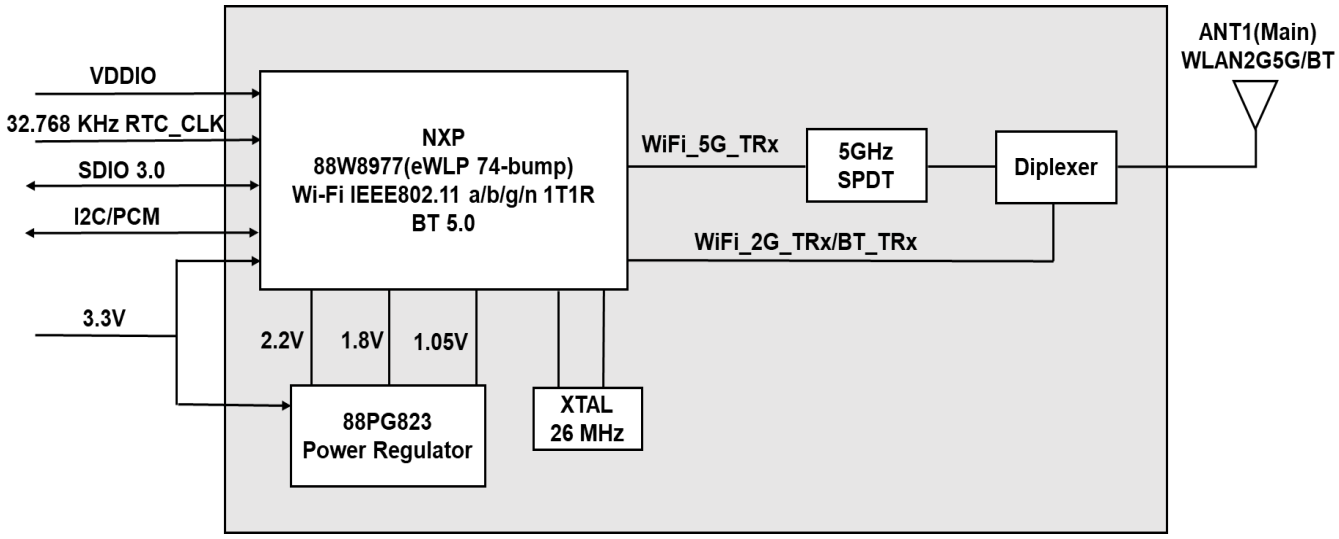
By using AW-AM281SM, the customers can easily integrate the Wi-Fi, BT, by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11a/b/g/n standard, the AW-AM281SM uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-AM281SM.

The AW-AM281SM supports standard interface **SDIO (4-bit and 1-bit)** for WLAN/BT. AW-AM281SM is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the AW-AM281SM is the best solution for the consumer electronics and the tablet PC.

## 1.2 Block Diagram

A simplified block diagram of the AW-AM281SM module is depicted in the figure below.




**AW-AM281SM Block Diagram**

## 1.3 Specifications Table

### 1.3.1 General

| Features | Description |
|---|---|
| **Product Description** | IEEE 802.11 1T1R a/b/g/n Wireless LAN<br>+ Bluetooth 5.0 Combo LGA Module |
| **Major Chipset** | Marvell 88W8977(eWLP 74-bump) |
| **Host Interface** | WiFi + BT<br>SDIO +SDIO |
| **Dimension** | 12 mm X 12 mm x 1.7 mm(Max) |
| **Form factor** | LGA module 44 pins |
| **Antenna** | 1T1R for WiFi/BT<br>ANT1(Main)：WiFi 2G5G/Bluetooth → TX/RX |
| **Weight** | 0.5g |

### 1.3.2 WLAN

| Features | Description |
|---|---|
| **WLAN Standard** | IEEE802.11 a/b/g/n 1T1R |
| **WLAN VID/PID** | N/A |
| **WLAN SVID/SPID** | N/A |
| **Frequency Rage** | 2.4 GHz ISM Bands 2.412-2.472 GHz<br>5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe<br>5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe<br>5.47-5.725 GHz for Europe<br>5.725-5.825 GHz (FCC UNII-high band) for US/Canada |
| **Modulation** | DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM |
| **Number of Channels** | 2.4GHz:<br>■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11<br>■ China, Australia, Most European Countries - 1 ~ 13<br>■ Japan, 1 ~ 13<br><br>5GHz:<br>■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165 |

<table>
<tr><td></td><td>■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140<br>■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power<br>(Board Level Limit)*</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)<br>@EVM<35%</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)<br>@EVM≦ -27 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)<br>@EVM≦ -28 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)<br>@EVM≦ -28 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)<br>@EVM≦ -27 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)<br>@EVM≦ -28 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)<br>@EVM≦ -28 dB</td><td>8</td><td>10</td><td>12</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-87</td><td>-84</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-73</td><td>-71</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-69</td><td>-66</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-67</td><td>-64</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-67</td><td>-64</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-63</td><td>-60</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Data Rate</td><td>WLAN:<br>802.11b : 1, 2, 5.5, 11Mbps<br>802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps<br>802.11n : Maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)</td></tr>
<tr><td>Security</td><td>■ WAPI<br>■ WEP 64-bit and 128-bit encryption with H/W TKIP processing<br>■ WPA/WPA2 (Wi-Fi Protected Access)<br>■ AES-CCMP hardware implementation as part of 802.11i security standard</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

### 1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 4.2 (includes LE)+EDR<br>Bluetooth 5</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK<br>Payload 2M: π/4-DQPSK<br>Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>-4</td><td>-1</td><td>1</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR(DH1)</td><td>-</td><td>-90</td><td>-80</td><td>dBm</td></tr>
<tr><td>EDR(2DH5)</td><td>-</td><td>-92</td><td>-80</td><td>dBm</td></tr>
<tr><td>EDR(3DH5)</td><td>-</td><td>-88</td><td>-70</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>-</td><td>-92</td><td>-85</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

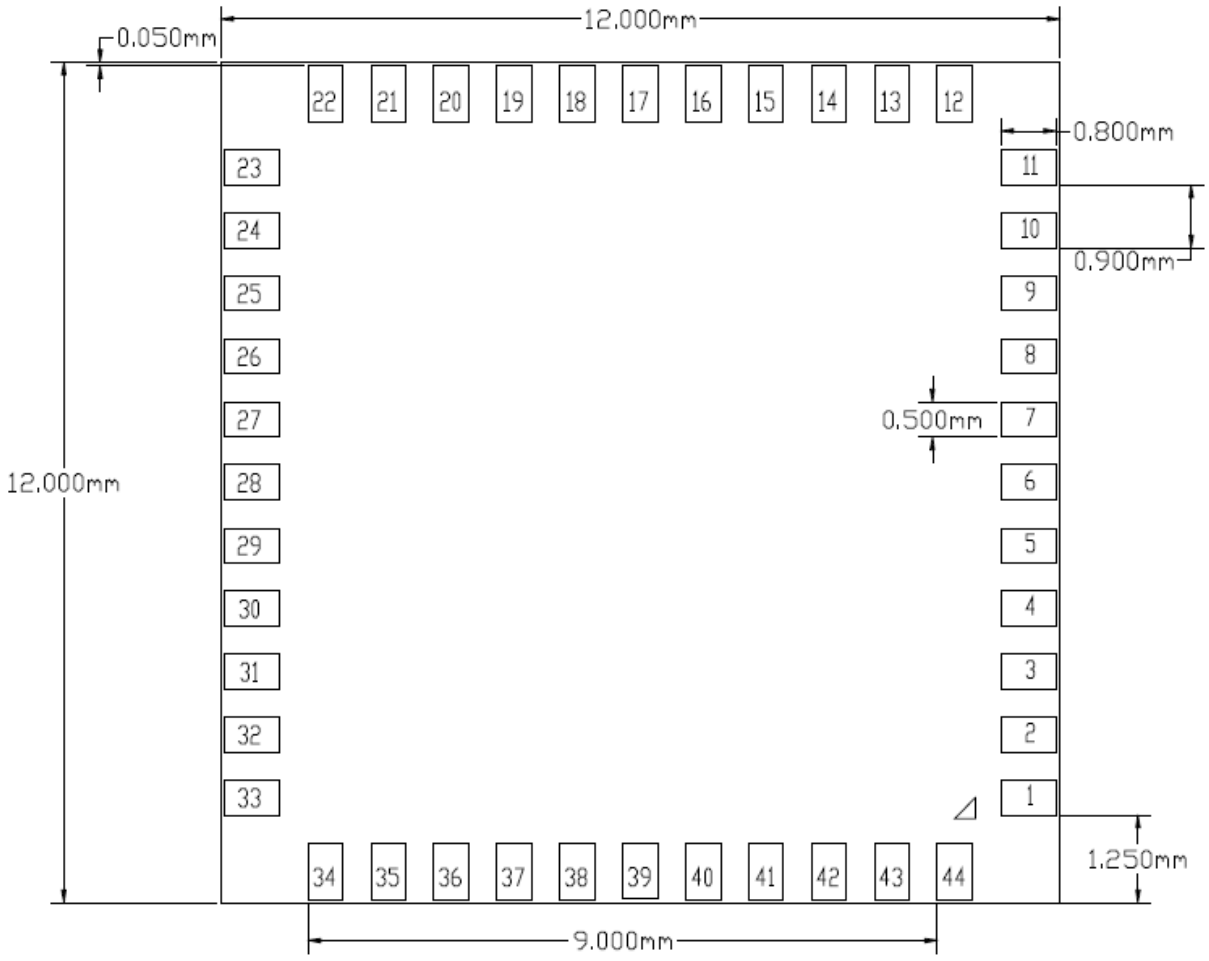
### 1.3.4 Operating Conditions

| Features | Description |
|---|---|
| **Operating Conditions** | |
| **Voltage** | 3.3V |
| **Operating Temperature** | -20 ºC to +85 ºC |
| **Operating Humidity** | Less than 85%R.H. |
| **Storage Temperature** | -40 ºC to +85 ºC |
| **Storage Humidity** | Less than 60%R.H. |
| **ESD Protection** | |
| **Human Body Model** | ±2KV (MIL-STD-883H Method 3015.8) |
| **Changed Device Model** | ±500V (JEDEC EIA/JESD22-C101E) |

# 2. Pin Definition

## 2.1 Pin Map

AW-AM281SM pin out drawing (top view).



## 2.2 Pin Table

| Pin No | Definition | Basic Description | Voltage | Type |
|---|---|---|---|---|
| **1** | GND1 | Ground | --- | --- |
| **2** | WL_BT_ANT | Option for RF I/O pin out | 1.8V | I/O |
| **3** | GND3 | Ground | --- | --- |
| **4** | NC4 | Floating Pin, No connect to anything. | --- | Floating |
| **5** | NC5 | Floating Pin, No connect to anything. | --- | Floating |
| **6** | BT_HOST_WAKE_DEV | BT Device Wake | VDDIO | I |
| **7** | BT_DEV_WAKE_Host | BT Host Wake | VDDIO | O |
| **8** | NC8 | Floating Pin, No connect to anything. | --- | Floating |
| **9** | VDD33 | 3.3V power voltage source input | 3.3V | P |
| **10** | NC10 | Floating Pin, No connect to anything. | --- | Floating |
| **11** | NC11 | Floating Pin, No connect to anything. | --- | Floating |
| **12** | WL_DIS# | WiFi reset pin | VDDIO | I |
| **13** | WL_DEV_WAKE_HOST | WL Host Wake | VDDIO | I/O |
| **14** | SDIO_DATA_2 | SDIO Data line Bit[2] | VDDIO | I/O |
| **15** | SDIO_DATA_3 | SDIO Data line Bit[3] | VDDIO | I/O |
| **16** | SDIO_DATA_CMD | SDIO Command | VDDIO | I/O |
| **17** | SDIO_DATA_CLK | SDIO Clock input | VDDIO | I |
| **18** | SDIO_DATA_0 | SDIO Data line Bit[0] | VDDIO | I/O |
| **19** | SDIO_DATA_1 | SDIO Data line Bit[1] | VDDIO | I/O |
| **20** | GND20 | Ground | --- | --- |
| **21** | NC21 | Floating Pin, No connect to anything. | --- | Floating |
| **22** | VDDIO | 1.8V/3.3V Digital I/O Power Supply | 1.8V/3.3V | P |
| **23** | NC23 | Floating Pin, No connect to anything. | --- | Floating |

| | | | | |
|---|---|---|---|---|
| **24** | SLP_CLK | External Low Power Clock input (32.768KHz) | VDDIO | I |
| **25** | PCM_OUT | PCM Data output | VDDIO | I/O |
| **26** | PCM_CLK | PCM Clock | VDDIO | I/O |
| **27** | PCM_IN | PCM data input | VDDIO | I/O |
| **28** | PCM_SYNC | PCM sync signal | VDDIO | I/O |
| **29** | NC29 | Floating Pin, No connect to anything. | --- | Floating |
| **30** | NC30 | Floating Pin, No connect to anything. | --- | Floating |
| **31** | GND31 | Ground | --- | --- |
| **32** | NC32 | Floating Pin, No connect to anything. | --- | Floating |
| **33** | GND33 | Ground | --- | --- |
| **34** | BT_DIS# | BT reset pin | VDDIO | I |
| **35** | NC35 | Floating Pin, No connect to anything. | --- | Floating |
| **36** | GND36 | Ground | --- | --- |
| **37** | NC37 | Floating Pin, No connect to anything. | --- | Floating |
| **38** | NC38 | Floating Pin, No connect to anything. | --- | Floating |
| **39** | GPIO8 | GPIO Mode : GPIO[8].<br>Bluetooth External Coexistence Mode : BT_FREQ. | VDDIO | I/O |
| **40** | GPIO9 | GPIO Mode : GPIO[9].<br>Bluetooth External Coexistence Mode : BT_STATE. | VDDIO | I/O |
| **41** | NC41 | Floating Pin, No connect to anything. | --- | Floating |
| **42** | NC42 | Floating Pin, No connect to anything. | --- | Floating |
| **43** | NC43 | Floating Pin, No connect to anything. | --- | Floating |
| **44** | NC44 | Floating Pin, No connect to anything. | --- | Floating |

# 3. Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **3.3V** | DC supply for the 3.3V input | -0.3 | 3.3 | 4.0 | V |
| **VDDIO** | Host I/O power supply | -0.3 | 3.3 | 4.0 | V |
| | | -0.3 | 1.8 | 2.2 | |

## 3.2 Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **3.3V** | DC supply for the 3.3V input | 2.97 | 3.3 | 3.63 | V |
| **VDDIO** | 1.8V/3.3V digital I/O power supply | 2.97 | 3.3 | 3.63 | V |
| | | 1.62 | 1.8 | 1.98 | |

## 3.3 Digital IO Pin DC Characteristics

### 3.3.1 1.8V Operation (VDDIO)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **$V_{IH}$** | Input high voltage | 0.7*V18 | - | V18+0.4 | V |
| **$V_{IL}$** | Input low voltage | -0.4 | - | 0.3*V18 | |
| **$V_{OH}$** | Output high voltage | V18-0.4 | - | - | |
| **$V_{OL}$** | Output low voltage | - | - | 0.4 | |

### 3.3.2 3.3V Operation (VDDIO)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **$V_{IH}$** | Input high voltage | 0.7*V33 | - | V33+0.4 | V |
| **$V_{IL}$** | Input low voltage | -0.4 | - | 0.3*V33 | V |
| **$V_{OH}$** | Output High Voltage | V33-0.4 | - | - | V |
| **$V_{OL}$** | Output Low Voltage | - | - | 0.4 | V |

## 3.4 Host Interface

### 3.4.1 SDIO Interface

The AW-AM281SM supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-AM281SM acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the frvice through the use of BARs and a DMA engine.

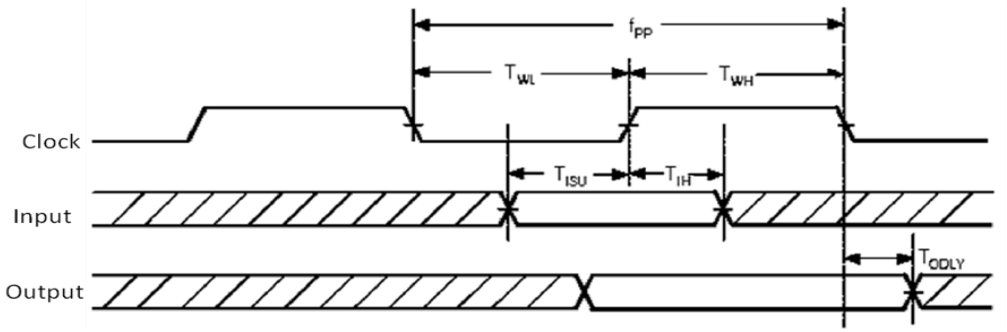
- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

**SDIO Interface Signals**

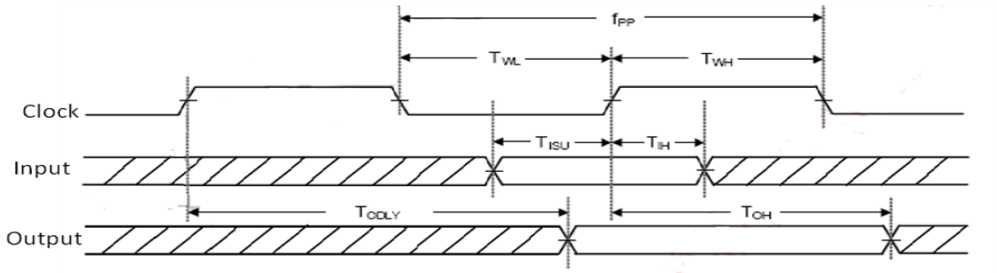
| AW-AM281SM SDIO Pin Name | Type | Description |
|---|---|---|
| **SDIO_DATA_CLK** | I | SDIO 4-bit mode: Clock<br>SDIO 1-bit mode: Clock |
| **SDIO_DATA_CMD** | I/O | SDIO 4-bit mode: Command line<br>SDIO 1-bit mode: Command line |
| **SDIO_DATA_3** | I/O | SDIO 4-bit mode: Data line Bit[3]<br>SDIO 1-bit mode: Not used |
| **SDIO_DATA_2** | I/O | SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional)<br>SDIO 1-bit mode: Read Wait (optional) |
| **SDIO_DATA_1** | I/O | SDIO 4-bit mode: Data line Bit[1]<br>SDIO 1-bit mode: Interrupt |
| **SDIO_DATA_0** | I/O | SDIO 4-bit mode: Data line Bit[0]<br>SDIO 1-bit mode: Data line |

### 3.4.2 SDIO Protocol Timing

#### 3.4.2.1 Default Speed, High-Speed Modes (3.3V)




SDIO protocol timing Diagram - Default mode. (3.3V)

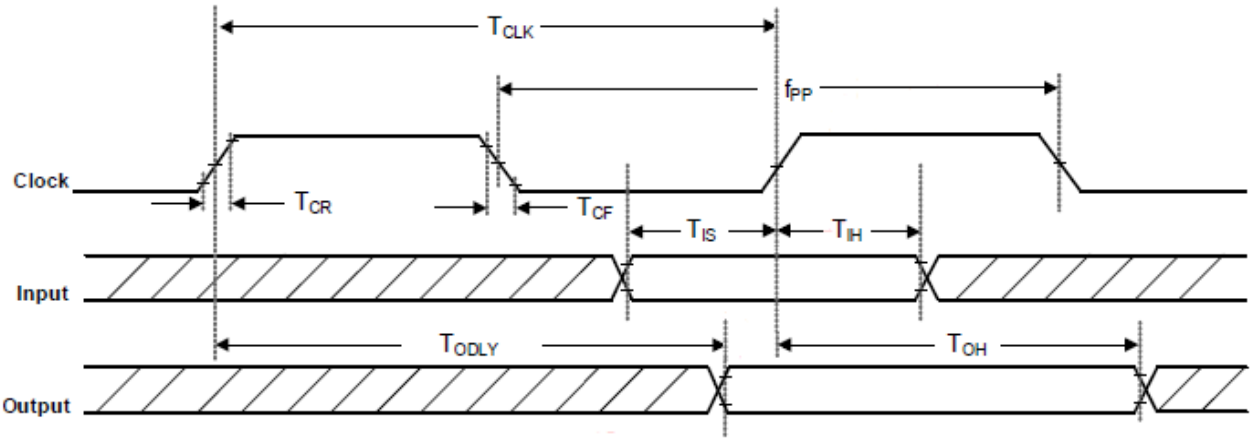



SDIO protocol timing Diagram - High Speed mode. (3.3V)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **fpp** | CLK Frequency | Normal | 0 | -- | 25 | MHz |
| | | High Speed | 0 | -- | 50 | MHz |
| **$T_{WH}$** | CLK High Time | Normal | 10 | -- | -- | ns |
| | | High Speed | 7 | -- | -- | ns |
| **$T_{WL}$** | CLK Low Time | Normal | 10 | -- | -- | ns |
| | | High Speed | 7 | -- | -- | ns |
| **$T_{ISU}$** | Input Setup Time | Normal | 5 | -- | -- | ns |
| | | High Speed | 6 | -- | -- | ns |
| **$T_{IH}$** | Input Hold Time | Normal | 5 | -- | -- | ns |
| | | High Speed | 2 | -- | -- | ns |
| **$T_{ODLY}$** | Output Delay Time | Normal | -- | -- | 14 | ns |
| | CL ≦ 40pF (1 card) | High Speed | -- | -- | 14 | ns |
| **$T_{OH}$** | Output Hold Time | High Speed | 2.5 | -- | -- | ns |

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)

### 3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

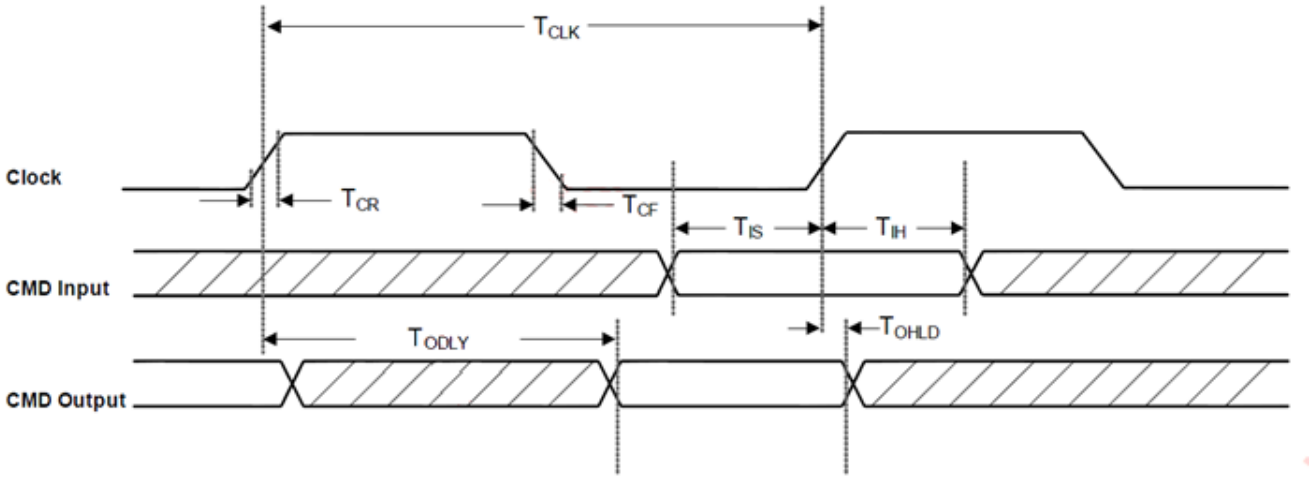



SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

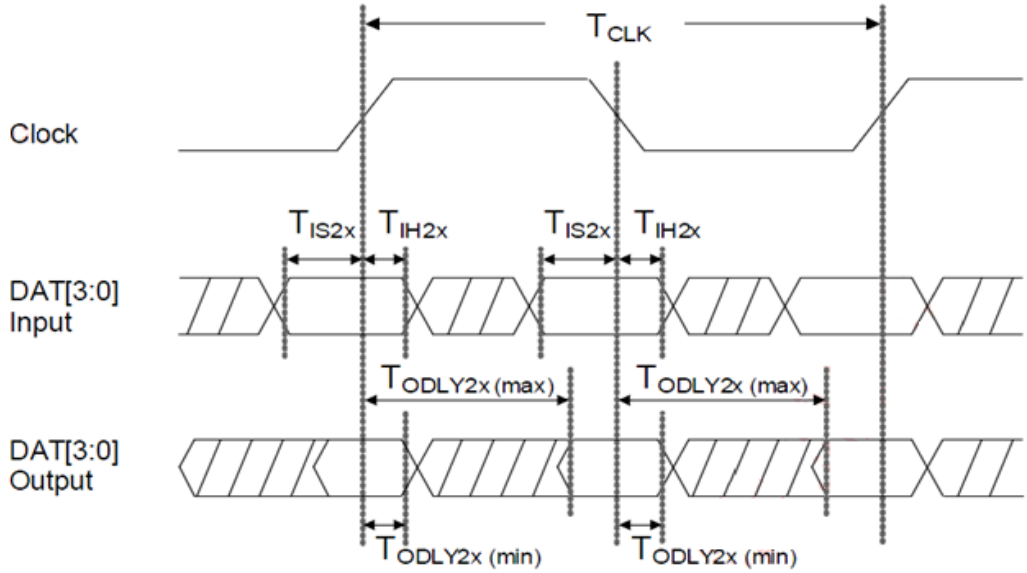
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{pp}$ | CLK Frequency | SDR12/25/50 | 25 | - | 100 | MHz |
| $T_{CLK}$ | Clock Time | SDR12/25/50 | 10 | - | 40 | ns |
| $T_{IS}$ | Input Setup Time | SDR12/25/50 | 3 | - | - | ns |
| $T_{IH}$ | Input Hold Time | SDR12/25/50 | 0.8 | - | - | ns |
| $T_{CR}$ ,$T_{CF}$ | Rise time, fail time<br>TCR ,TCF <2ns(max) at 100MHz<br>CCARD =10pF | SDR12/25/50 | - | - | 0.2*$T_{CLK}$ | ns |
| $T_{ODLY}$ | Output Delay Time<br>CL ≦ 30pF | SDR12/25/50 | - | - | 7.5 | ns |
| $T_{OH}$ | Output Hold Time<br>CL =15pF | SDR12/25/50 | 1.5 | - | - | ns |

SDIO Timing Data - SDR12/25/50 modes. (1.8V)

### 3.4.2.3 DDR50 Mode (50MHz) (1.8V)




SDIO CMD Timing Diagram - DDR50 Mode (50 MHz)




SDIO DAT[3:0] Timing Diagram - DDR50 Mode[1] (50 MHz)

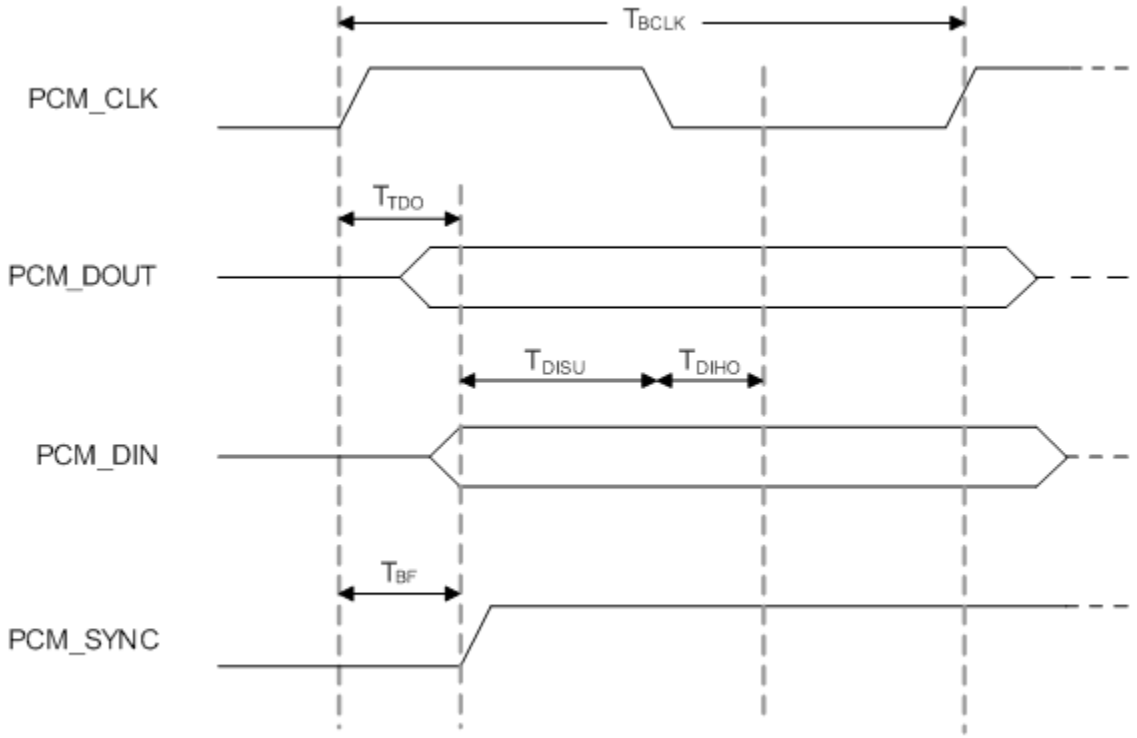
[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Clock** | | | | | | |
| **$T_{CLK}$** | Clock time | DDR50 | 20 | - | - | ns |
| **$T_{CR}$, $T_{CF}$** | Rise time, fall time | DDR50 | - | - | 0.2*$T_{CLK}$ | Ns |
| **Clock Duty** | | DDR50 | 45 | - | 55 | % |
| **CMD Input** | | | | | | |
| **$T_{IS}$** | Input setup time | DDR50 | 6 | - | - | ns |
| **$T_{IH}$** | Input hold time | DDR50 | 0.8 | - | - | ns |
| **CMD Output** | | | | | | |
| **$T_{ODLY}$** | Output delay time during data transfer mode | DDR50 | - | - | 13.7 | ns |
| **$T_{OHLD}$** | Output hold time | DDR50 | 1.5 | - | - | ns |
| **DAT [3:0] Input** | | | | | | |
| **$T_{IS2X}$** | Input hold time | DDR50 | 3 | - | - | ns |
| **$T_{IH2X}$** | Input hold time | DDR50 | 0.8 | - | - | ns |
| **DAT [3:0] Output** | | | | | | |
| **$T_{ODLY2X(max)}$** | Output delay time during data transfer mode | DDR50 | - | - | 7 | ns |
| **$T_{ODLY2X(min)}$** | Output hold time | DDR50 | 1.5 | - | - | ns |

SDIO Timing Data - DDR50 Mode (50MHz)

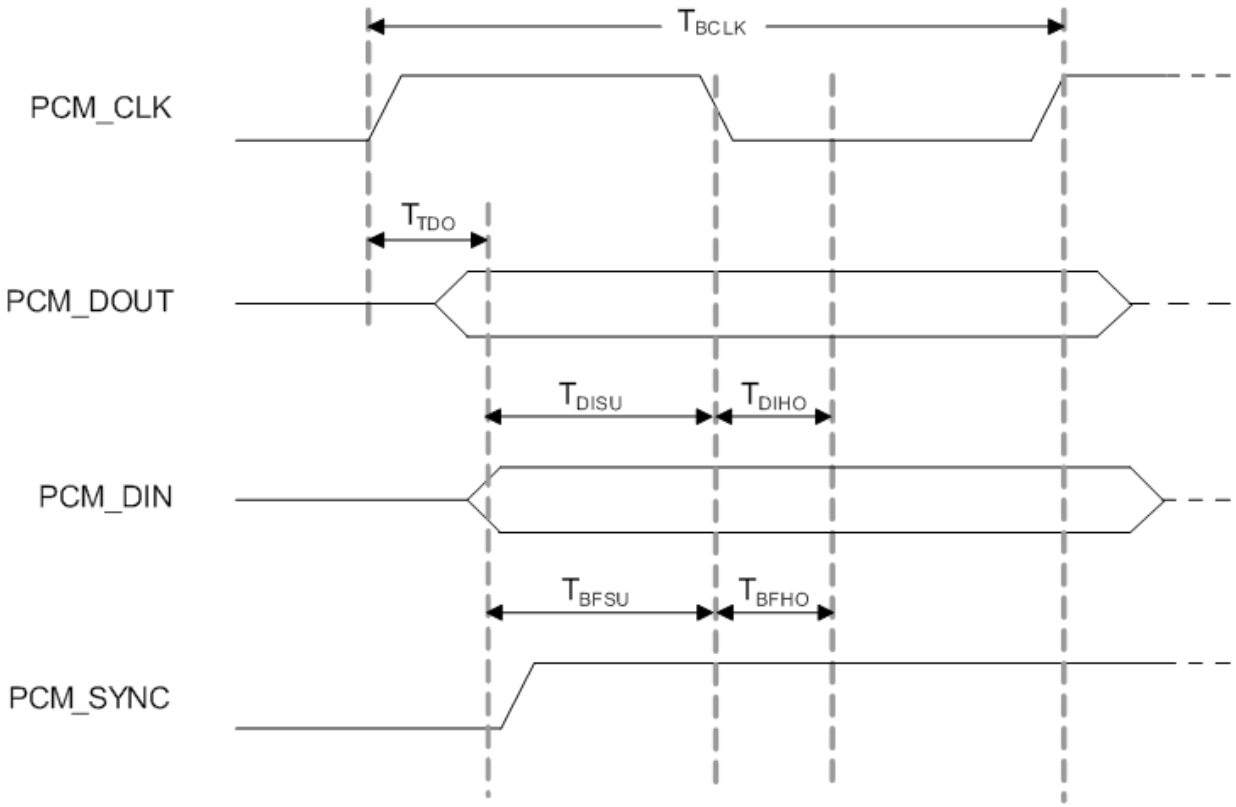
### 3.4.3 PCM Interface

#### 3.4.3.1 PCM Timing Specification – Master Mode




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **$F_{BCLK}$** | -- | -- | -- | 2/2.048 | -- | MHz |
| **Duty $Cycle_{BCLK}$** | -- | -- | 0.4 | 0.5 | 0.6 | -- |
| **$T_{BCLK\ rise/fall}$** | -- | -- | -- | 3 | -- | ns |
| **$T_{DO}$** | -- | -- | -- | -- | 15 | ns |
| **$T_{DISU}$** | -- | -- | 20 | -- | -- | ns |
| **$T_{DIHO}$** | -- | -- | 15 | -- | -- | ns |
| **$T_{BF}$** | -- | -- | -- | -- | 15 | ns |

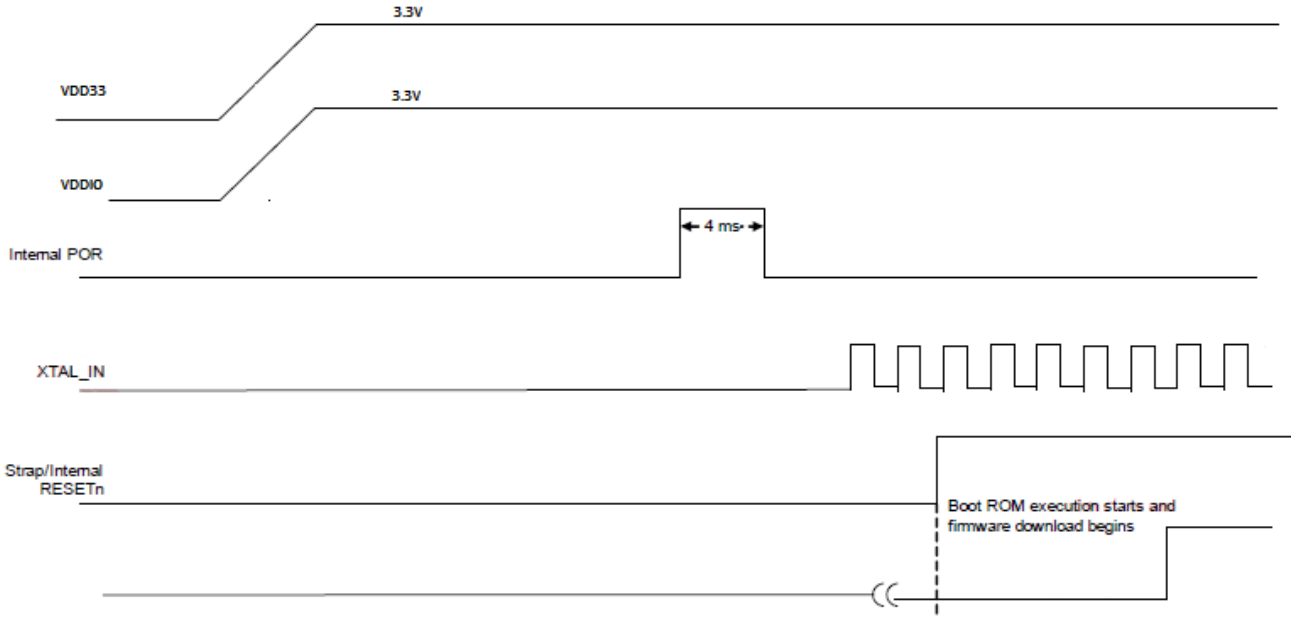
### 3.4.3.2 PCM Timing Specification – Slave Mode




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **$F_{BCLK}$** | -- | -- | -- | 2/2.048 | -- | MHz |
| **Duty $Cycle_{BCLK}$** | -- | -- | 0.4 | 0.5 | 0.6 | -- |
| **$T_{BCLK\ rise/fall}$** | -- | -- | -- | 3 | -- | ns |
| **$T_{DO}$** | -- | -- | -- | -- | 30 | ns |
| **$T_{DISU}$** | -- | -- | 15 | -- | -- | ns |
| **$T_{DIHO}$** | -- | -- | 10 | -- | -- | ns |
| **$T_{BFSU}$** | -- | -- | 15 | -- | -- | ns |
| **$T_{BFHO}$** | | | 10 | | -- | ns |

## 3.5 Timing Sequence

AW-AM281SM power up timing sequence.



## 3.6 Power Consumption*

### 3.6.1 WLAN

| | Item | | | VBAT=3.3V | | | |
|---|---|---|---|---|---|---|---|
| Band (GHz) | Mode | BW (MHz) | RF Power (dBm) | Transmit | | Receive | |
| | | | | Max. | Avg. | Max. | Avg. |
| 2.4G | 11b@1Mbps | 20 | 16 | 272.6mA | 270.3mA | 46.5mA | 38.7mA |
| | 11g@54Mbps | 20 | 14 | 203.3mA | 200.8mA | 49.1mA | 42.0mA |
| | 11n@MCS7 | 20 | 13 | 200.7mA | 198.8mA | 48.6mA | 41.6mA |
| | 11n@MCS7 | 40 | 11 | 187.3mA | 185.8mA | 55.5mA | 48.4mA |
| | 11a@54Mbps | 20 | 13 | 158.3mA | 143.5mA | 80.5mA | 70.1mA |
| | 11n@MCS7 | 20 | 12 | 260.1mA | 248.3mA | 74.6mA | 64.1mA |
| 5G | 11n@MCS7 | 40 | 10 | 239.3mA | 227.9mA | 80.2mA | 69.7mA |

* The power consumption is based on Azurewave test environment, these data for reference only.

### 3.6.2 Bluetooth

| No. | Mode | VBAT=3.3V | | | |
|---|---|---|---|---|---|
| | | Transmit | | Receive | |
| | | Max. | Avg. | Max. | Avg. |
| 1 | DH5 | 23.1mA | 22.6mA | N/A | N/A |
| 2 | 3DH5 | 29.5mA | 26.9mA | N/A | N/A |
| 3 | LE | 13.1mA | 12.4mA | 12.9mA | 10.2mA |

* The power consumption is based on Azurewave test environment, these data for reference only.

## 3.7 Sleep Clock

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

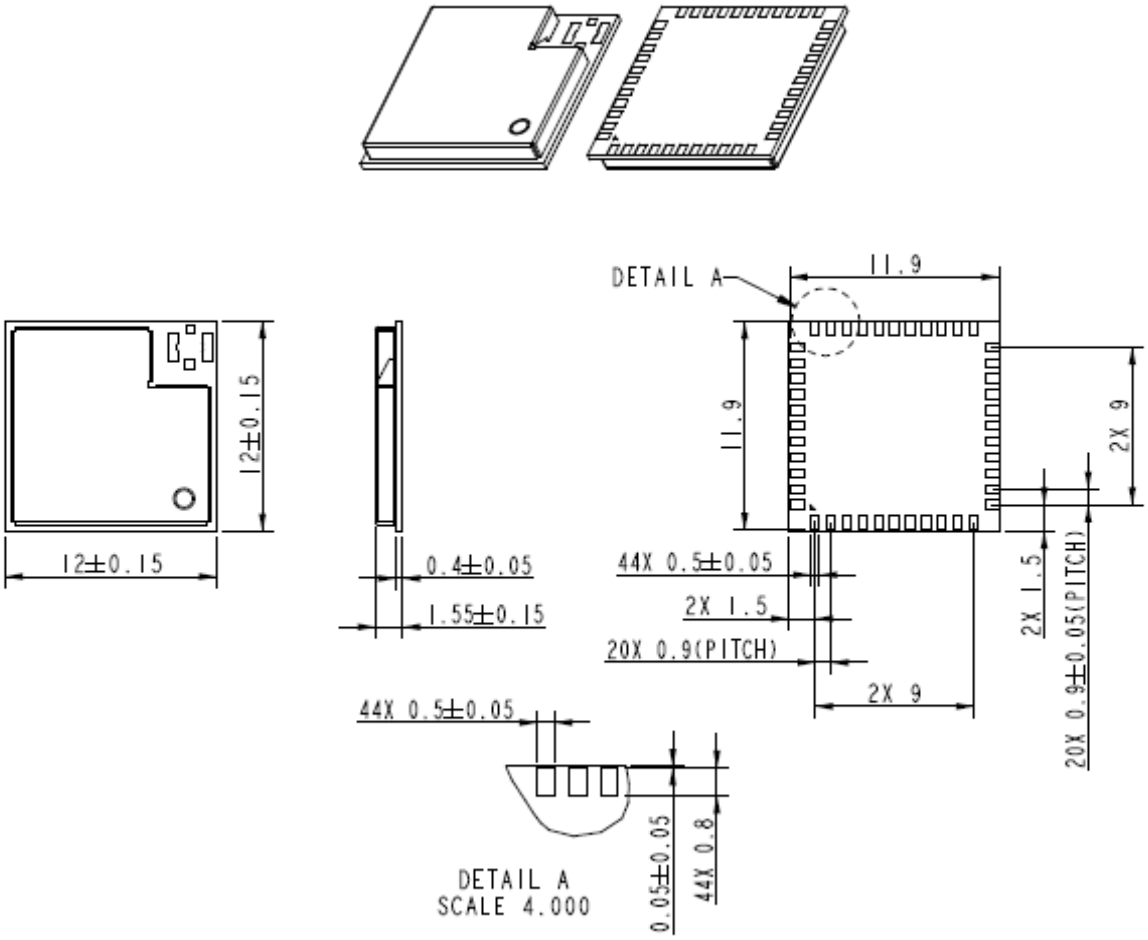
### External 32.768KHz Low-Power Oscillator

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **CLK** | Clock frequency range/ accuracy<br>■ CMOS input clock signal type<br>■ ±250 ppm (initial, aging, temperature) | - | 32.768 | - | kHz |
| **$V_{IH}$*** | Input levels, where VDDIO=1.8, 3.3V | 0.7*VDDIO | - | VDDIO+0.4 | V |
| **$V_{IL}$*** | | -0.4 | - | 0.3*VDDIO | V |
| **PN** | Phase noise requirement (@ 100KHz) | - | -125 | - | dBc/Hz |
| **$J_C$** | Cycle jitter | - | 1.5 | - | ns (RMS) |
| **SR** | Slew rate limit (10-90%) | - | - | 100 | ns |
| **DC** | Duty cycle tolerance | 20 | - | 80 | % |

*For $V_{HL}$,$V_{IL}$, see 3.3 Digital IO Pin DC Characteristics

# 4. Mechanical Information

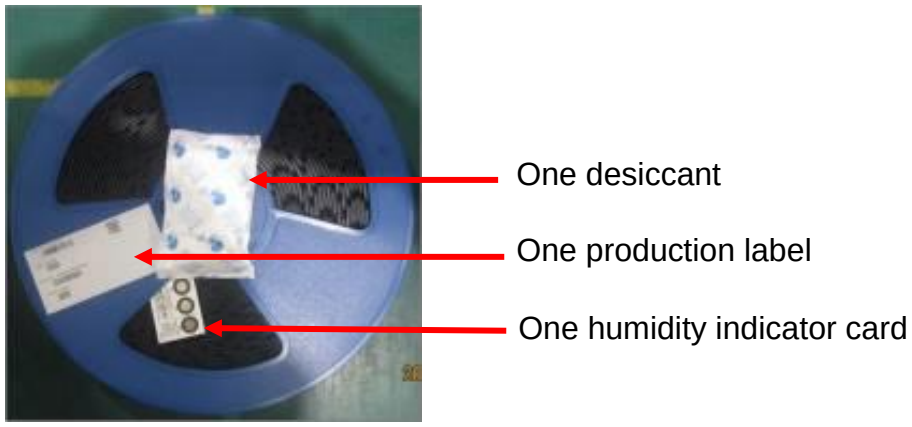
## 4.1 Mechanical Drawing



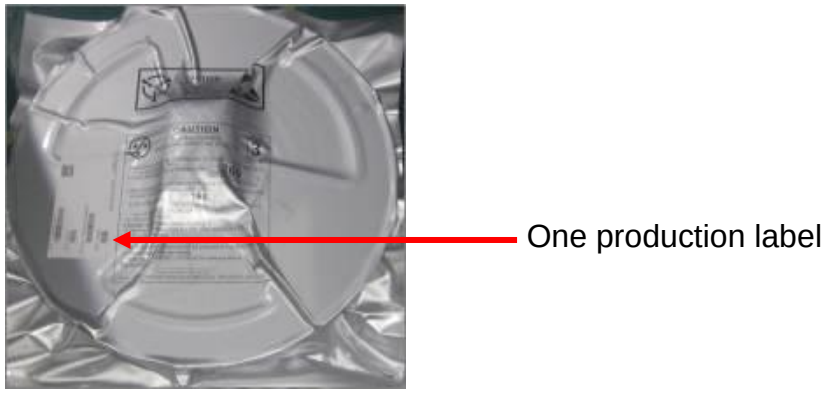

TOLERANCES UNLESS OTHERWISE SPECIFIED:±0.1mm

# 5. Packing Information

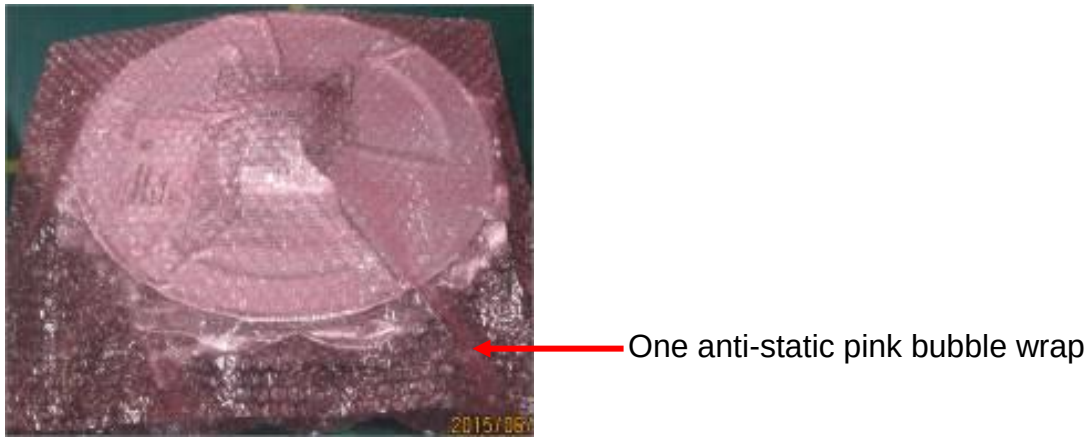
1. One reel can pack 1,500pcs 12x12 stamp modules
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel




3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag




4. A bag is put into the anti-static pink bubble wrap



5. A bubble wrap is put into the inner box and then one label is pasted on the inner box


One production label

6. 5 inner boxes could be put into one carton


7. Sealing the carton by AzureWave tape

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton


| | |
|---|---|
| **Example of carton label** | AzureWave Technologies Inc.<br>AzureWave P/N<br>Customer: 由業務提供<br>Customer P/N: 由業務提供<br>Customer PO: 由業務提供<br>Description: AW-XXXXXX<br>QTY: 1200 pcs<br>C/N<br>N.W. G.W.<br>RoHS COMPLIANT |
| **Example of box label** | BOX0012018 |
| **Example of production label** | P/N:<br>D/C: 1309<br>PCK NO.: PCKNO0069097<br>QTY: 294<br>BAG SEAL DATE: _____ |
| **Example of balance label** | 尾数<br>Balance |

**Note:**

- **1 reel = 1 inner box = 1,500pcs**
- **1 carton = 5 inner boxes = 5 * 1,500pcs = 7,500pcs**