

# **AW-XM664-SD**

## **IEEE 802.11 a/b/g/n/ac/ax**

### **Datasheet**

**Rev. A**

**DF**

**(For Standard)**

## Features

### Wi-Fi

- IEEE 802.11a/b/g/n/ac/ax compliant
- Tri-band (2.4/5/6 GHz) device
- 1x1 with 20-MHz channels supporting PHY data rates up to 802.11ax (MCS11 1024-QAM 5/6)
- Transmit (TX) power with internal PA
- Sensitivity with internal LNA
- OFDMA uplink and downlink as STA
- Downlink multi-user MIMO(MU-MIMO) as STA
- Individual target-wake-time (TWT), broadcast TWT
- BSS color
- Support for switched antenna diversity and external PAs and LNAs for improved range
- SDIO 2.0/3.0: up to 100 Mbps sustained throughput
- Security WPA2 (Personal/Enterprise), WPA3 (Personal/Enterprise with 192-bit security)



AzureWave Technologies, Inc.

## Revision History

Document NO: R2-2690-DST-01

[illegible]

## Table of Contents

Features .....	2
Revision History .....	3
Table of Contents .....	4
1. Introduction .....	5
1.1 Product Overview .....	5
1.2 Block Diagram .....	6
1.3 Specifications Table .....	7
1.3.1 General .....	7
1.3.2 WLAN .....	7
1.3.3 Operating Conditions .....	9
2. Pin Definition .....	10
2.1 Pin Map .....	10
2.2 Pin Table .....	11
3. Electrical Characteristics .....	14
3.1 Absolute Maximum Ratings .....	14
3.2 Recommended Operating Conditions .....	14
3.3 Digital IO Pin DC Characteristics .....	14
3.4 Host Interface .....	15
3.4.1 SDIO Interface .....	15
3.5 Power up Timing Sequence .....	19
3.6 Power Consumption* .....	20
3.6.1 WLAN .....	20
4. Mechanical Information .....	21
4.1 Mechanical Drawing .....	21
5. Packaging Information .....	22

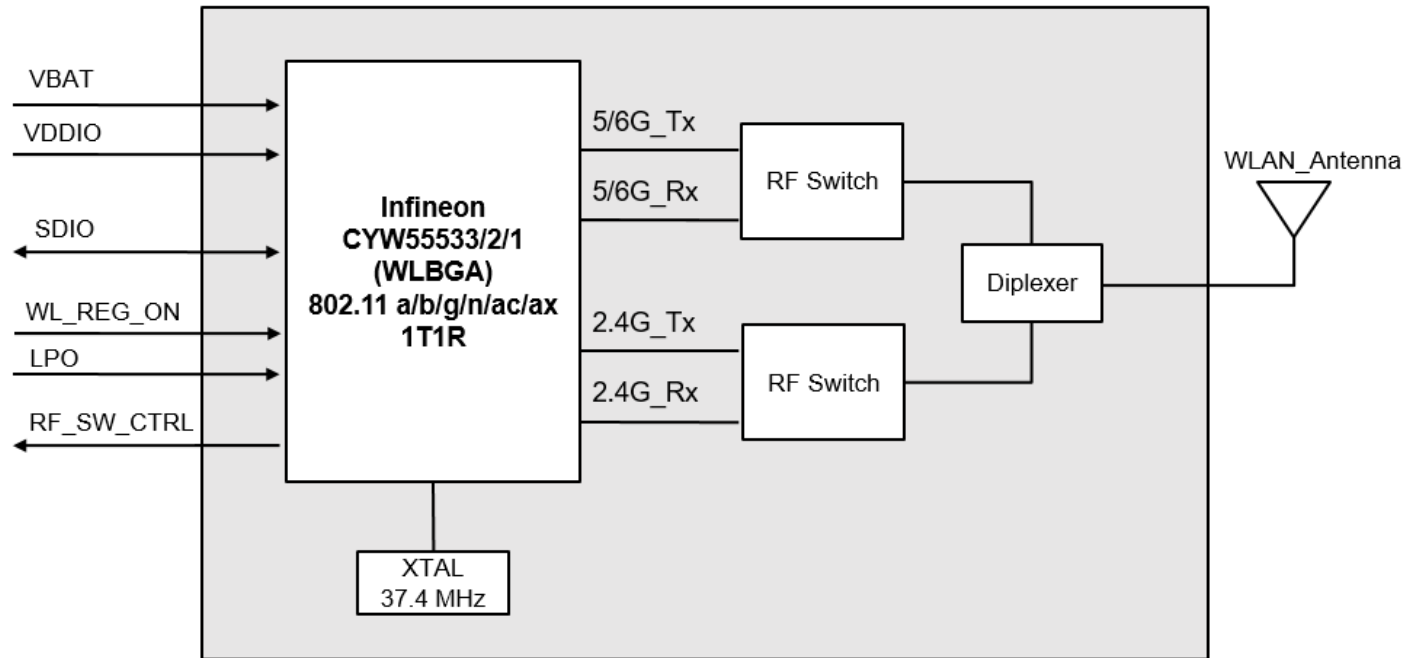
## 1. Introduction

### 1.1 Product Overview

The Infineon AW-XM664-SD device for low-power, single-chip devices that support single-stream, tri-band/dual-band/single-band Wi-Fi 6/6E, IEEE 802.11ax-compliant Wi-Fi MAC/baseband/radio. In 802.11ax mode, the device supports rates up to 1024 QAM MCS11 in 20 MHz channels.

All legacy rates in the 802.11a/b/g/n/ac are also supported. Included on-chip are 2.4 GHz, 5/6 GHz transmit power amplifiers (PA), and low-noise amplifiers (LNA). The device is also capable of operating with external antenna diversity, if an improved range is required. An SDIO v3.0 for interfacing with the host.

## 1.2 Block Diagram



AW-XM664-SD BLOCK DIAGRAM

## 1.3 Specifications Table

### 1.3.1 General

Features	Description
<b>Product Description</b>	IEEE 802.11 a/b/g/n/ac/ax Wireless LAN Module
<b>Major Chipset</b>	Infineon CYW55533/CYW55532/CYW55531
<b>Host Interface</b>	WiFi :SDIO
<b>Dimension</b>	12mm(L) x 12mm(W) x 1.65mm(T)
<b>Form Factor</b>	LGA module, 47 pins
<b>Antenna</b>	1T1R ANT1(Main) : WiFi → TX/RX
<b>Weight</b>	TBD

### 1.3.2 WLAN

Features	Description
<b>WLAN Standard</b>	IEEE 802.11a/b/g/n/ac/ax 1T1R
<b>WLAN VID/PID</b>	N/A
<b>WLAN SVID/SPID</b>	N/A
<b>Frequency Range</b>	WLAN: 2.4 GHz / 5GHz/ 6GHz Band
<b>Modulation</b>	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9), 1024-QAM(MCS10~11)
<b>Number of Channels</b>	<b>2.4GHz</b> ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13 <b>5GHz</b> ■ USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

<b>Output Power</b>	<b>6GHz</b> ■ CH1~CH233				
	<b>2.4G</b>				
		Min	Typ	Max	Unit
	11b (11Mbps) @EVM<35%		TBD		dBm
	11g (54Mbps) @EVM ≤ -25 dB		TBD		dBm
	11n (HT20 MCS7) @EVM ≤ -27 dB		TBD		dBm
	11ax (HE20 MCS11) @EVM ≤ -35 dB		TBD		dBm
	<b>5G</b>				
		Min	Typ	Max	Unit
	11a (54Mbps) @EVM ≤ -25 dB		TBD		dBm
	11n (HT20 MCS7) @EVM ≤ -27 dB		TBD		dBm
	11ac (VHT20 MCS8) @EVM ≤ -30 dB		TBD		dBm
	11ax (HE20 MCS11) @EVM ≤ -35 dB		TBD		dBm
	<b>6G</b>				
		Min	Typ	Max	Unit
	11ax (HE20 MCS11) @EVM ≤ -35 dB		TBD		dBm
<b>Receiver Sensitivity</b>	<b>2.4G</b>				
		Min	Typ	Max	Unit
	11b (11Mbps)		TBD		dBm
	11g (54Mbps)		TBD		dBm
	11n (HT20 MCS7)		TBD		dBm
	11ax (HE20 MCS11)		TBD		dBm
	<b>5G</b>				
		Min	Typ	Max	Unit
	11a (54Mbps)		TBD		dBm
	11n (HT20 MCS7)		TBD		dBm
	11ac (VHT20 MCS8)		TBD		dBm
	11ax (HE20 MCS11)		TBD		dBm



	<b>6G</b>				
		Min	Typ	Max	Unit
	11ax (HE20 MCS11)		TBD		dBm
<b>Data Rate</b>	802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: MCS0~7 HT20 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac: MCS0~8 VHT20 802.11ax: MCS10~11 HE20				
<b>Security</b>	<ul style="list-style-type: none"> <li>● WPA/WPA2/WPA3 personal (SAE, SAE Transmission mode)</li> <li>● WPA3 personal-SAE-FT</li> <li>● WPA3 Enterprise-SAE-FT(Host support)</li> <li>● WPA3 Enterprise with 192-bit encryption</li> <li>● Hardware accelerator (AES)</li> </ul>				

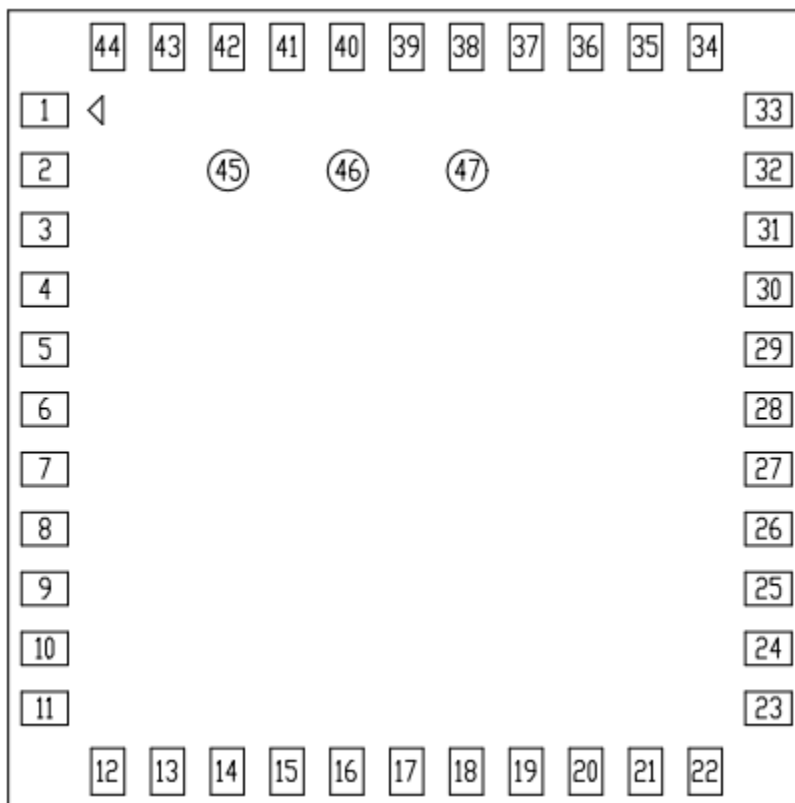
\* If you have any certification questions about output power please contact FAE directly.

### 1.3.3 Operating Conditions

Features	Description
<b>Operating Conditions</b>	
<b>Voltage</b>	2.97 V– 4.8 V
<b>Operating Temperature</b>	TBD
<b>Operating Humidity</b>	less than 85% R.H.
<b>Storage Temperature</b>	TBD
<b>Storage Humidity</b>	less than 60% R.H.
<b>ESD Protection</b>	
<b>Human Body Model</b>	TBD
<b>Changed Device Model</b>	TBD

## 2. Pin Definition

### 2.1 Pin Map



**AW-XM664-SD Top View Pin Map**

## 2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	WL_ANT	WLAN RF TX/RX path.		RF
3	GND	Ground.		GND
4	NC	Floating Pin, No connect to anything.		Floating
5	NC	Floating Pin, No connect to anything.		Floating
6	NC	Floating Pin, No connect to anything.		Floating
7	NC	Floating Pin, No connect to anything.		Floating
8	NC	Floating Pin, No connect to anything.		Floating
9	VBAT	3.3V power pin	3.3V	VCC
10	NC	Floating Pin, No connect to anything.		Floating
11	NC	Floating Pin, No connect to anything.		Floating
12	WL_REG_ON	This signal is used by the PMU to power up the WLAN core and the internal CYW55533/CYW55532/CYW55531 regulators. When this pin is HIGH, the regulators are enabled and the WLAN core is out of reset. When this pin is LOW, all the WLAN core is in reset and all the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and disabled upon recognizing HIGH on this pin.	1.8V	I
13	GPIO0_WL_HOST_WAKE	WL Host Wake.	1.8V	O
14	SDIO_DATA2	SDIO Data Line 2.	1.8V	I/O
15	SDIO_DATA3	SDIO Data Line 3.	1.8V	I/O
16	SDIO_DATA_CMD	SDIO Command Input.	1.8V	I/O
17	SDIO_DATA_CLK	SDIO Clock Input.	1.8V	I
18	SDIO_DATA0	SDIO Data Line 0.	1.8V	I/O
19	SDIO_DATA1	SDIO Data Line 1.	1.8V	I/O
20	GND	Ground.		GND

21	VIN_LDO_OUT	Internal Buck 1.2V voltage generation pin.	1.4V	O
22	VDDIO	1.8V VDDIO supply for WLAN.	1.8V	VCC
23	VIN_LDO	Internal Buck 1.2V voltage generation pin.	1.4V	I
24	LPO	External 32K or RTC clock.	0.2~3.3V	I
25	NC	Floating Pin, No connect to anything.		Floating
26	NC	Floating Pin, No connect to anything.		Floating
27	NC	Floating Pin, No connect to anything.		Floating
28	NC	Floating Pin, No connect to anything.		Floating
29	NC	Floating Pin, No connect to anything.		Floating
30	NC	Floating Pin, No connect to anything.		Floating
31	GND	Ground.		GND
32	NC	Floating Pin, No connect to anything.		Floating
33	GND	Ground.		GND
34	NC	Floating Pin, No connect to anything.		Floating
35	NC	Floating Pin, No connect to anything.		Floating
36	GND	Ground.		GND
37	NC	Floating Pin, No connect to anything.		Floating
38	NC	Floating Pin, No connect to anything.		Floating
39	RF_SW_CTRL_0	Programmable RF switch control lines	3.3V	O
40	GPIO1_WL_DEV_WAKE	WL_DEV_WAKE	1.8V	I
41	NC	Floating Pin, No connect to anything.		Floating
42	NC	Floating Pin, No connect to anything.		Floating
43	NC	Floating Pin, No connect to anything.		Floating
44	NC	Floating Pin, No connect to anything.		Floating
45	NC	Floating Pin, No connect to anything.		Floating
46	NC	Floating Pin, No connect to anything.		Floating

47	NC	Floating Pin, No connect to anything.		Floating
----	----	---------------------------------------	--	----------

### 3. Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
<b>VBAT</b>	DC supply for the VBAT and PA driver supply	-0.5	-	6	V
<b>VDDIO</b>	DC supply voltage for digital I/O	-0.5	-	2.2	V
<b>Tj</b>	Maximum junction temperature	-	-	125	°C

#### 3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
<b>VBAT</b>	Power supply for Internal Regulator	2.97	3.6	4.8	V
<b>VDDIO</b>	DC supply voltage for digital I/O	1.71	1.8	1.89	V

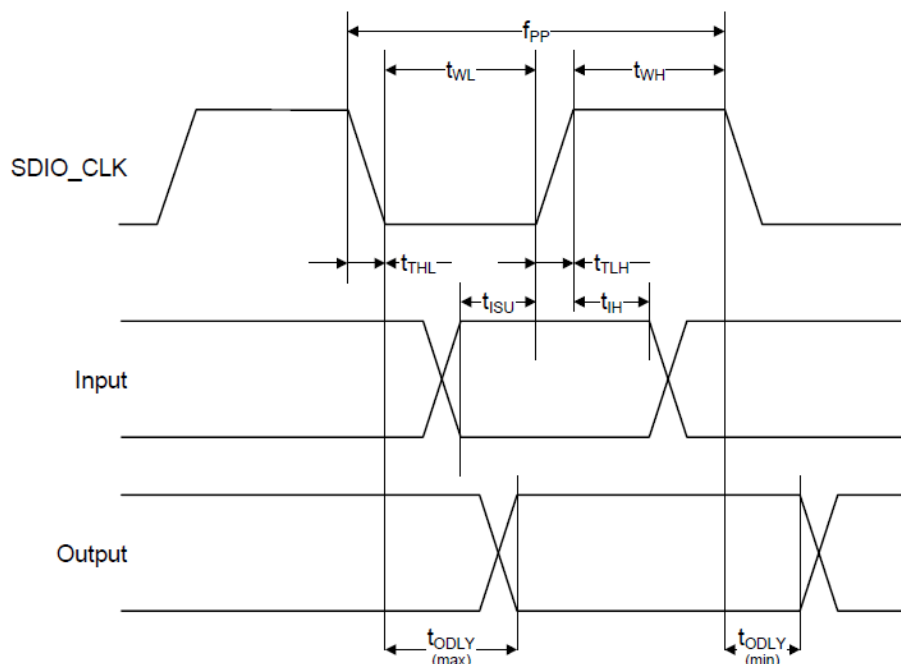
#### 3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
<b>Digital I/O pins, VDDIO=1.8V</b>					
<b>V<sub>IH</sub></b>	Input high voltage	$0.65 \times VDDIO$	-	-	V
<b>V<sub>IL</sub></b>	Input low voltage	-	-	$0.35 \times VDDIO$	V
<b>V<sub>OH</sub></b>	Output high voltage	$VDDIO - 0.40$	-	-	V
<b>V<sub>OL</sub></b>	Output Low Voltage	-	-	0.45	V

## 3.4 Host Interface

### 3.4.1 SDIO Interface

#### SDIO Bus Timing (Default Mode)



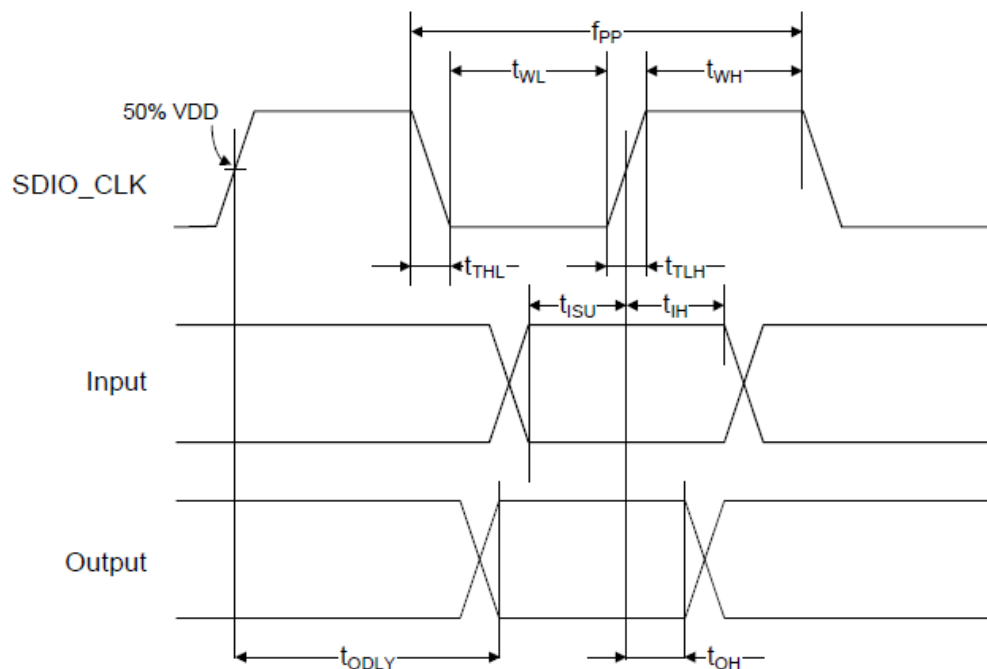
#### SDIO Bus Timing Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
<b>SDIO CLK (All values are referred to minimum VIH and maximum VIL)</b>					
Frequency – Data Transfer mode	$f_{PP}$	0	–	25	MHz
Frequency – Identification mode	$f_{OD}$	0	–	400	kHz
Clock low time	$t_{WL}$	10	–	–	ns
Clock high time	$t_{WH}$	10	–	–	ns
Clock rise time	$t_{TLH}$	–	–	10	ns
Clock low time	$t_{THL}$	–	–	10	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
Input setup time	$t_{ISU}$	5	–	–	ns
Input hold time	$t_{IH}$	5	–	–	ns

Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t <sub>ODLY</sub>	0	–	14	ns
Output delay time – Identification mode	t <sub>ODLY</sub>	0	–	50	ns



## SDIO Bus Timing (High-Speed Mode)



### SDIO Bus Timing Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
<b>SDIO CLK (all values are referred to minimum VIH and maximum VIL<sup>b</sup>)</b>					
<b>Frequency – Data Transfer Mode</b>	$f_{PP}$	0	–	50	MHz
<b>Frequency – Identification Mode</b>	$f_{OD}$	0	–	400	kHz
<b>Clock low time</b>	$t_{WL}$	7	–	–	ns
<b>Clock high time</b>	$t_{WH}$	7	–	–	ns
<b>Clock rise time</b>	$t_{TLH}$	–	–	3	ns
<b>Clock low time</b>	$t_{THL}$	–	–	3	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
<b>Input setup Time</b>	$t_{ISU}$	6	–	–	ns
<b>Input hold Time</b>	$t_{IH}$	2	–	–	ns
<b>Outputs: CMD, DAT (referenced to CLK)</b>					
<b>Output delay time – Data Transfer Mode</b>	$t_{ODLY}$	–	–	14	ns
<b>Output hold time</b>	$t_{OH}$	2.5	–	–	ns

Total system capacitance (each line)	CL	–	–	40	pF
--------------------------------------	----	---	---	----	----

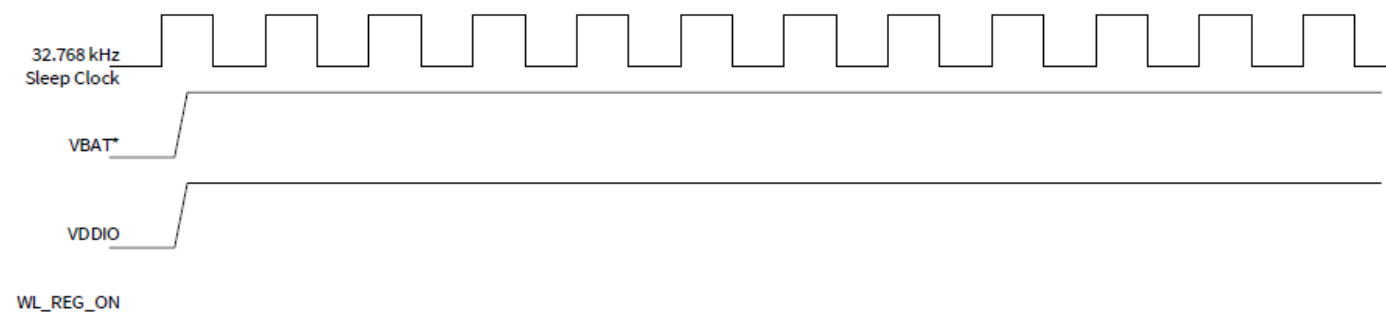
### 3.5 Power up Timing Sequence

AW-XM664-SD has a signal that allow the host to control power consumption by enabling or disabling WLAN, and internal regulator blocks. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

#### Description of Control Signals

##### ■ WL\_REG\_ON:

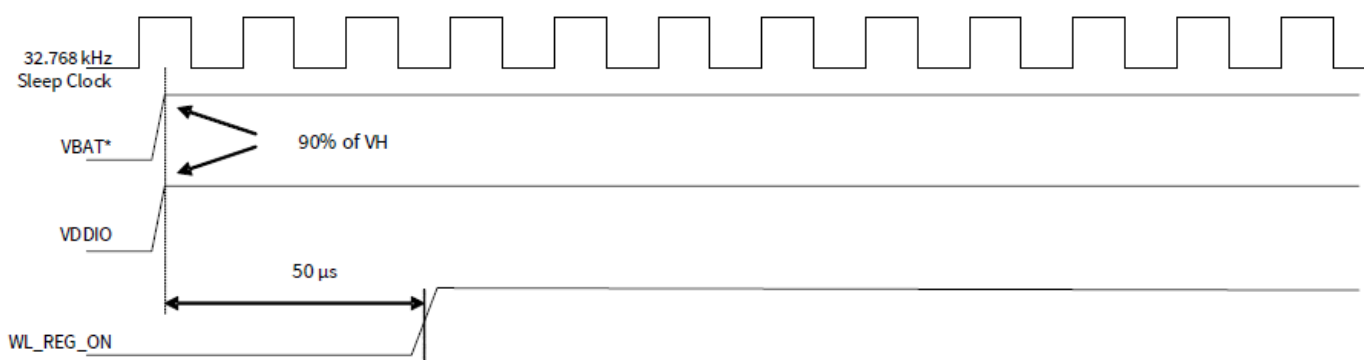
Used by the PMU to power up the WLAN section and control the internal AW-XM664-SD regulators. When this pin is HIGH, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.



**\*Notes:**

1. VBAT and VDDIO should not rise 10%–90% faster than 40  $\mu$ s.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is HIGH.

#### WLAN = ON



**\*Notes:**

1. VBAT and VDDIO should not rise 10%–90% faster than 40  $\mu$ s.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is HIGH.

#### WLAN = OFF

## **3.6 Power Consumption\***

### **3.6.1 WLAN**

**TBD**

## **4. Mechanical Information**

### **4.1 Mechanical Drawing**

**TBD**

## 5. Packaging Information

**TBD**