AW-XM650

IEEE 802.11a/b/g/n/ac/ax Wi-Fi with Bluetooth

Combo LGA Module

Datasheet

Rev. B

DF

(For Standard)

Features

WLAN

- IEEE 802.11a/b/g/n/ac/ax compliant
- Dual-band (2.4 GHz/5 GHz)
- 1x1 with 20 MHz channels supporting PHY data rates up to 802.11ax (MCS11 1024-QAM 5/6)
- Wi-Fi 6 release features
  - OFDMA uplink and downlink as STA
  - Downlink multi-user MIMO as STA
  - Individual target-wake-time (TWT)
  - BSS color
- - Interfaces
  - SDIO 2.0/3.0: Up to 100 Mbps sustained throughput
  - GSPI: Up to 20 Mbps sustained throughput
- Modes: STA, SoftAP, Wi-Fi Direct
- Security
  - TKIP, WEP, WPA2 (Personal/Enterprise), WPA3 (Personal/Enterprise/192b)

Bluetooth

- Bluetooth® 5.4 (BDR + EDR + Bluetooth® Low Energy)
- All Bluetooth® 5.0/5.1/5.2/5.3/5.4 optional features
  - Host to Controller Encryption Key Control Enhancements
  - LE long range
  - LE 2Mbps
  - LE mesh
  - Advertising extensions
  - LE audio with LC3 codec in ROM in offload mode or HCI mode with LC3 codecs on host
  - LE Isochronous Channels
- Bluetooth® LNA can be shared with WLAN LNA for reduced antenna count
- Dedicated Bluetooth® LNA for improved RF and coexistence performance
- 0, +13, and +20 dBm Bluetooth® PA paths optimized for best efficiency, output power options adjustable in 4dB steps.
- UART interface (4-wire)
- Two audio interfaces, supporting hands free profile (HFP), A2DP, and LE audio.
- TDM1, TDM2 supporting inter-IC sound (I2S) (2-channels) and PCM (8-channels), 8k to 96k sample rates, and16- and 24-bit sample widths
- Bidirectional PCM (TDM and I2S) with 8k, 16k sample rates and 16-bit sample width for HFP. Multiplexed with TDM2 through second audio interface.
- Single-direction I2S with 44.1k. The 48k sample rates and 16-bit sample width for

A2DP. Multiplexed with TDM2 through second audio interface.

- On-chip memory includes 768 KB SRAM and 2048 KB ROM

Revision History

Document NO: R2-2650-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2024/04/16	DCN031389	● Initial version	Nyx. Wong	N.C.Chen
B	2024/11/13	DCN032492	● Updated RF specification ● Updated Operating Conditions ● Updated Pin Table ● Updated Power Consumption ● Removed JTAG	Tom Hsieh	N.C.Chen

Table of Contents

1. Introduction

1.1 Product Overview

The AW-XM650 is a low-power, single-chip device that supports single-stream, dual-band, Wi-Fi 6, IEEE802.11ax-compliant Wi-Fi MAC/baseband/radio and Bluetooth®/Bluetooth® Low Energy 5.4. In 802.11ax mode, the device supports rates up to 1024 QAM MCS11 in 20 MHz channels. All legacy rates in the 802.11a/b/g/n/ac are also supported. Included on-chip are 2.4 GHz, 5 GHz transmit power amplifiers (PA) and low-noise amplifiers (LNA). An SDIO v3.0 interface or GSPI are available for interfacing with the host.

The AW-XM650 includes a Bluetooth® subsystem that is Bluetooth® 5.4-compliant, supporting basic rate, enhanced data rate (EDR) and Bluetooth® Low Energy. The device supports Bluetooth® Low Energy 2 Mbps, Bluetooth® Low Energy 1 Mbps, low-energy mesh, low-energy long range (LR), and advertising extensions. The device can support Bluetooth® Low Energy audio, with LC3 codec running on the device enabling typical Smart watch audio use cases. A pair of time-division multiplexing (TDM) interfaces enables a flexible interface for various audio use cases and a PDM interface is available for connecting digital microphones. The device includes on-chip power

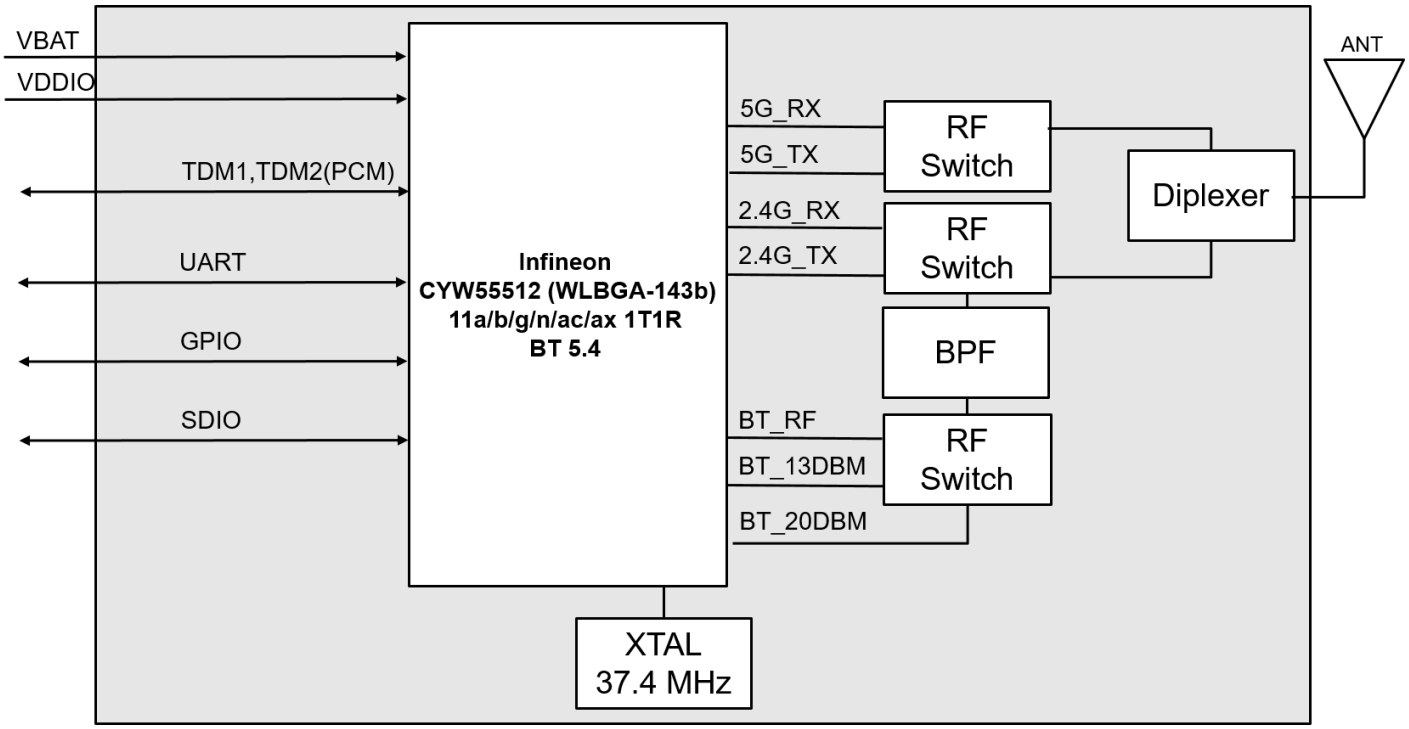
Amplifiers supporting three different output power paths optimized for best efficiency, 0 dBm, +13 dBm, and +20 dBm path for driving poor antennas in wearable devices. A 4-wire UART interface is available for interfacing with the host.

The CYW55512 is designed to address the needs of Internet on Things (IoT) devices that require minimal power consumption and compact size. It includes a power management unit (PMU), and an internal 37.4 MHz crystal which provides the system reference clock, and can operate from an external 32.768 kHz crystal (eLPO) for higher accuracy.

The AW-XM650 operates over the TBD temperature range, and is available in 12x12 mm package.

1.2 Block Diagram

1.2.1 Block Diagram



AW-XM650 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11a/b/g/n/ac/ax Wi-Fi with Bluetooth Combo LGA Module
Major Chipset	Infineon CYW55512(WLBGA-143-ball)
Host Interface	Wi-Fi: SDIO , BT: UART/PCM
Dimension	12mm(L) 12xmm(W) x 1.75 mm(H) (Typical)
Form factor	LGA Module 63 pin
Antenna	1T1R for WiFi/BT ANT1(Main)：WiFi/Bluetooth → TX/RX
Weight	0.5g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac/ax, Wi-Fi compliant
Frequency Rage	WLAN: 2.4 GHz / 5 GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9), 1024-QAM(MCS10~11)
Number of Channels	**2.4GHz** ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13 **5GHz** ■ USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

Output Power[1][2] (Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM≦-9 dB	17	19	21	dBm
11g (54Mbps) @EVM≦-25 dB	16	18	20	dBm
11n (HT20 MCS7) @EVM≦-27 dB	15	17	19	dBm
11ax (HE20 MCS11) @EVM≦-35 dB	13	15	17	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM≦-25 dB	14.5	16.5	18.5	dBm
11n (HT20 MCS7) @EVM≦-27 dB	13	15	17	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	12	14	16	dBm
11ax (HE20 MCS11) @EVM≦-35 dB	11	13	15	dBm

Receiver Sensitivity

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-89	-86	dBm
11g (54Mbps)		-76	-73	dBm
11n (HT20 MCS7)		-76	-73	dBm
11ax (HE20 MCS11)		-63	-60	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		-74	-71	dBm
11n (HT20 MCS7)		-74	-71	dBm
11ac[3] (VHT20 MCS8)		-70	-67	dBm
11ax[4] (HE20 MCS11)		-60	-57	dBm

Data Rate

802.11b: 1, 2, 5.5, 11Mbps
802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps

[1] EVM Spec are under typical test conditions.
[2] Output Power means measurement power inside the range (Min and Max) with spectral mask and EVM compliance.
[3] Tested by BCC instead of LDPC.
[4] Tested by BCC instead of LDPC.

	802.11n: MCS0~7 HT20 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac: MCS0~8 VHT20 802.11ax: MCS0~11 HE20
Security	● WEP,WPA/WPA2/WPA3 Enterprise with 192-bit Encryption, hardware accelerator (AES) ● AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility. ● Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS).

*** If you have any certification questions about output power please contact FAE directly.**
**** Project is in engineering stage, RF performance is still being verified.**

1.3.3 Bluetooth

Features	**Description**
Bluetooth Standard	BT5.4+Enhanced Data Rate (EDR)
Bluetooth VID/PID	N/A
Frequency Rage	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: 4-DQPSK Payload 3M: 8DPSK
Output Power	

	Min	Typ	Max	Unit
BR	3	6.5	10	dBm
BLE(1M)	3	6.5	10	dBm
BLE(2M)	3	6.5	10	dBm

Receiver Sensitivity[5]

	Min	Typ	Max	Unit
BR		-86	-83	dBm
BLE(1M)		-89	-86	dBm
BLE(2M)		-86	-83	dBm

[5] Tested by sLNA.

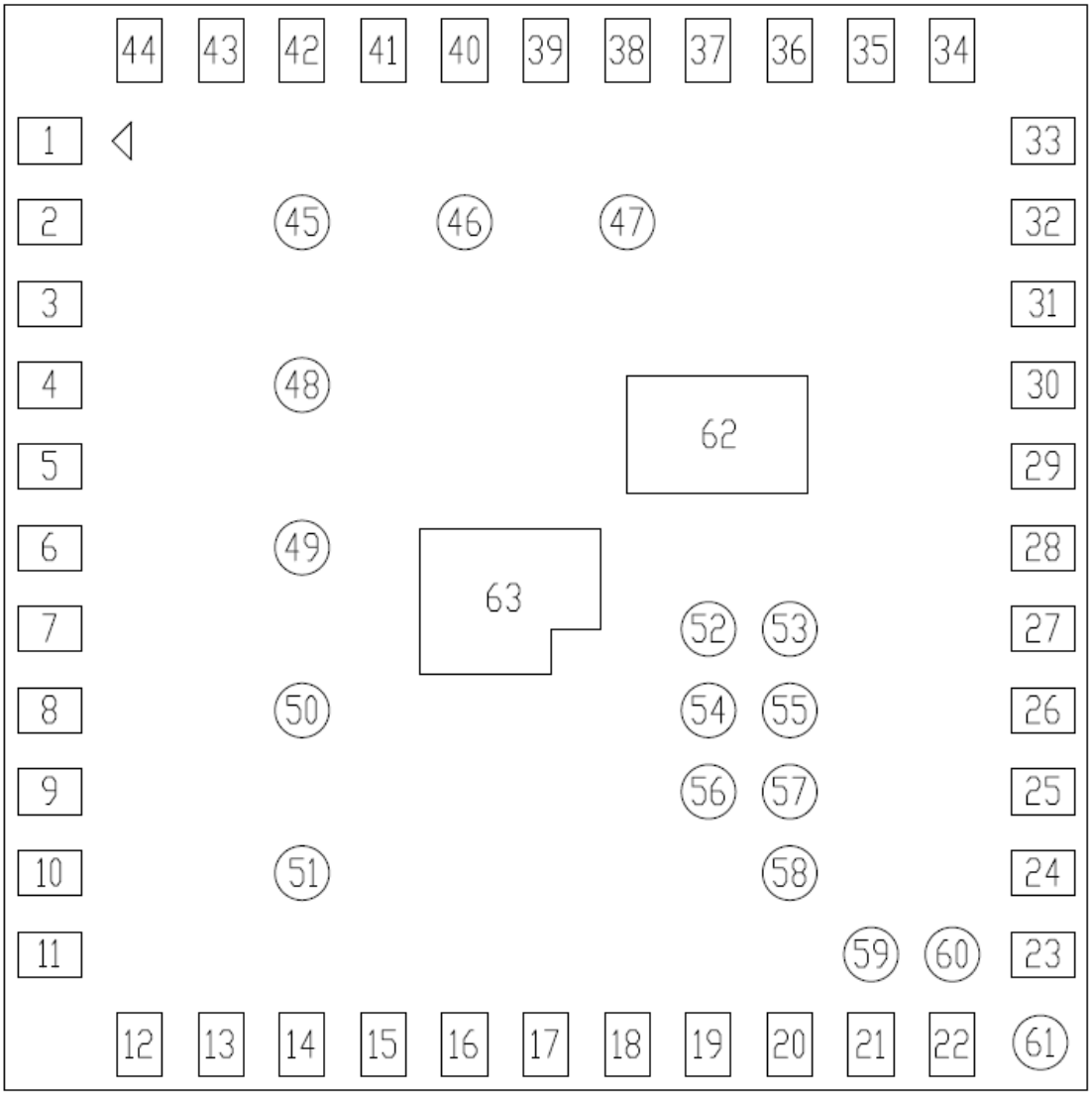
1.3.4 Operating Conditions

Operating Conditions	
Voltage	Power supply for host:3.3V
Operating Temperature	-40 ℃ ~ 85℃[6]
Operating Humidity	less than 85% R.H.
Storage Temperature	-40 ℃ ~ 85 ℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	±2000V
Changed Device Model	±250V

[6] -40℃~85℃ is Functional operation, for detail please check with AzureWave FAE.

2. Pin Definition

2.1 Pin Map



AW-XM650 Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
3	GND	Ground.		GND
4	GPIO_2	GPIO configuration pin	VDDIO	I/O
5	GPIO_3	GPIO configuration pin	VDDIO	I/O
6	BT_DEV_WAKE	BT Device Wake	VDDIO	I
7	BT_HOST_WAKE	BT Host Wake	VDDIO	O
8	GPIO_4	GPIO configuration pin		I/O
9	VBAT	3.3V power pin	VBAT	VCC
10	NC	Floating Pin, No connect to anything.		Floating
11	NC	Floating Pin, No connect to anything.		Floating
12	WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 KΩ pull down resistor that is auto enabled and disabled upon recognizing high on this pin.. It can be disabled through programming.	VDDIO	I
13	WL_SDIO_HOSTWAKE	WL Host Wake	VDDIO	O
14	SDIO_DATA2	SDIO Data Line 2	VDDIO	I/O
15	SDIO_DATA3	SDIO Data Line 3	VDDIO	I/O
16	SDIO_CMD	SDIO Command Input	VDDIO	I/O
17	SDIO_CLK	SDIO Clock Input	VDDIO	I
18	SDIO_DATA0	SDIO Data Line 0	VDDIO	I/O
19	SDIO_DATA1	SDIO Data Line 1	VDDIO	I/O
20	GND	Ground.		GND

21	VIN_LDO_OUT	Internal Buck voltage generation pin	1.12V(typ)	VCC
22	VDDIO	1.8V VDDIO supply for WLAN and BT	VDDIO	VCC
23	VIN_LDO	Internal Buck voltage generation pin	1.12V(typ)	VCC
24	SUSCLK_IN	External 32.768K or RTC clock		I
25	TDM2_DO/BT_PCM_OUT	TDM2_DO/PCM data Out	VDDIO	O
26	TDM2_SCK/BT_PCM_CLK	TDM2_SCK/PCM Clock	VDDIO	I/O
27	TDM2_DI/BT_PCM_IN	TDM2_DI/PCM data Input	VDDIO	I
28	TDM2_WS/BT_PCM_SYNC	TDM2_WS/PCM Synchronization control	VDDIO	I/O
29	NC	Floating Pin, No connect to anything.		Floating
30	NC	Floating Pin, No connect to anything.		Floating
31	GND	Ground.		GND
32	TDM2_MCK	TDM2 interface Master Clock	VDDIO	I/O
33	GND	Ground.		GND
34	BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserte. This pin has an internal 50 kΩ pull-down resistor that is auto enabled and disabled upon recognizing high on this pin. It can be disabled through programming.	VDDIO	I
35	GPIO_5	GPIO configuration pin	VDDIO	I/O
36	GND	Ground.		GND
37	NC	Floating Pin, No connect to anything.		Floating
38	NC	Floating Pin, No connect to anything.		Floating
39	NC	Floating Pin, No connect to anything.		Floating
40	NC	Floating Pin, No connect to anything.		Floating
41	BT_UART_RTS_N	High-Speed UART RTS	VDDIO	O
42	BT_UART_TXD	High-Speed UART Data Out	VDDIO	O

43	BT_UART_RXD	High-Speed UART Data In	VDDIO	I
44	BT_UART_CTS_N	High-Speed UART CTS	VDDIO	I
45	BT_GPIO_2	Bluetooth GPIO configuration pin	VDDIO	I/O
46	BT_GPIO_3	Bluetooth GPIO configuration pin	VDDIO	I/O
47	BT_GPIO_4	Bluetooth GPIO configuration pin	VDDIO	I/O
48	GND	Ground.		GND
49	GND	Ground.		GND
50	GND	Ground.		GND
51	GND	Ground.		GND
52	TDM1_DO	TDM2 interface Data Out	VDDIO	
53	LHL_GPIO_3	Miscellaneous GPIO configuration pin	VDDIO	I/O
54	LHL_GPIO_2	Miscellaneous GPIO configuration pin	VDDIO	I/O
55	TDM1_SCK	TDM1 interface Slave Clock	VDDIO	
56	TDM1_WS	TDM1 interface WordSelec	VDDIO	
57	TDM1_MCK	TDM1 interface Master Clock	VDDIO	
58	TDM1_DI	TDM1 interface Data In	VDDIO	
59	GND	Ground.		GND
60	GND	Ground.		GND
61	GND	Ground.		GND
62	GND	Ground.		GND
63	GND	Ground.		GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply voltage for VBAT.	-0.5	-	+6[7]	V
VDDIO	DC supply voltage for VDDIO.	-0.5	-	+2.2	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply voltage for VBAT.	3.13[8]	3.3	3.6	V
VDDIO	DC supply voltage for VDDIO.	1.71	1.8	1.89	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO=1.8V					
V_{IH}	Input high voltage (V_{DDIO})	0.65 × VDDIO	-		V
V_{IL}	Input low voltage (V_{DDIO})	-	-	0.35 × VDDIO	V
V_{OH}	Output High Voltage @ 2mA	VDDIO – 0.40	-	-	V
V_{OL}	Output Low Voltage @ 2mA	-	-	0.45	V

[7] The maximum continuous voltage is 5.25 V. Voltage transients up to 6.0 V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed.

[8] AW-XM650 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13V < VBAT < 3.5V.

3.4 Power up Timing Sequence

The AW-XM650 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals (Power-Up/Power-Down/Reset Control Signals)

Signal	Description
WL_REG_ON	Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-XM606 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and disabled upon recognizing high on this pin.
BT_REG_ON	Used by the PMU to power up the BT section. It is also OR-gated with the WL_REG_ON input to control the internal AW-XM606 regulators. When this pin is high, the regulators are enabled and the BT section is out of reset. When this pin is low the BT section is in reset. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and disabled upon recognizing high on this pin.

Control Signal Timing Diagrams

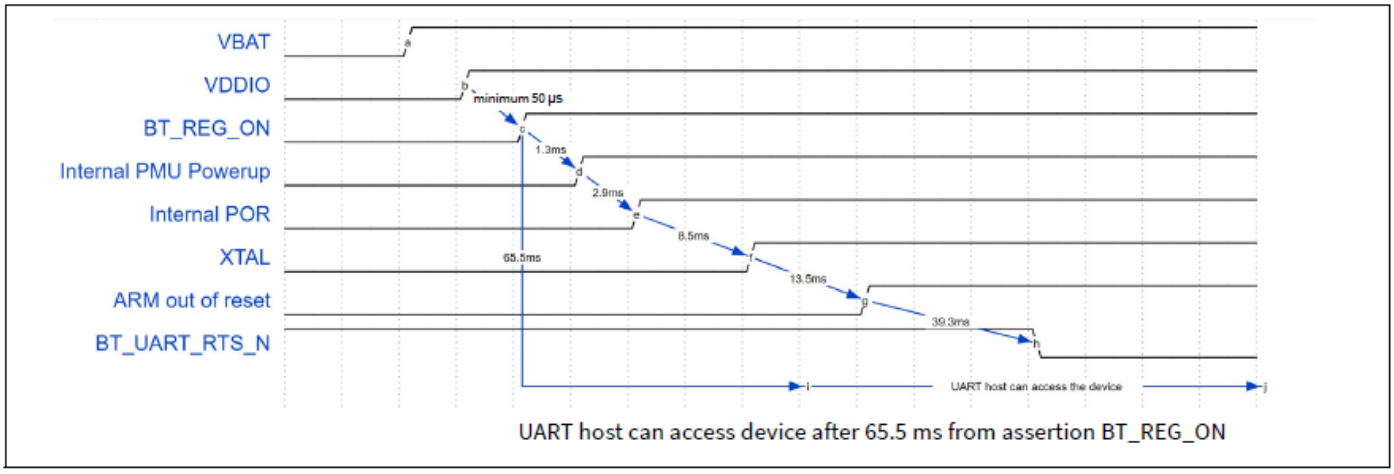


Figure 1 Bluetooth® subsystem boot-up sequence

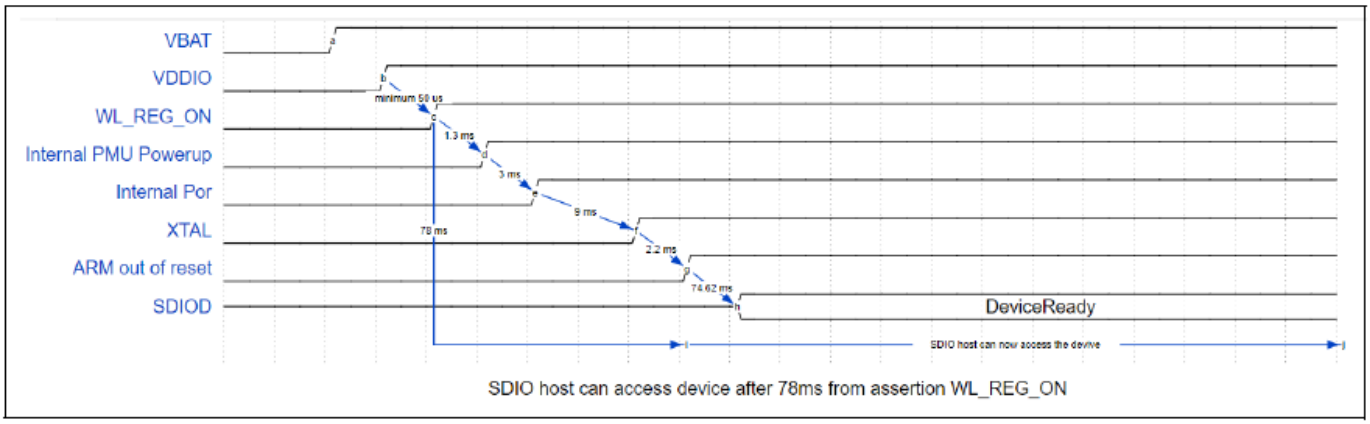


Figure 2 WLAN boot-up sequence for SDIO

3.5 SDIO Timing

3.5.1 SDIO default mode timing

SDIO default mode timing is shown by the combination of Figure 1 and Table 1.

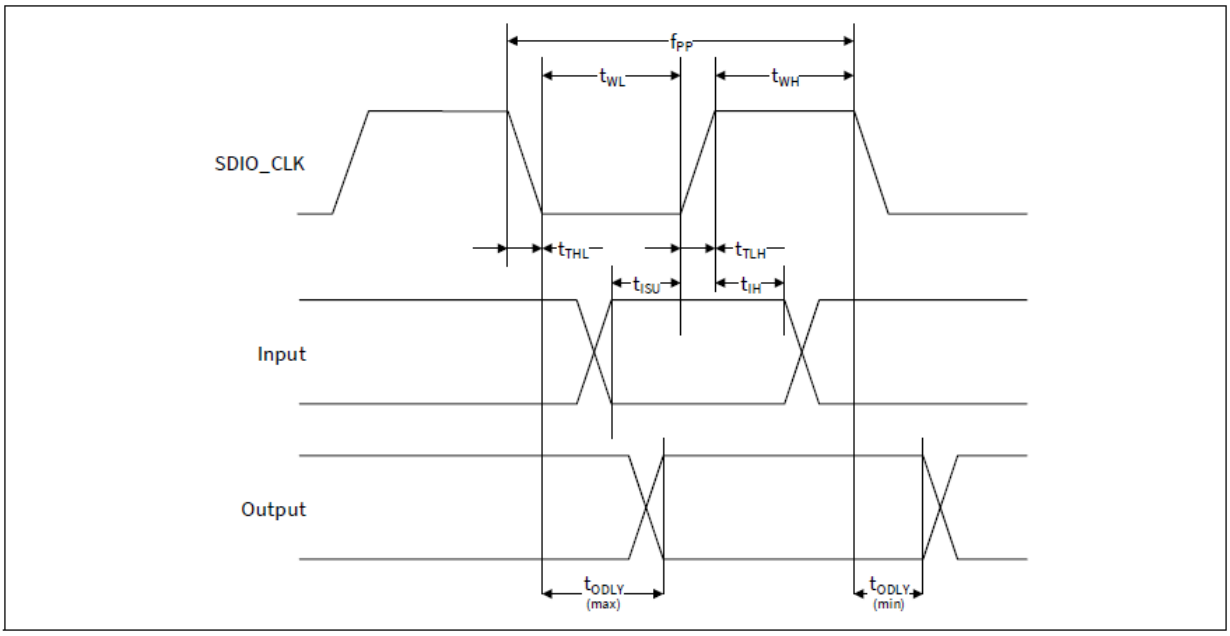


Figure 1 SDIO bus timing (Default mode)

Table 1 SDIO bus timing[9] parameters (Default mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[87])					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

87.Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

[9] Timing is based on CL ≦ 40 pF load on CMD and data.

3.5.2 SDIO high-speed mode timing

SDIO high-speed mode timing is shown by the combination of Figure 2 and Table 2.

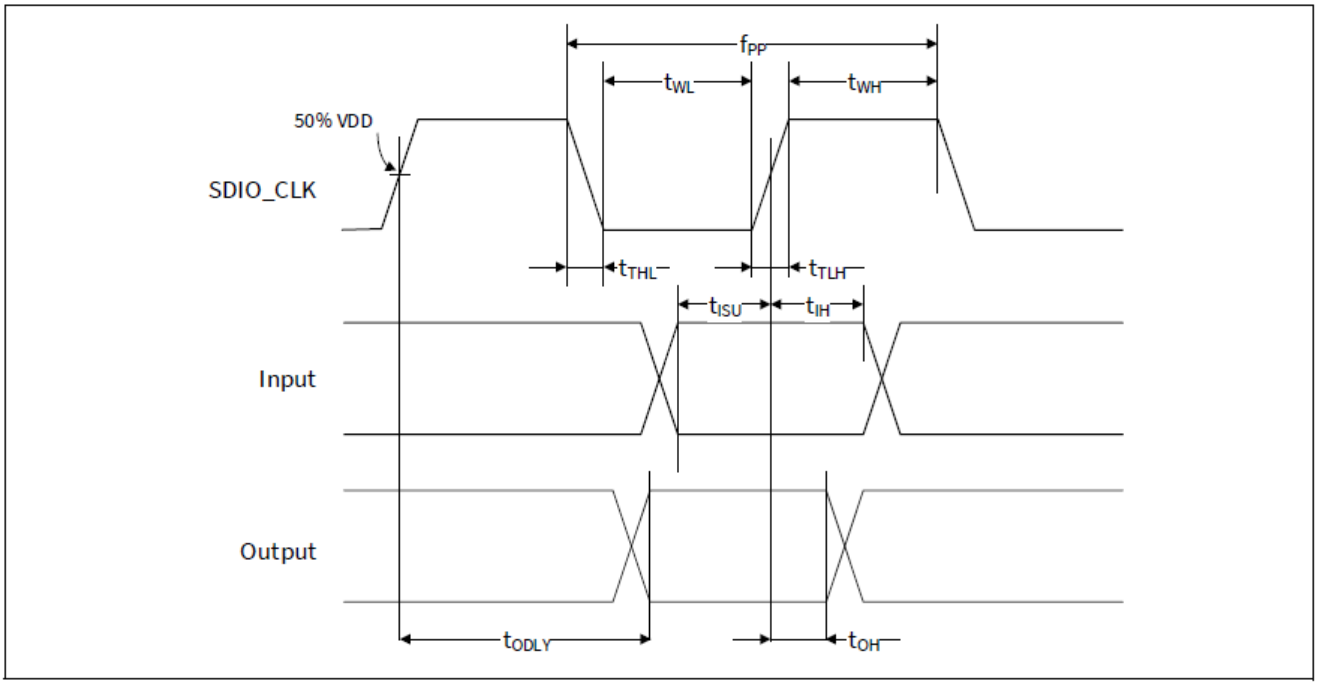


Figure 2 SDIO bus timing (high-speed mode)

Table 2 SDIO bus timing[10] parameters (Default mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[89]					
Frequency – Data Transfer mode	f_{PP}	0	–	50	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

89.Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

[10] Timing is based on CL ≦ 40 pF load on CMD and data.

3.5.2 SDIO bus timing specifications in SDR modes

3.5.2.1 Clock timing

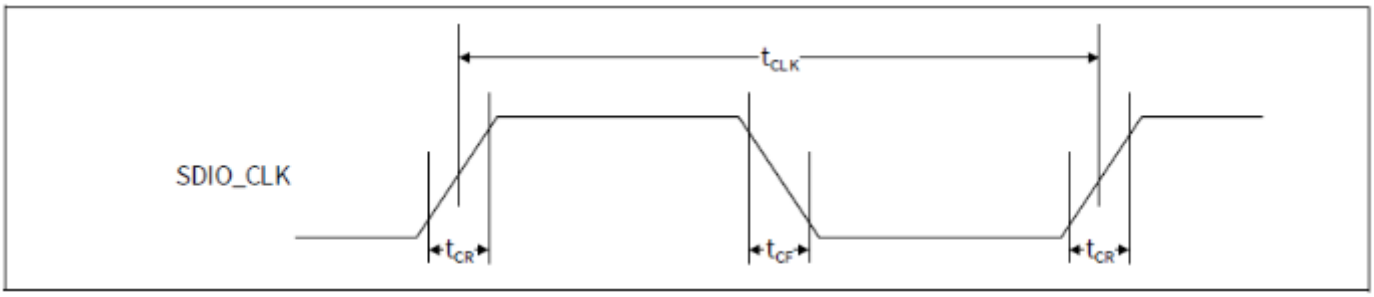


Figure 3 SDIO clock timing (SDR modes)

Table 3 SDIO bus clock timing parameters (SDR modes)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		12.5	–	ns	SDR50 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) at 100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) at 208 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	30	70	%	–

3.5.2.2 Device input timing

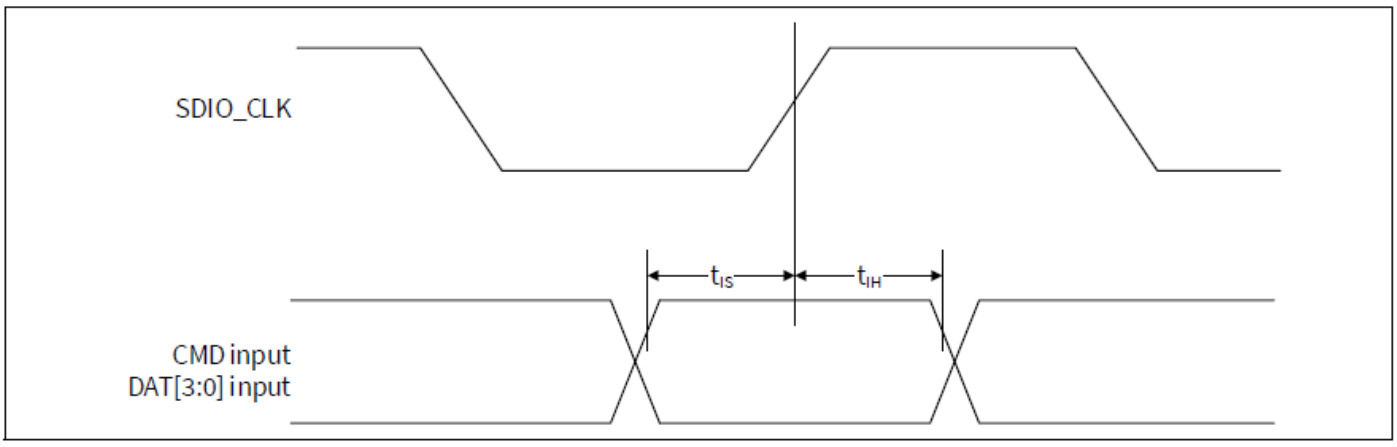


Figure 4 SDIO bus input timing (SDR modes)

Table 4 SDIO bus input timing parameters (SDR modes)

Symbol	Min	Max	Unit	Comments
SDR50 mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975 V

3.5.2.3 Device output timing

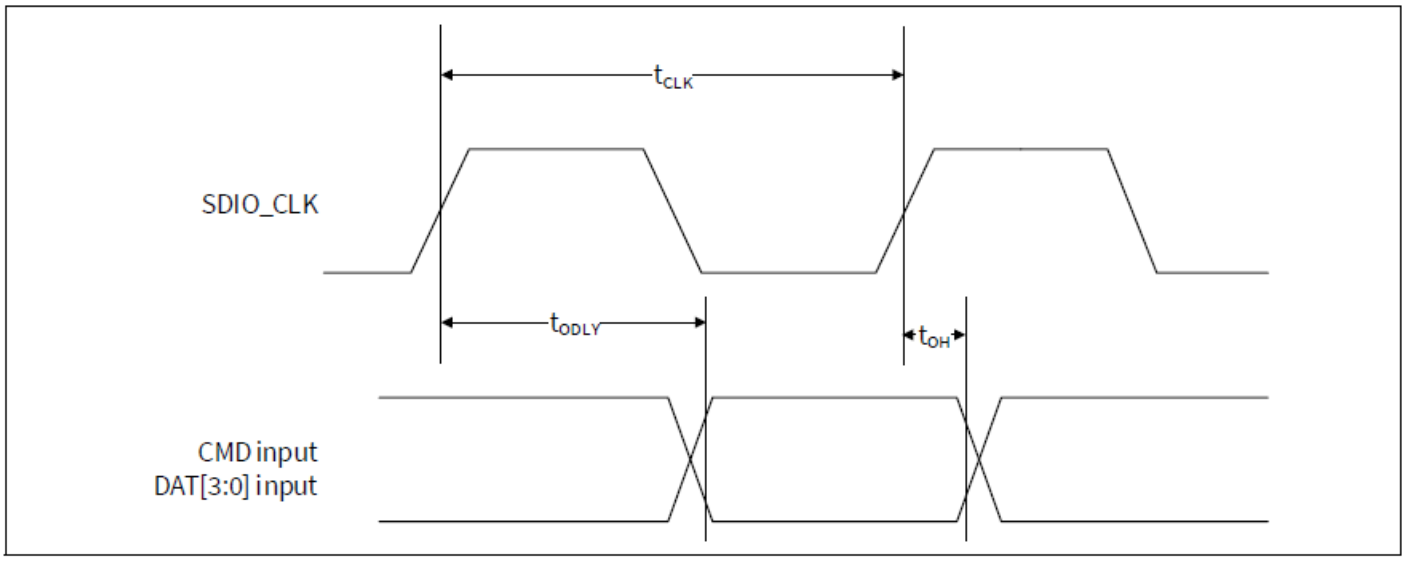


Figure 5 SDIO bus output timing (SDR modes)

Table 5 SDIO bus output timing parameters (SDR modes up to 80 MHz)

Symbol	Min	Max	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns C_L = 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns C_L = 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L = 15 pF

3.5.2.4 SDIO bus timing specifications in DDR50 mode

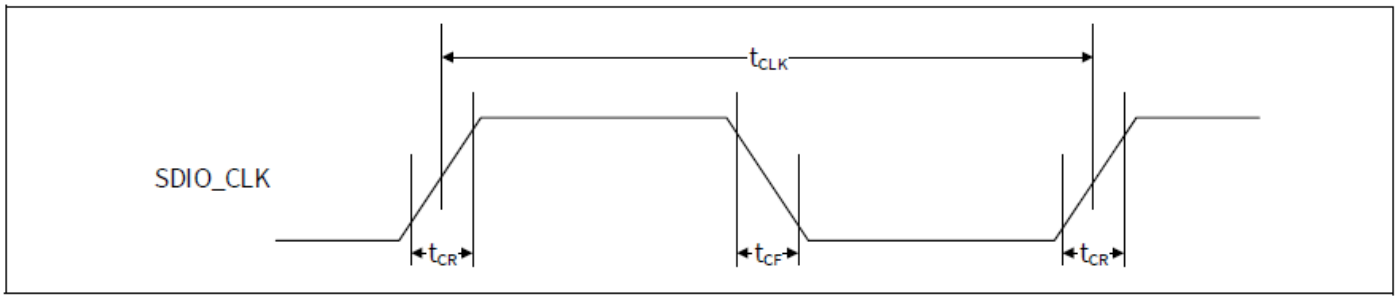


Figure 6 SDIO clock timing (DDR50 mode)

Table 6 SDIO bus clock timing parameters (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	25	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 4.00 ns (max) at 50 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	45	55	%	–

3.5.2.5 Data timing

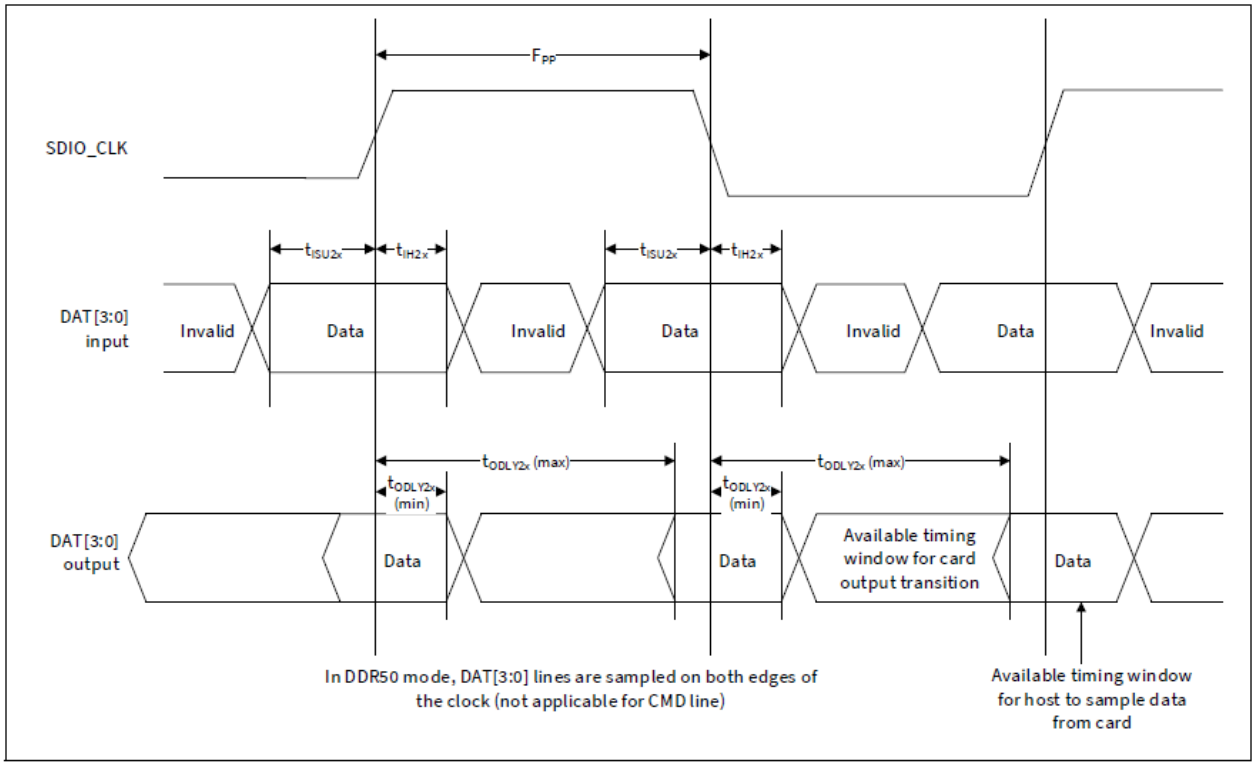


Figure 7 SDIO data timing (DDR50 mode)

Table 7 SDIO bus timing parameters (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

3.7 Power Consumption[11]

3.7.1 WLAN

No.	Item			VBAT_IN=3.3 V	
				Max.	Avg.
1	Pdn *(1)(2)(5)			TBD	TBD
2	Deep Sleep *(2)(3)(5) (Not associated with AP)			TBD	TBD
3	Power Save DTIM 1 (2.4GHz)*(2)(4)(5)			TBD	TBD
4	Power Save DTIM 1 (5GHz) *(2)(4)(5)			TBD	TBD
Band (GHz)	**Mode**	**BW (MHz)**	**RF Power (dBm)**	**Transmit*(6)**	
				Max.	**Avg.**
2.4	11b@1Mbps	20	19	264	260
	11g@54Mbps	20	18	269	243
	11n@MCS0	20	17	247	221
	11ax@MCS11 NSS1	20	15	210	207
5	11a@6Mbps	20	16.5	313	309
	11n@MCS7	20	15	272	269
	11ac@MCS0 NSS1	20	14	276	255
	11ac@MCS8 NSS1	20	14	260	247
	11ax@MCS0 NSS1	20	13	267	252
	11ax@MCS11 NSS1	20	13	245	243
Band (GHz)	**Mode**	**BW(MHz)**		**Receive*(6)**	
				Max.	**Avg.**
2.4	11b@11Mbps	20		30.2	29.1
	11g@54Mbps	20		35.5	33.4
	11n@MCS7	20		35.7	34.2
	11ax@MCS11 NSS1	20		42.8	41.1
5	11a@54Mbps	20		44.1	42.2
	11n@MCS7	20		44.6	43.1
	11ac@MCS8 NSS1	20		44.7	43.5
	11ax@MCS11 NSS1	20		47.1	46.1

***Current Unit: mA**

[11] For Details, please contact Azurewave FAE

No.	Item			VDDIO=1.8 V	
				Max.	Avg.
1	Pdn *(1)(2)(5)			TBD	TBD
2	Deep Sleep *(2)(3)(5) (Not associated with AP)			TBD	TBD
3	Power Save DTIM 1 (2.4GHz)*(2)(4)(5)			TBD	TBD
4	Power Save DTIM 1 (5GHz) *(2)(4)(5)			TBD	TBD
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit*(6)	
				Max.	Avg.
2.4	11b@11Mbps	20	19	4.73	4.71
	11ax@MCS11 NSS1	20	15	4.73	4.63
5	11a@54Mbps	20	16.5	4.71	4.43
	11ax@MCS11 NSS1	20	13	4.73	4.62
Band (GHz)	Mode	BW(MHz)		Receive*(6)	
				Max.	Avg.
2.4	11b@11Mbps	20		0.73	0.72
5	11ax@MCS11 NSS1	20		0.73	0.72

***Current Unit: mA**

3.7.2 Bluetooth

Mode	Packet Type	RF Power (dBm)	VBAT_IN=3.3 V	
			Max.	Avg.
Sleep*(1)	N/A	N/A	TBD	TBD
Transmit*(2)(3)	DH5	6.5	36.4	34.9
Receive*(2)(3)	DH5	N/A	24.1	22.6

***Current Unit: mA**

Mode	Packet Type	RF Power (dBm)	VDDIO=1.8 V	
			Max.	Avg.
Sleep*(1)	N/A	N/A	TBD	TBD
Transmit*(2)(3)	DH5	6.5	499	487
Receive*(2)(3)	DH5	N/A	494	480

***Current Unit: uA**

3.8 Frequency Reference

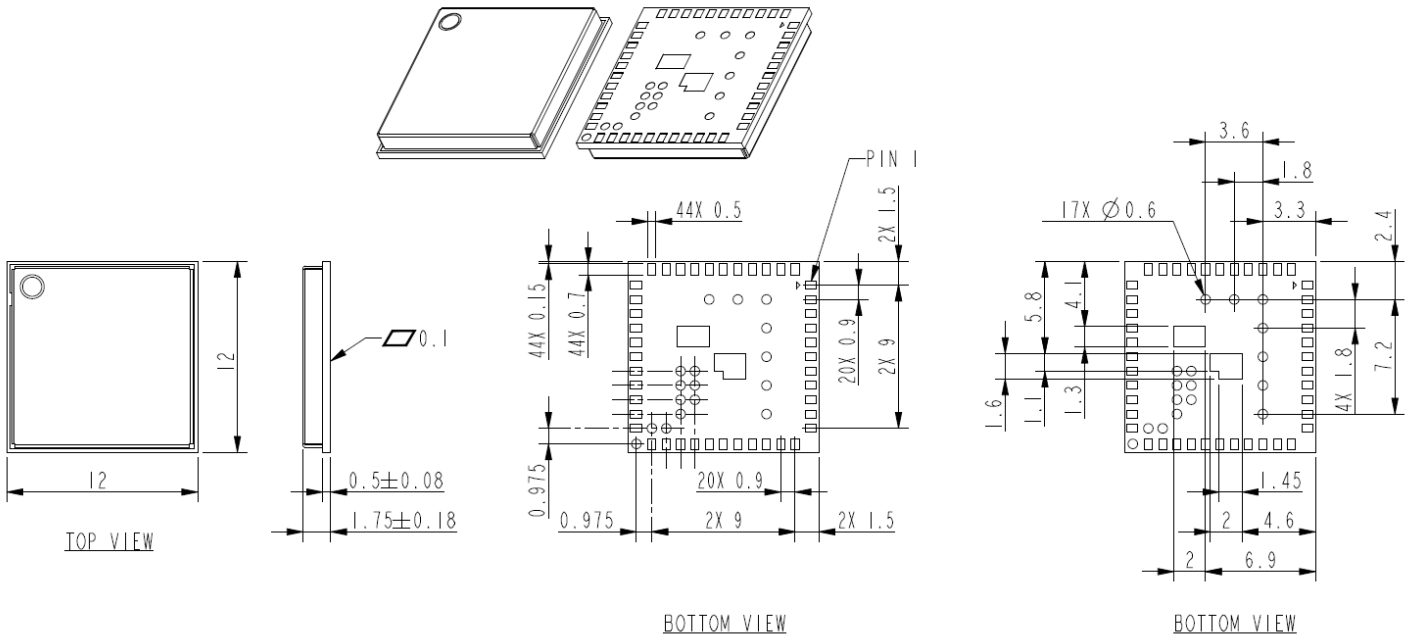
The AW-XM650 requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed in below table must be used.

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	Ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300 mV,	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance[12]	> 100k	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10,000	Ppm

[12] When power is applied or switched off.

4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

5. Packaging Information

TBD