AW-XM632-SURX

IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6E

+ Bluetooth 5.3 Combo Module

Datasheet

Rev.A

DF

(For Standard)

Features

Wi-Fi

- 802.11a/b/g/n/ac/ax compliant, tri-band capable (2.4/5/6 GHz).
- 5/6 GHz: 20/40/80-MHz channels, 1024-QAM, 1×1 providing up to 600 Mbps PHY data rate.
- 2.4 GHz: 20/40[1]-MHz channels, 1024-QAM, 1×1 providing up to 287 Mbps PHY date rate.
- 802.11ax STA mode and Soft AP mode with 11ax scheduled access.
- Supports 802.11d, h, k, r, v, w, ai.
- On-chip power amplifiers and low-noise amplifiers.
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE.
- Fast VSDB (Virtual Simultaneous Dual Band).
- Worldwide regulatory support: Global products supported with worldwide homologated design.
- Integrated Arm® Cortex® R4 processor with tightly coupled memory for complete WLAN subsystem functionality. This architecture offloads the host processor completely from WLAN functionality.
- Transmission and reception of HE-SU and HE-ER-SU PPDU.
- Reception of HE-MU PPDU-OFDMA/MU-MIMO Frame.
- Transmission of HE-TB PPDU (Uplink MU OFDMA).

Bluetooth

- Bluetooth 5.3 (BDR + EDR + BLE).
- All Bluetooth 5.0/5.1/5.2 optional features supported including LE-Audio.
- Dedicated Bluetooth® RF path for best Wi-Fi + Bluetooth coexistence performance.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM/I2S for audio data.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- On-chip memory includes 512 KB SRAM and 2 MB ROM.

Interface

- SDIO 2.0/3.0 for WLAN.
- HCI-UART, PCM/I2S for Bluetooth.

Coexistence

- Built-in advanced algorithms for Wi-Fi + Bluetooth coexistence.
- 2-wire SECI for external 3rd party Bluetooth®/GPS/LTE radios.

General

- Fully integrated programmable dynamic Power Management Unit.
- Supports 1.8 V VDDIO.
- Supports 1340 Bytes of OTP shared between Bluetooth and WLAN for storing board parameters.

Revision History

Document NO: R2-2661-DST-02

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2024/08/21	DCN032165	● Initial Version	YuFu Chen	N.C. Chen

Table of Contents

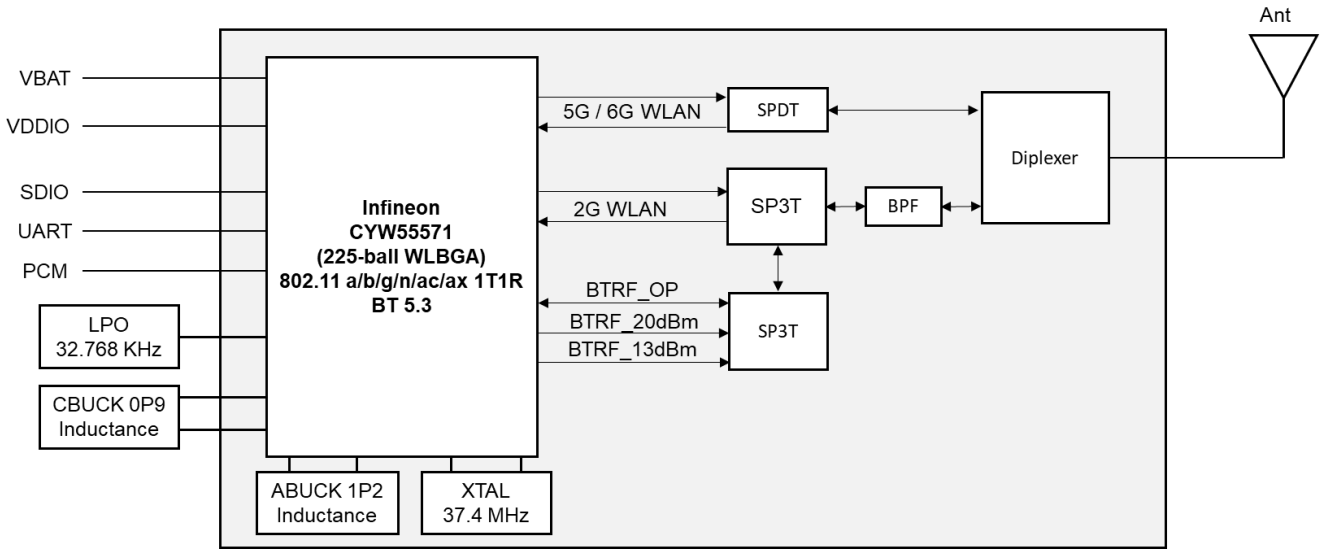
1. Introduction

1.1 Product Overview

The AW-XM632-SURX provides the highest level of integration for Commercial and Consumer IoT wireless systems with integrated tri-band 1x1 IEEE 802.11ax WLAN MAC/baseband/radio, Bluetooth 5.3 MAC/baseband/radio, and integrated Power Management Unit. WLAN and Bluetooth radios also include on-chip power amplifiers and low-noise amplifiers to further reduce the need for external components.

WLAN interfaces to host processor through a SDIO 3.0 interface while Bluetooth host interface is provided through high-speed 4-wire UART interface. Additionally, the Bluetooth section supports PCM and I2S interfaces for audio applications. AW-XM632-SURX is qualified to operate across Industrial (–40°C to +85°C) temperature range.

1.2 Block Diagram



AW-XM632-SURX Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	802.11 a/b/g/n/ac/ax Wi-Fi 6E + Bluetooth 5.3 Combo Module
Major Chipset	Infineon CYW55571 WLBGA
Host Interface	Wi-Fi + BT → SDIO + UART
Dimension	12 mm x 12 mm x 1.8 mm
Form factor	LGA, 47 pins
Antenna	Tri-band 1x1 ANT : Wi-Fi/Bluetooth → TX/RX
Weight	TBD

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	WLAN: 2.4 / 5 / 6 GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9), 1024-QAM(MCS10~11)
Number of Channels	**2.4GHz** ● USA, Canada and Taiwan – 1 ~ 11 ● China, Most European Countries – 1 ~ 13 ● Japan, 1 ~ 13 **5GHz** ● USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165 **6GHz** ● CH1~CH233

Output Power[1,2]
(Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<8%	16	18	20	dBm
11g (54Mbps) @EVM≦-25 dB	15	17	19	dBm
11n (HT20 MCS7) @EVM≦-27 dB	14.5	16.5	18.5	dBm
11ax (HE20 MCS11) @EVM≦-35 dB	12	14	16	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM<-25 dB	14	16	18	dBm
11n (HT20 MCS7) @EVM≦-27 dB	14	16	18	dBm
11n (HT40 MCS7) @EVM≦-27 dB	14	16	18	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	13.5	15.5	17.5	dBm
11ac (VHT40 MCS9) @EVM≦-32 dB	12.5	14.5	16.5	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	12	14	16	dBm
11ax (HE20 MCS11) @EVM≦-35 dB	12.5	14.5	16.5	dBm
11ax (HE40 MCS11) @EVM≦-35 dB	12	14	16	dBm
11ax (HE80 MCS11) @EVM≦-35 dB	11.5	13.5	15.5	dBm

6G

	Min	Typ	Max	Unit
11ax (HE20 MCS11) @EVM≦-35 dB	10	12	14	dBm
11ax (HE40 MCS11) @EVM≦-35 dB	9	11	13	dBm
11ax (HE80 MCS11) @EVM≦-35 dB	8	10	12	dBm

[1] Unless otherwise stated, limit values apply for an ambient temperature of +25 °C.
[2] Tx power variation ±3.0 dB for process, voltage and temperature variation across –40°C to +85°C.

Receiver Sensitivity**

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		88	85	dBm
11g (54Mbps)		76	73	dBm
11n (HT20 MCS7)		74	71	dBm
11ax (HE20 MCS11)		63	60	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		74	71	dBm
11n (HT20 MCS7)		72	69	dBm
11n (HT40 MCS7)		69	66	dBm
11ac (VHT20 MCS8)		67	64	dBm
11ac (VHT40 MCS9)		63	60	dBm
11ac (VHT80 MCS9)		60	57	dBm
11ax (HE20 MCS11)		60	57	dBm
11ax (HE40 MCS11)		56	53	dBm
11ax (HE80 MCS11)		55	52	dBm

6G

	Min	Typ	Max	Unit
11ax (HE20 MCS11)		56	53	dBm
11ax (HE40 MCS11)		54	51	dBm
11ax (HE80 MCS11)		52	49	dBm

Data Rate

802.11b: 1, 2, 5.5, 11Mbps
802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n: MCS0~7 HT20/HT40
802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11ac: MCS0~8 VHT20
802.11ac: MCS0~9 VHT40/VHT80
802.11ax: MCS10~11 HE20/HE40/HE80

Security

- WEP
- WPA/WPA2/WPA3 Enterprise with 192-bit encryption
- WMM, WMM-PS (U-APSD), WMM-SA
- AES (hardware accelerator),
- TKIP (hardware accelerator)
- CKIP (software support)

*** If you have any certification questions about output power please contact FAE directly**
**** Project is in engineering stage, RF performance is still being verified.**

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 5.3</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2400~2483.5MHz</td></tr>
<tr><td>Modulation</td><td>GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)</td></tr>
<tr><td>Output Power*</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>3</td><td>6</td><td>9</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td>3</td><td>6</td><td>9</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity**</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td></td><td>-90</td><td>-87</td><td>dBm</td></tr>
<tr><td>EDR</td><td></td><td>-86</td><td>-83</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td></td><td>-92</td><td>-89</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

*** If you have any certification questions about output power please contact FAE directly**
**** Project is in engineering stage, RF performance is still being verified.**

1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V
Operating Temperature	-40℃ to 85℃
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃ to 125℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

1.4 Frequency references

1.4.1 External 32.768 kHz sleep clock specifications

AW-XM632-SURX requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed must be used.

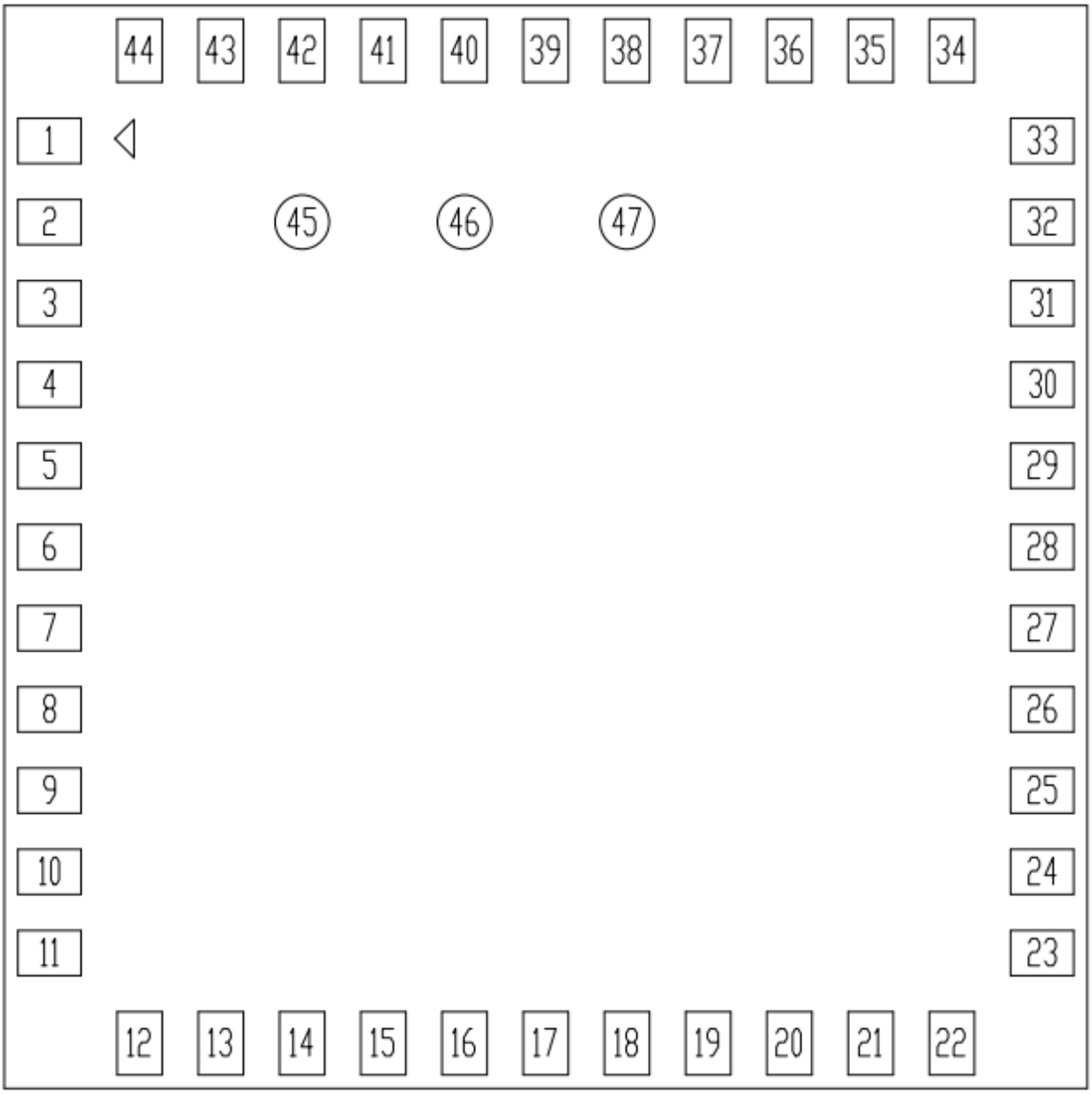
External 32.768 kHz sleep clock specifications

Parameter	LPO clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30 – 70	%
Input signal amplitude	200–1800	mV, p–p
Signal type	Square-wave or sine-wave	-
Input impedance[1]	> 100k	Ω
Clock jitter[2] (during initial startup)	< 5	pF
	< 10,000	ppm

Notes:
1. When power is applied or switched off.
2. The LPO_IN input receiver has ac-coupled capacitance on the input with the feedback resistor to maintain the common mode around VDDIO/2 and power supply noise should be maintained less than 100mV to avoid any false glitches before the time constant (ac- coupled capacitance * feedback resistor, i.e., 100 µs) settles down.

2. Pin Definition

2.1 Pin Map



AW-XM632-SURX Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.	-	GND
2	ANT	WLAN/BT RF ANT.		RF
3	GND	Ground.	-	GND
4	NC	Floating	-	-
5	GND	Ground.	-	GND
6	BT_DEV_WAKE	Bluetooth DEVICE WAKE.	VDDIO	I/O
7	BT_HOST_WAKE	Bluetooth HOST WAKE.	-	I/O
8	NC	Floating	-	-
9	VBAT	3.3V power pin.	3.3V	PWR
10	NC		-	-
11	NC		-	-
12	WL_REG_ON	Used by the PMU to power up or power down the internal AW-XM632-SURX regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 KΩ pull-down resistor that is auto enabled/disabled by programming.	VDDIO	I
13	WL_HOST_WAKE	WLAN HOST_WAKE.	VDDIO	I/O
14	SDIO_DATA_2	SDIO data line 2	-	I/O
15	SDIO_DATA_3	SDIO data line 3	-	I/O
16	SDIO_DATA_CMD	SDIO command line	-	I/O
17	SDIO_DATA_CLK	SDIO Clock Input	-	I
18	SDIO_DATA_0	SDIO data line 0	-	I/O
19	SDIO_DATA_1	SDIO data line 1	-	I/O
20	GND	Ground.	-	GND
21	CSR_VLX	CSR Power Stage Output to Inductor.	0.9V	O
22	VDDIO	1.8 V IO Supply for WLAN GPIOs.	1.8V	PWR
23	CBUCK_0P9	Internal Buck 0.9V voltage generation pin.	0.9V	I

24	LPO_IN	External Sleep Clock Input (32.768 kHz)	-	I
25	BT_PCM_OUT	PCM data output.	VDDIO	O
26	BT_PCM_CLK	PCM clock	VDDIO	I/O
27	BT_PCM_IN	PCM data input.	VDDIO	I
28	BT_PCM_SYNC	PCM sync signal	VDDIO	I/O
29	NC	Floating	-	-
30	NC	Floating	-	-
31	GND	Ground.	-	GND
32	NC	Floating	-	-
33	GND	Ground.	-	GND
34	BT_REG_ON	Used by the PMU to power up or power down the internal regulators used by the Bluetooth® section. When deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.	VDDIO	I
35	GPIO_2	WLAN General Purpose I/O	VDDIO	I/O
36	GND	Ground.	-	GND
37	WL_DEV_WAKE	WL_DEV_WAKE	VDDIO	I/O
38	GPIO_3	WLAN General Purpose I/O	VDDIO	I/O
39	GPIO_4	WLAN General Purpose I/O	VDDIO	I/O
40	GPIO_5	WLAN General Purpose I/O	VDDIO	I/O
41	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	VDDIO	O
42	BT_UART_TXD	UART Serial Output. Serial data output for the HCI UART interface.	VDDIO	O
43	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	VDDIO	I
44	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	VDDIO	I
45	BT_GPIO_2	Bluetooth General Purpose I/O	VDDIO	I/O
46	NC	Floating	-	-
47	NC	Floating	-	-

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	-0.5	-	6.0	V
VDDIO	DC supply voltage for digital I/O	-0.5	-	2.2	V
T_j	Maximum junction temperature	-	-	125	°C

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulator	3.13	3.3	3.47	V
VDDIO	DC supply voltage for digital I/O	1.71	1.8	1.89	V

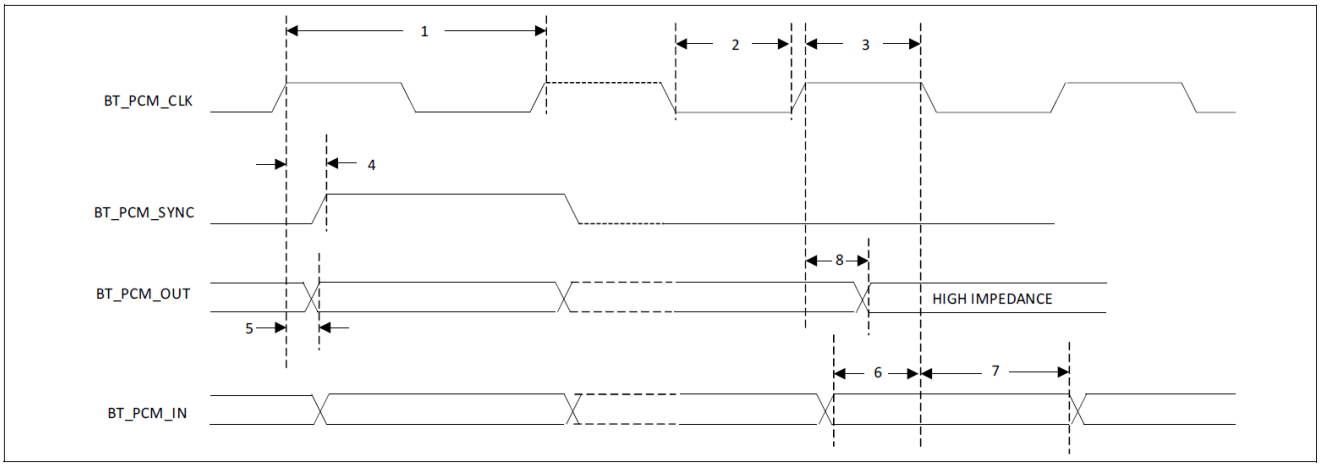
3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital I/O pins, VDDIO=1.8V					
V_{IH}	Input high voltage	0.65 × VDDIO	-	-	V
V_{IL}	Input low voltage	-	-	0.35 × VDDIO	V
V_{OH}	Output high voltage	VDDIO – 0.40	-	-	V
V_{OL}	Output Low Voltage	-	-	0.45	V
WL_REG_ON & BT_REG_ON Pins					
-	Input high voltage	1.2	-	VBAT	-
-	Input low voltage	-	-	0.3	-

3.4 Host Interface

3.4.1 PCM Interface Timing

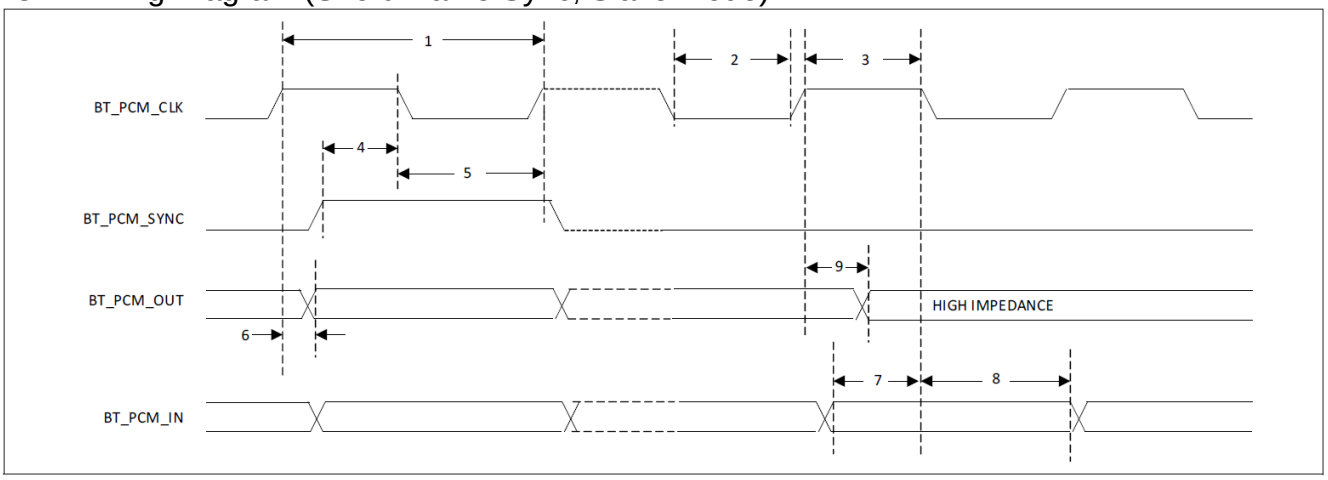
■ PCM Timing Diagram (Short Frame Sync, Master Mode)



PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

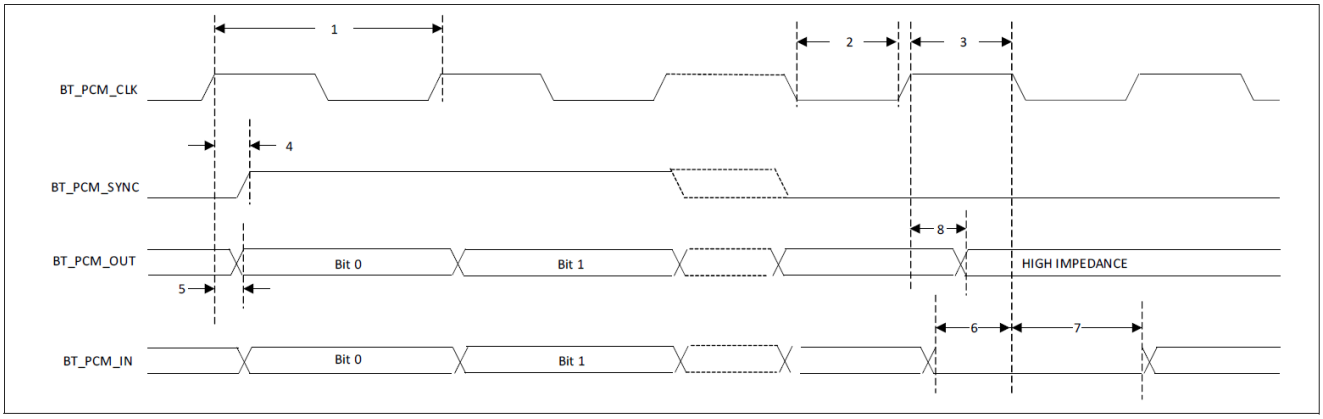
■ PCM Timing Diagram (Short Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

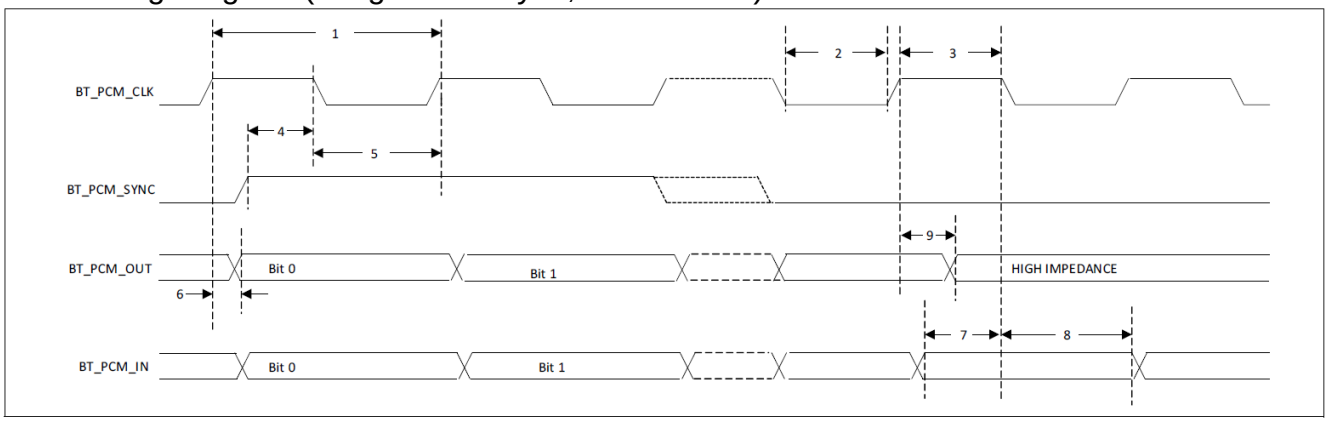
■ PCM Timing Diagram (Long Frame Sync, Master Mode)



PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

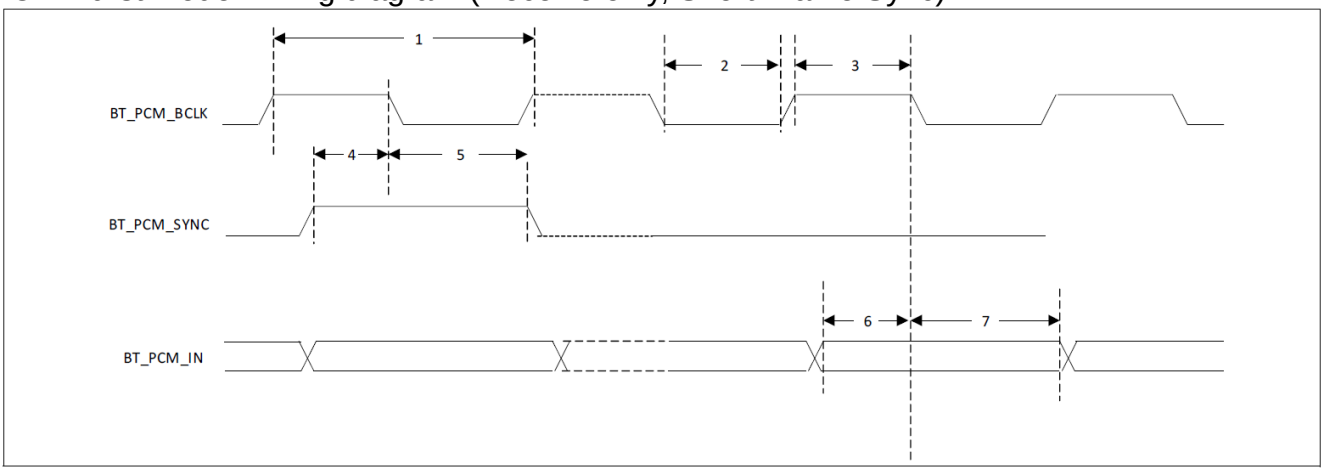
■ PCM Timing Diagram (Long Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

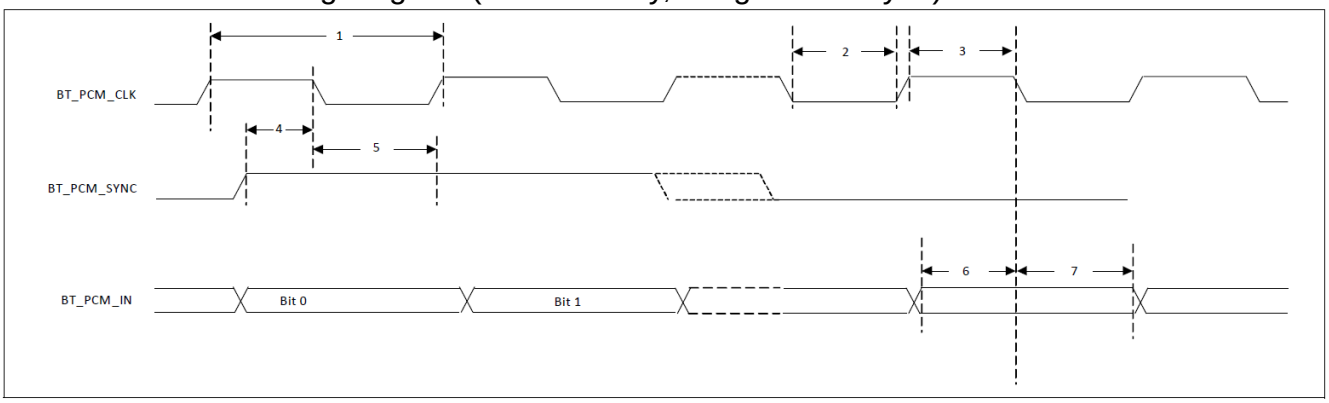
■ PCM Burst Mode Timing diagram (Receive only, Short Frame Sync)



PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

■ PCM Burst Mode Timing diagram (Receive only, Long Frame Sync)



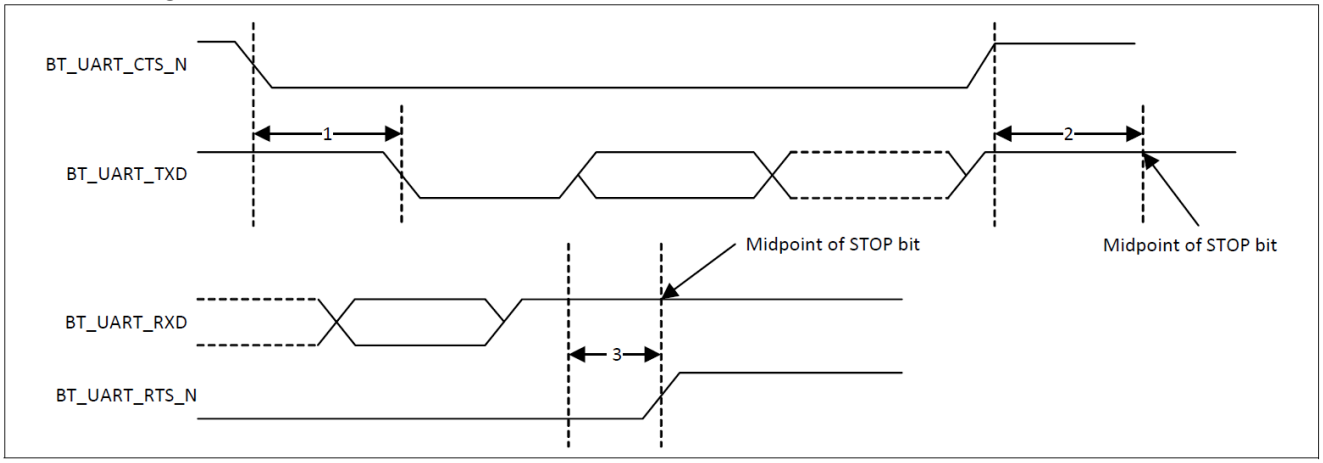
PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

3.4.2 UART Interface

The AW-XM632-SURX UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The baud rate may be selected through a vendor-specific UART HCI command. UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.0 UART HCI specification. The default baud rate is 115.2 Kbaud.
The AW-XM632-SURX UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.
Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-XM632-SURX UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

■ UART Timing

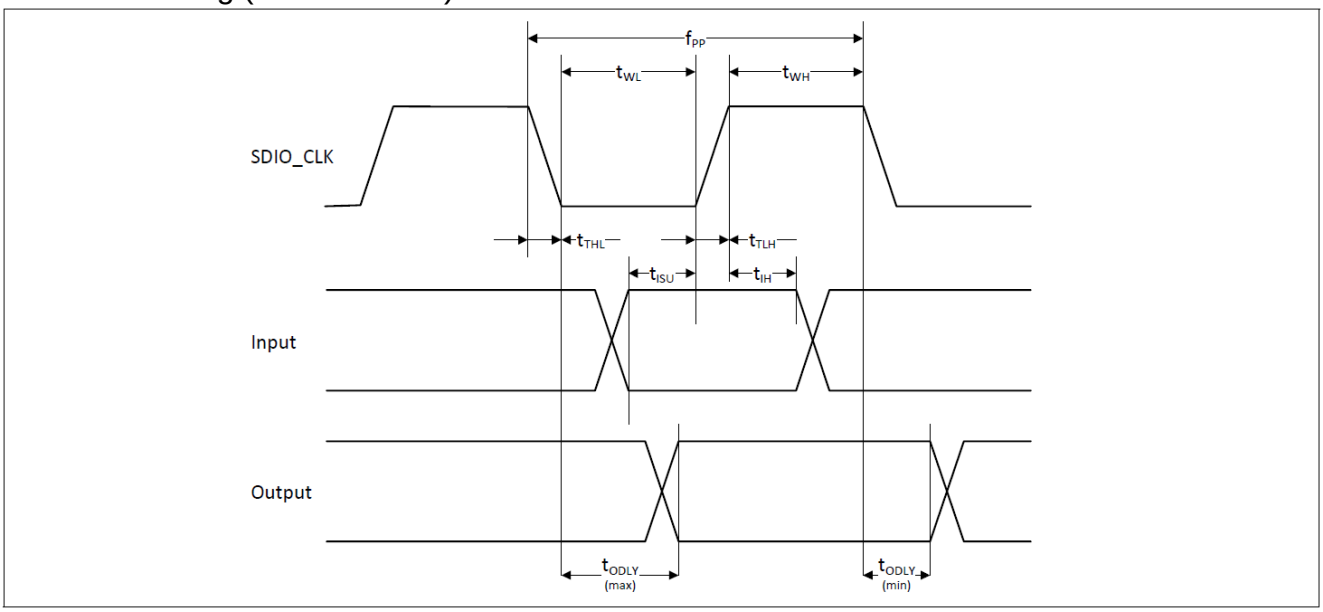


UART Timing specifications

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

3.4.3 SDIO Interface

■ SDIO Bus Timing (Default Mode)



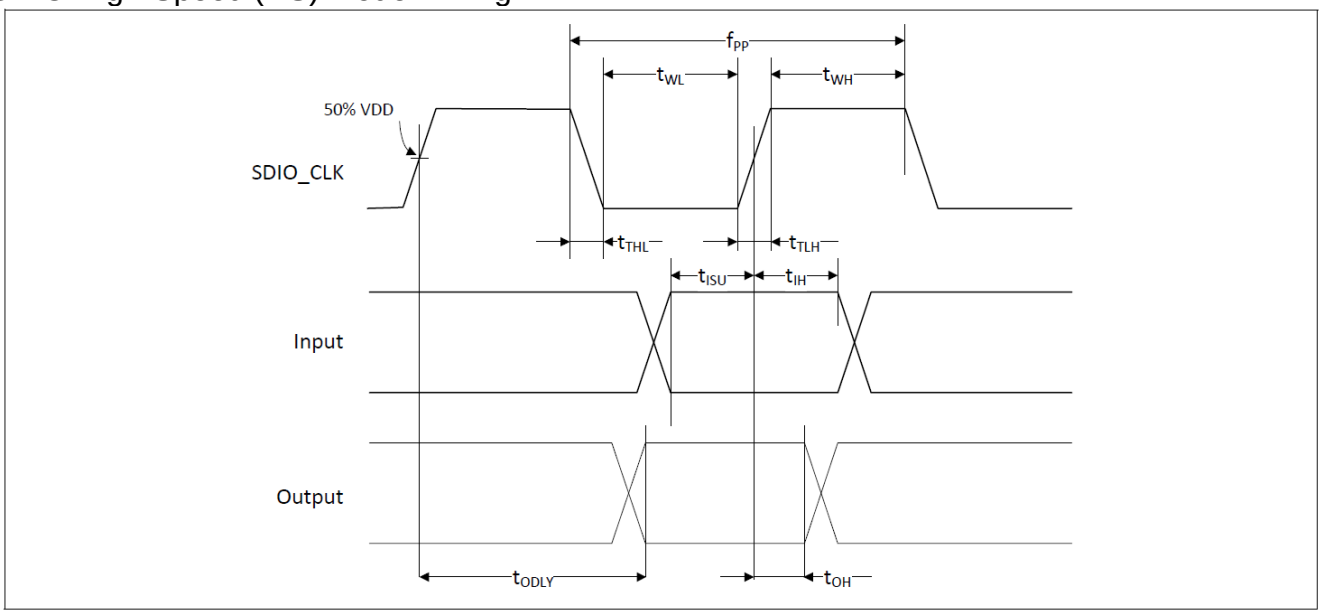
SDIO Bus Timing[1] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns

Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

Notes:
1. Timing is based on CL *f* ≤ 40 pF load on CMD and Data..
2. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

■ SDIO High-Speed (HS) Mode Timing



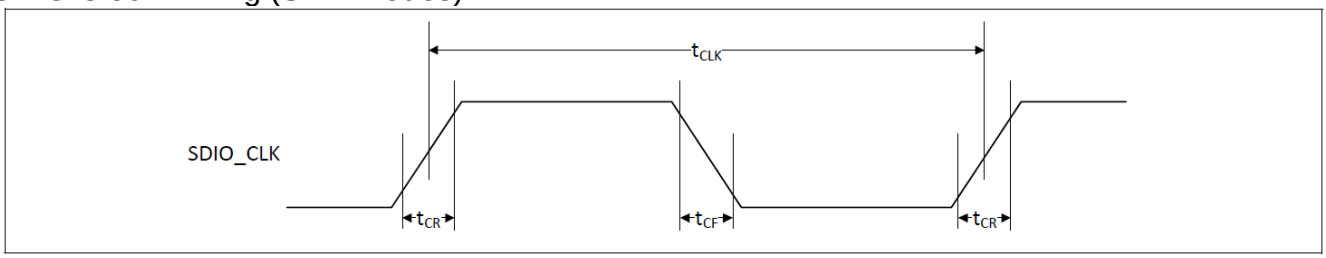
SDIO Bus Timing[1] parameters (HS Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns

Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

Notes:
1. Timing is based on CL f ≤ 40 pF load on CMD and Data.
2. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

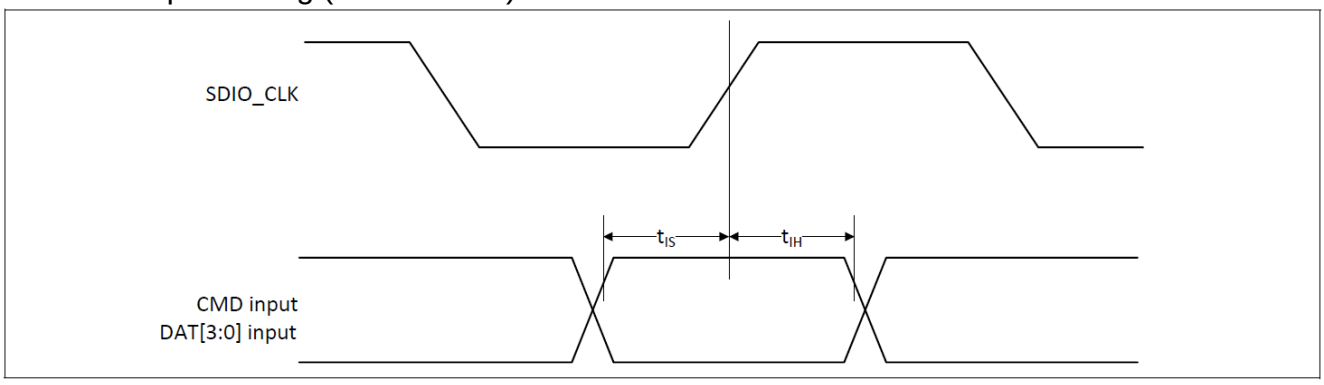
■ SDIO Clock Timing (SDR Modes)



SDIO Bus Clock Timing parameters (SDR Modes)

Parameter	Symbol	Minimum	Typical	Unit	Comments
–	t_{CLK}	40.0	–	ns	SDR12 mode
		20.0	–	ns	SDR25 mode
		10.0	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, CCARD = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, CCARD = 10 pF
Clock duty	–	30.0	70.0	%	–

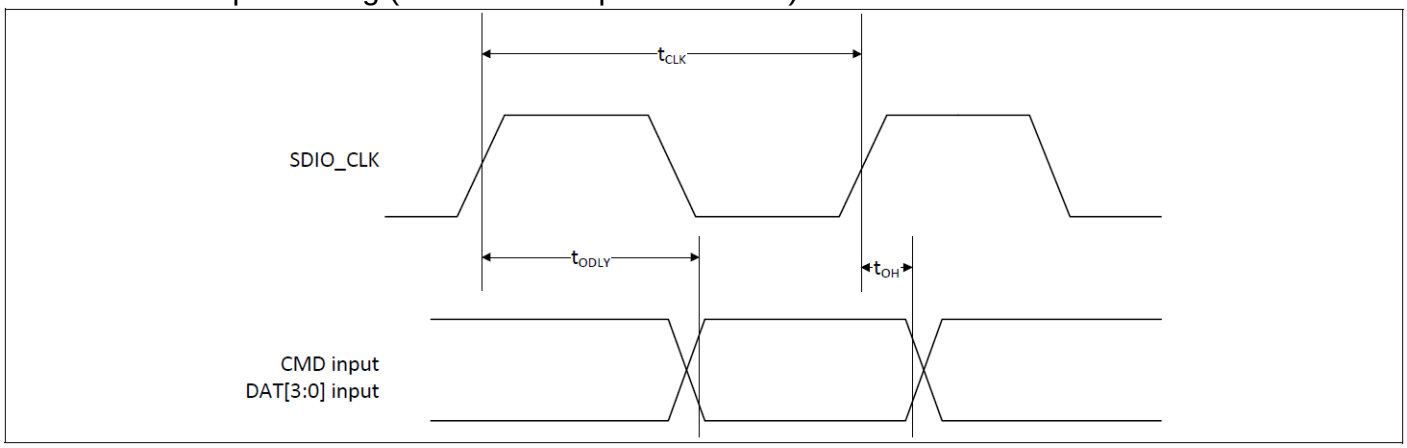
■ SDIO Bus Input Timing (SDR Modes)



SDIO Bus Input Timing parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975 V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975 V

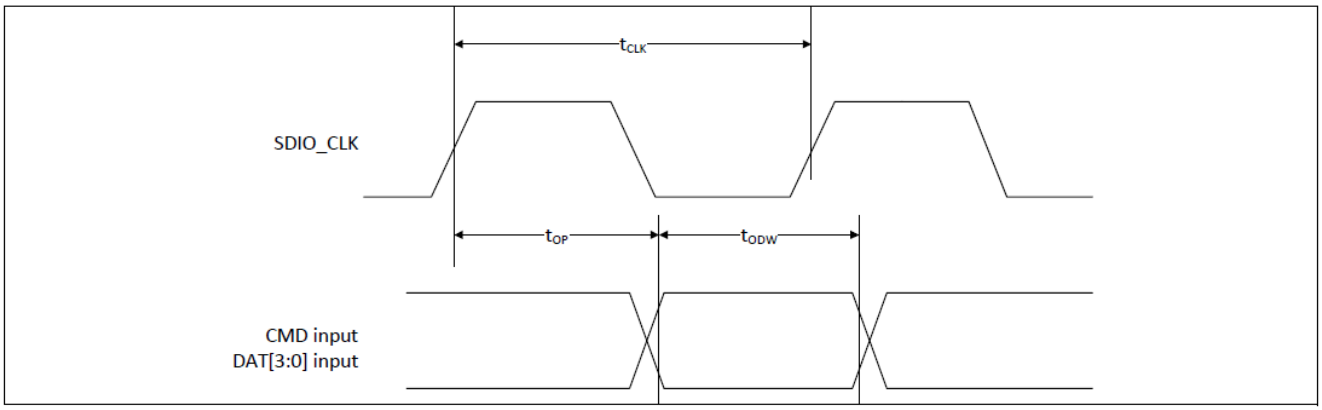
■ SDIO Bus Output Timing (SDR Modes up to 100 MHz)



SDIO Bus Output Timing parameters (SDR Modes up to 100 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq$ 10 ns CL= 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq$ 20 ns CL= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) CL= 15 pF

■ SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

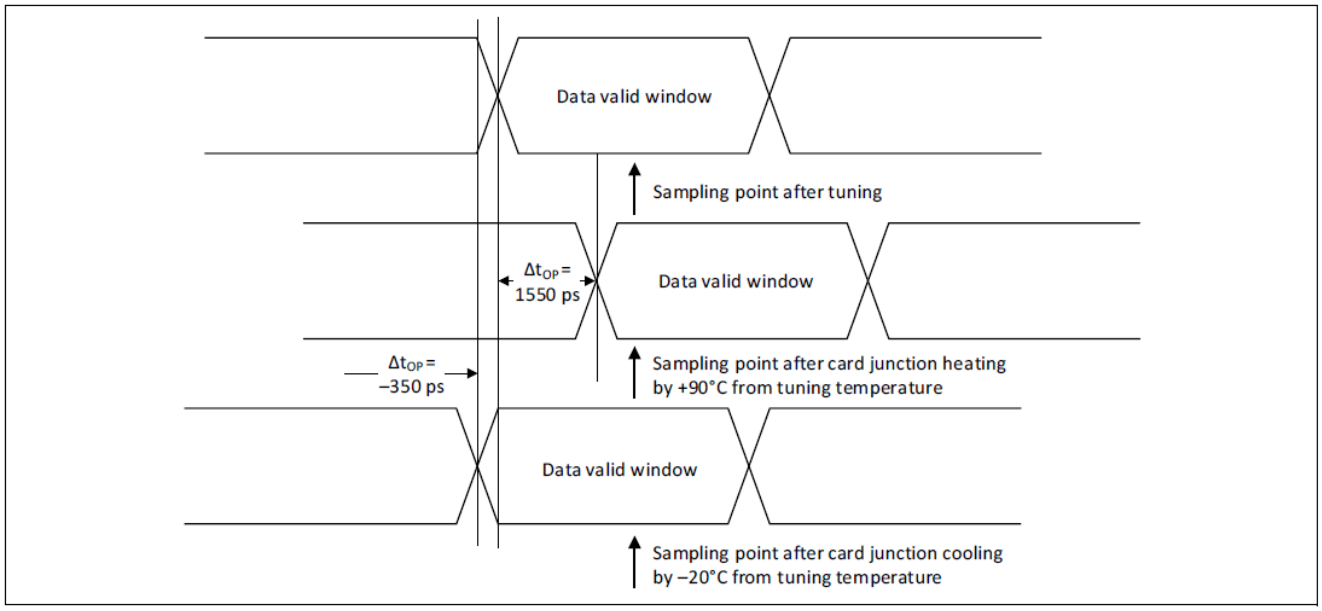


SDIO Bus Output Timing parameters (SDR Modes 100 MHz to 208 MHz)

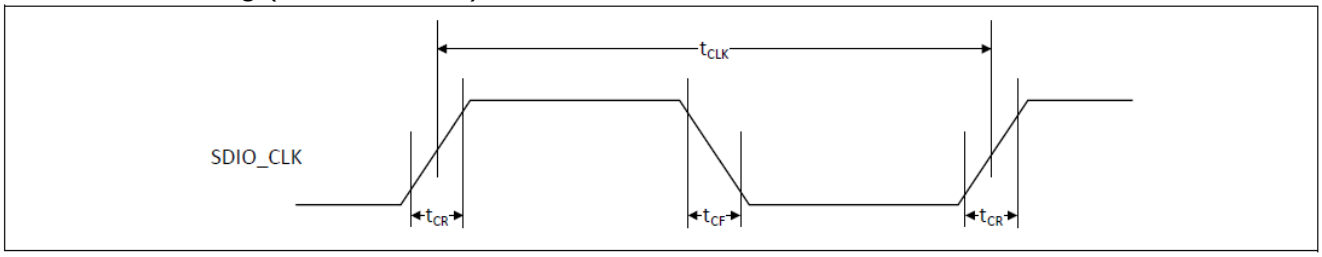
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2.0	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
Δt_{OP} = -350 ps for junction temperature of Δt_{OP} = -20 degrees during operation
Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = -20 to +125 degrees during operation

■ △tOP Consideration for Variable Data Window (SDR 104 Mode)



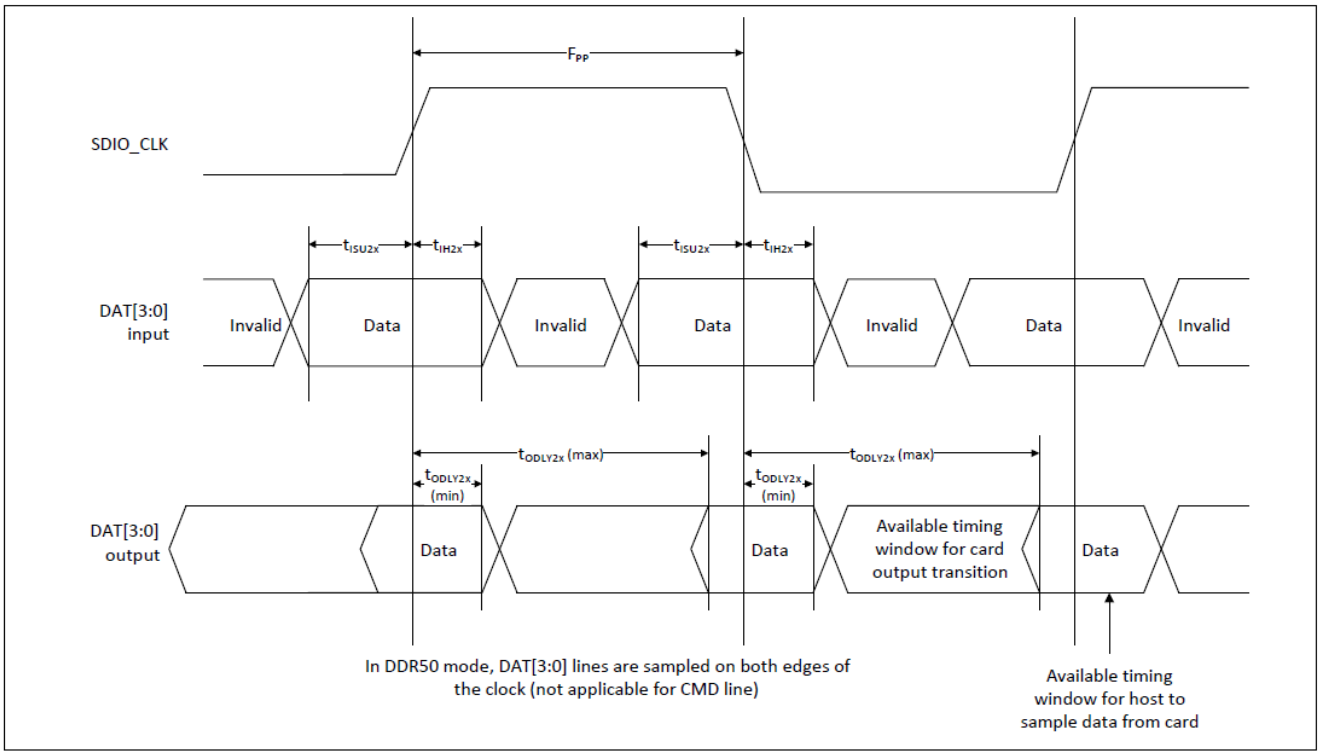
■ SDIO Clock Timing (DDR50 Mode)



SDIO Bus Clock Timing parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20.0	–	ns	DDR50 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45.0	55.0	%	–

■ SDIO Data Timing (DDR50 Mode)



SDIO Bus Timing parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6.0	–	ns	CCARD < 10pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	CCARD < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–		ns	CCARD < 30pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	CCARD < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3.0	–	ns	CCARD < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	CCARD < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	CCARD < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	CCARD < 15pF (1 Card)

3.5 Power up Timing Sequence

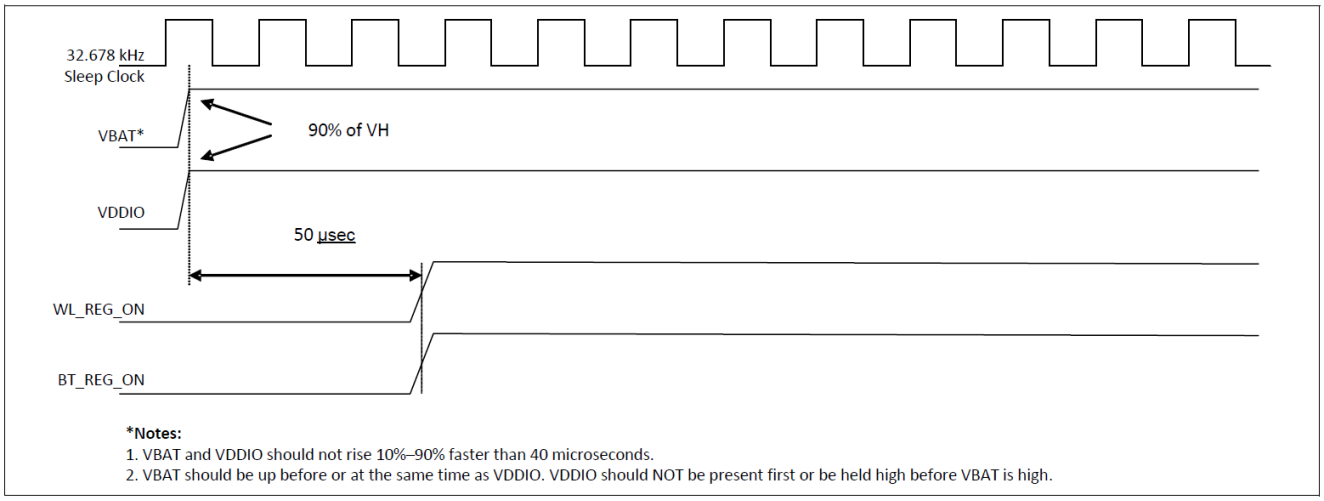
AW-XM632-SURX has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

3.5.1 Description of Control Signals

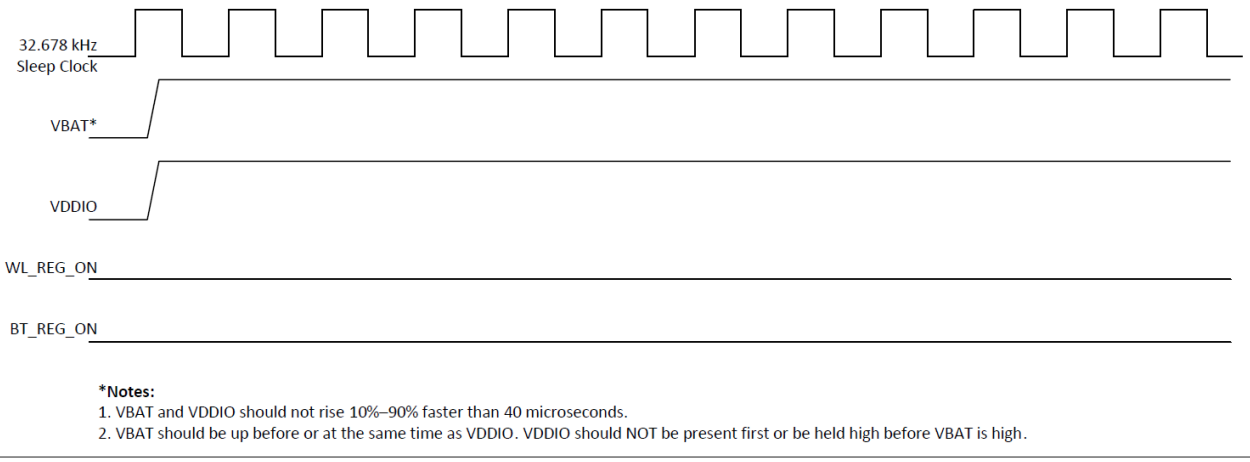
■ WL_REG_ON: Used by the PMU to power up the WLAN section. It is also OR–gated with the BT_REG_ON input to control the internal AW-XM632-SURX regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
■ BT_REG_ON: Used by the PMU (OR–gated with WL_REG_ON) to power up the internal AW-XM632-SURX regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the Bluetooth section is in reset.
■ Note
VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.

3.5.2 Control Signal Timing Diagrams

■ WLAN = ON, Bluetooth = ON

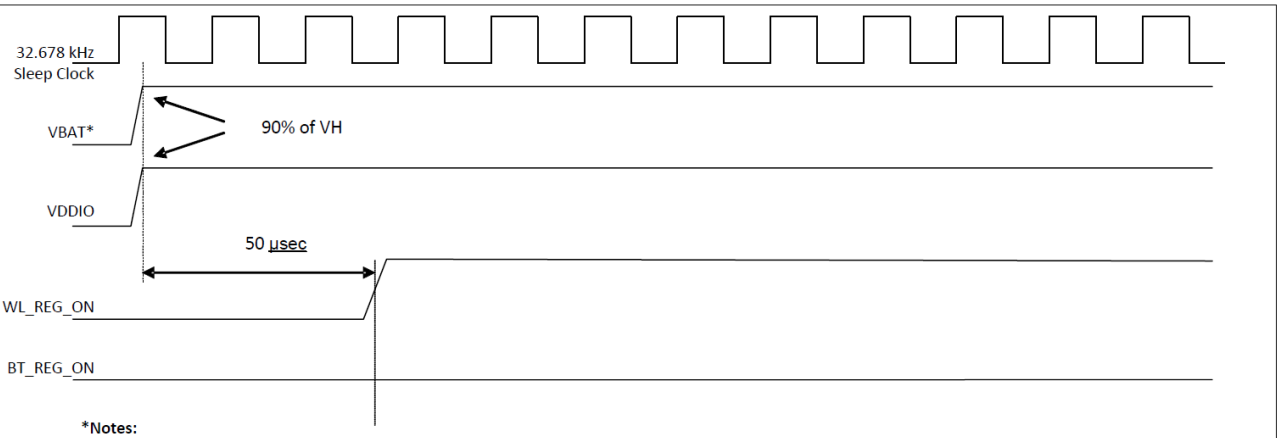


■ WLAN = OFF, Bluetooth = OFF



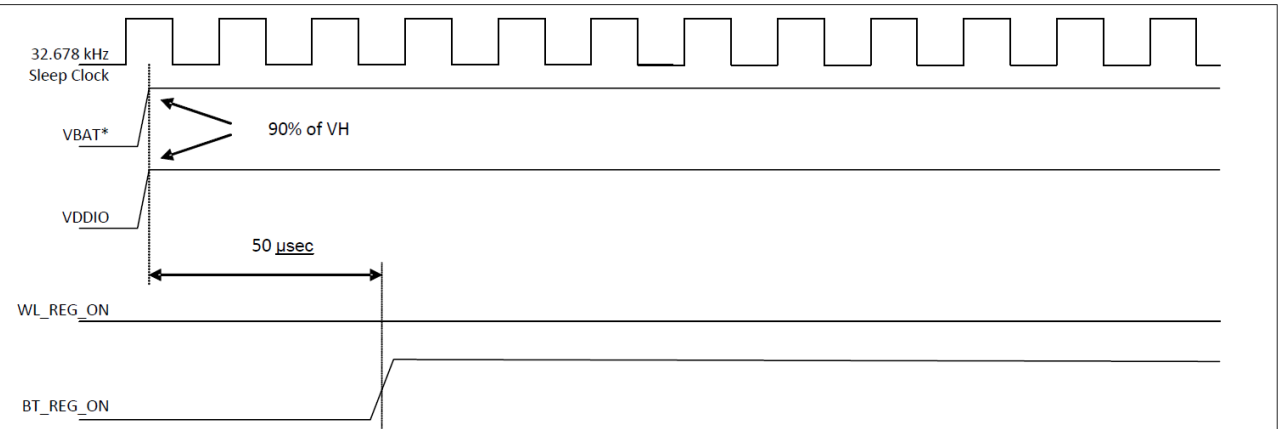
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

■ WLAN = ON, Bluetooth = OFF



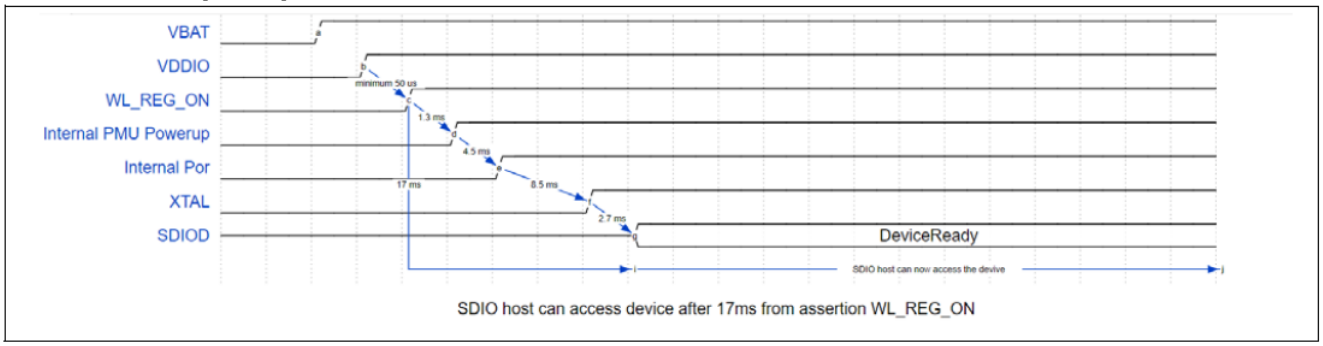
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

■ WLAN = OFF, Bluetooth = ON

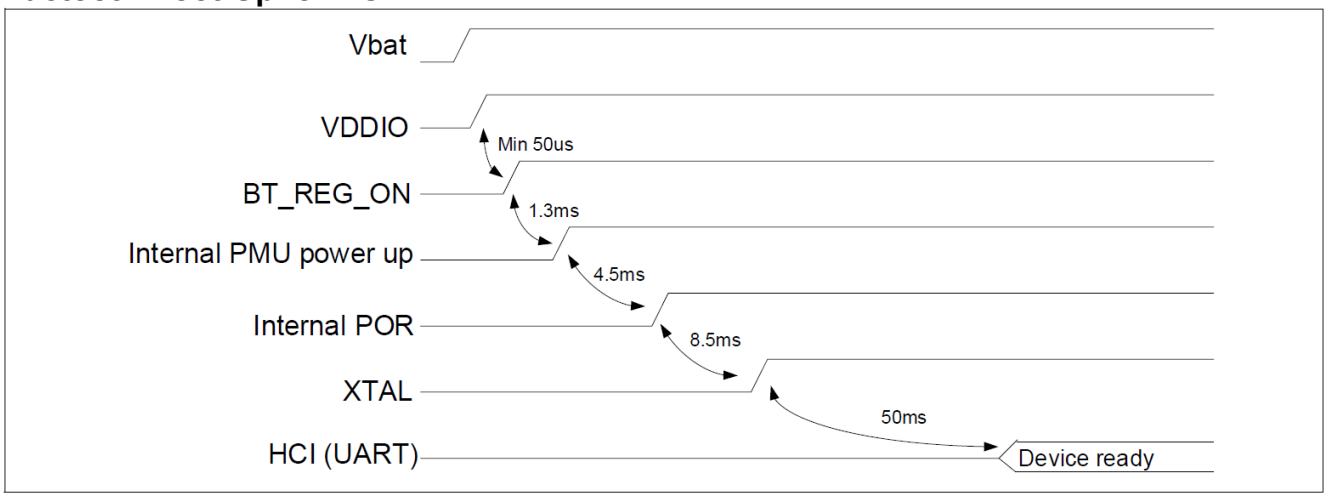


***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

■ WLAN Boot-Up Sequence for SDIO Host



■ Bluetooth Boot-Up for HCI



3.6 Power Consumption*

3.6.1 WLAN

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

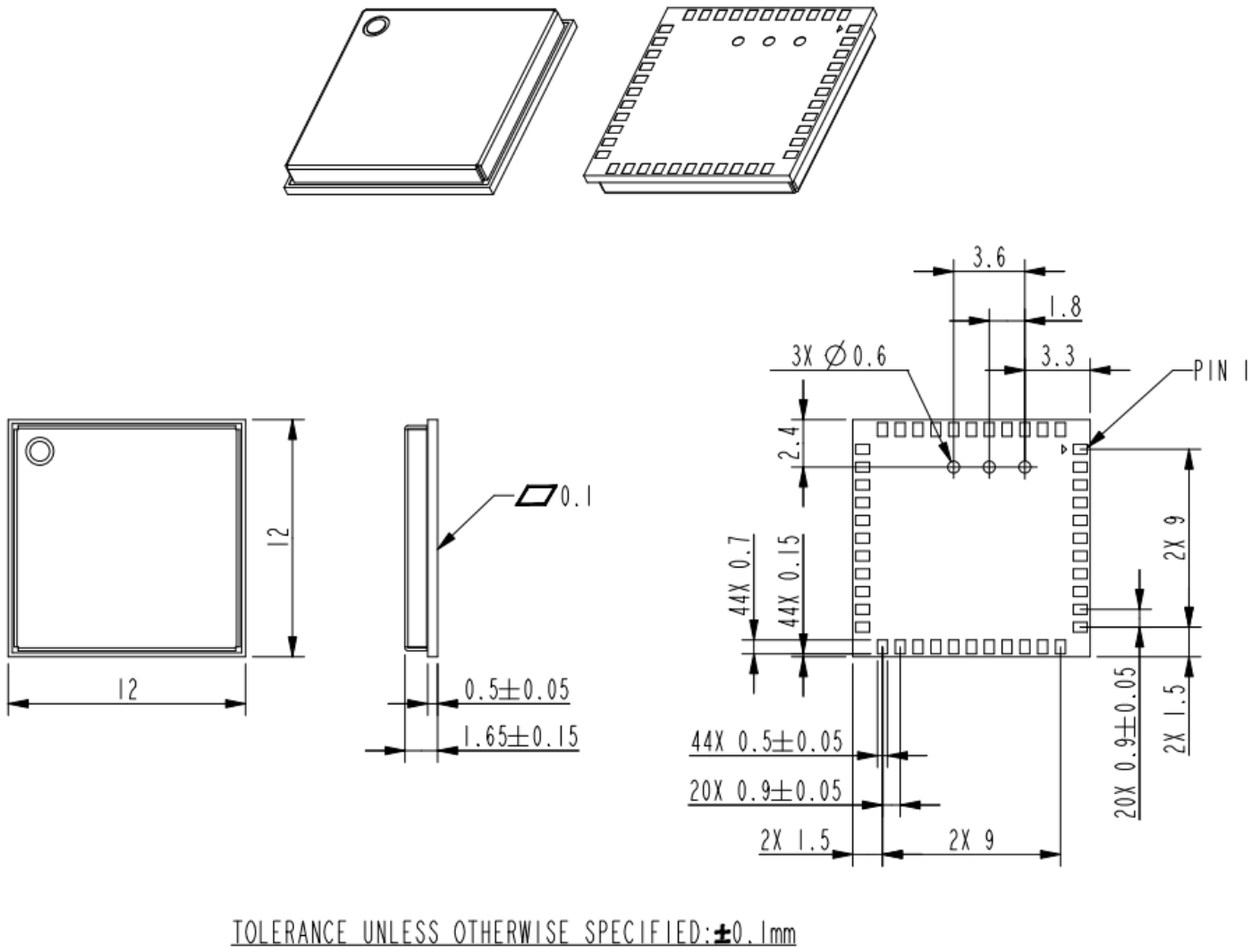
3.6.2 Bluetooth

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

5. Packaging Information

TBD