# AW-XM632-PUR

## IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6E

## + Bluetooth 6.0 Combo Module

## Datasheet

**Rev.C**

**DF**

**(For Standard)**



FORM NO.: FR2-015_ A Responsible Department：WBU Expiry Date: Forever
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# Features

## Wi-Fi

- 802.11a/b/g/n/ac/ax compliant, tri-band capable (2.4/5/6 GHz).
- 5/6 GHz: 20/40/80-MHz channels, 1024-QAM, 1×1 providing up to 600 Mbps PHY data rate.
- 2.4 GHz: 20/40[1]-MHz channels, 1024-QAM, 1×1 providing up to 287 Mbps PHY date rate.
- 802.11ax STA mode and Soft AP mode with 11ax scheduled access.
- Supports 802.11d, h, k, r, v, w, ai.
- On-chip power amplifiers and low-noise amplifiers.
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE.
- Fast VSDB (Virtual Simultaneous Dual Band).
- Worldwide regulatory support: Global products supported with worldwide homologated design.
- Integrated Arm® Cortex® R4 processor with tightly coupled memory for complete WLAN subsystem functionality. This architecture offloads the host processor completely from WLAN functionality.
- Transmission and reception of HE-SU and HE-ER-SU PPDU.
- Reception of HE-MU PPDU-OFDMA/MU-MIMO Frame.
- Transmission of HE-TB PPDU (Uplink MU OFDMA).

## Bluetooth

- Bluetooth 6.0 (BDR + EDR + BLE).
- All Bluetooth 5.0/5.1/5.2 optional features supported including LE-Audio.
- Supports ISOAL HCI Enhancement (6.0) to enhance low latency and high reliable audio.
- Dedicated Bluetooth® RF path for best Wi-Fi + Bluetooth coexistence performance.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM/I2S for audio data.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- On-chip memory includes 512 KB SRAM and 2 MB ROM.

## Interface

- PCIe Gen2 (3.0 Compliant) for WLAN: complies with PCI Express base specification revision 3.0 for ×1 lane and power management running at Gen2 speeds.
- HCI-UART, PCM/I2S for Bluetooth.

## Coexistence

- Built-in advanced algorithms for Wi-Fi + Bluetooth coexistence.
- 2-wire SECI for external 3rd party Bluetooth®/GPS/LTE radios.

## General

- Fully integrated programmable dynamic Power Management Unit.
- Supports 1.8 V VDDIO.



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- Supports 1340 Bytes of OTP shared between Bluetooth and WLAN for storing board parameters.


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# Revision History

Document NO: R2-2632-DST-01

| Version | Revision Date | DCN NO. | Description | Initials | Approved |
|---|---|---|---|---|---|
| A | 2024/01/18 | DCN030965 | • Initial Version | YuFu Chen | N.C. Chen |
| B | 2024/07/19 | DCN031976 | • Change model name<br>• Added RF specifications | YuFu Chen | N.C. Chen |
| C | 2025/03/04 | DCN033614 | • Updated Bluetooth certified version<br>• Updated Module Weight<br>• Updated ESD Specification<br>• Updated Power Consumption<br>• Updated Packaging Information | YuFu Chen | N.C. Chen |
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# Table of Contents




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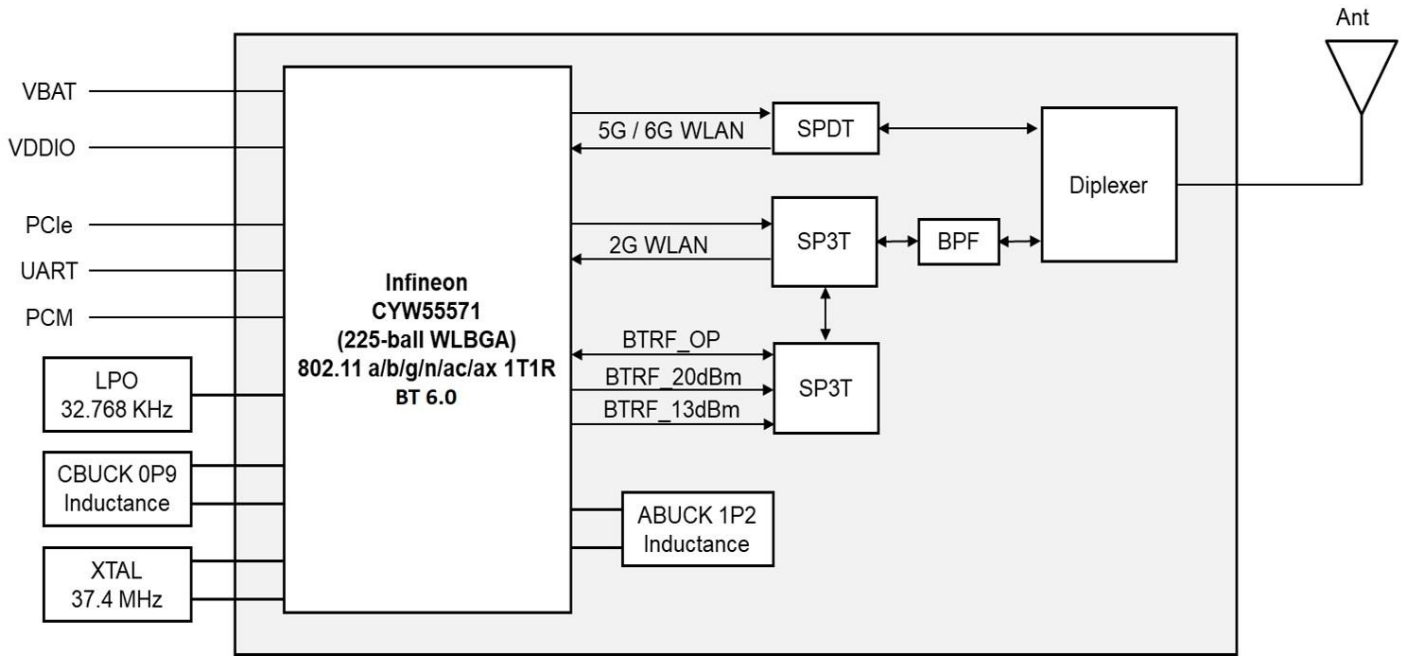
# 1. Introduction

## 1.1 Product Overview

The AW-XM632-PUR device provides the highest level of integration for commercial and Industrial IoT wireless systems with integrated tri-band 1x1 Wi-Fi 6E WLAN MAC/baseband/radio, Bluetooth 6.0 MAC/baseband/radio, and integrated Power Management Unit. WLAN and Bluetooth radios also include on-chip power amplifiers and low-noise amplifiers to further reduce the need for external components.

WLAN interfaces to host processor through a PCIe v3.0 Gen2 interface while Bluetooth host interface is provided through high-speed 4-wire UART interface. Additionally, the Bluetooth section supports PCM and I2S interfaces for audio applications. AW-XM632-PUR is qualified to operate across Industrial (–40°C to +85°C) temperature.

## 1.2 Block Diagram




**AW-XM632-PUR Block Diagram**





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## 1.3 Specifications Table

### 1.3.1 General

| Features | Description |
|---|---|
| **Product Description** | 802.11 a/b/g/n/ac/ax Wi-Fi 6E + Bluetooth 6.0 Combo Module |
| **Major Chipset** | Infineon CYW55571 WLBGA |
| **Host Interface** | Wi-Fi + BT → PCIe + UART |
| **Dimension** | 12 mm x 12 mm x 1.93 mm |
| **Form factor** | LGA, 49 pins |
| **Antenna** | Tri-band 1x1<br>ANT : Wi-Fi/Bluetooth → TX/RX |
| **Weight** | 0.6 (g) |

### 1.3.2 WLAN

| Features | Description |
|---|---|
| **WLAN Standard** | IEEE 802.11 a/b/g/n/ac/ax |
| **WLAN VID/PID** | N/A |
| **WLAN SVID/SPID** | N/A |
| **Frequency Rage** | WLAN: 2.4 / 5 / 6 GHz Band |
| **Modulation** | DSSS<br>DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps)<br>OFDM<br>BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2),<br>16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7),<br>256-QAM(MCS8~9), 1024-QAM(MCS10~11) |
| **Number of Channels** | **2.4GHz**<br>● USA, Canada and Taiwan – 1 ~ 11<br>● China, Most European Countries – 1 ~ 13<br>● Japan, 1 ~ 13<br>**5GHz**<br>● USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165<br>**6GHz**<br>● CH1~CH233 |


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**Output Power**[1]
**(Board Level Limit)****

**2.4G**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 11b (11Mbps) @EVM<35% | 16 | 18 | 20 | dBm |
| 11g (54Mbps) @EVM≦-25 dB | 15 | 17 | 19 | dBm |
| 11n (HT20 MCS7) @EVM≦-27 dB | 14.5 | 16.5 | 18.5 | dBm |
| 11ax (HE20 MCS11) @EVM≦-35 dB | 12 | 14 | 16 | dBm |

**5G**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 11a (54Mbps) @EVM<-25 dB | 14 | 16 | 18 | dBm |
| 11n (HT20 MCS7) @EVM≦-27 dB | 14 | 16 | 18 | dBm |
| 11n (HT40 MCS7) @EVM≦-27 dB | 14 | 16 | 18 | dBm |
| 11ac (VHT20 MCS8) @EVM≦-30 dB | 13.5 | 15.5 | 17.5 | dBm |
| 11ac (VHT40 MCS9) @EVM≦-32 dB | 12.5 | 14.5 | 16.5 | dBm |
| 11ac (VHT80 MCS9) @EVM≦-32 dB | 12 | 14 | 16 | dBm |
| 11ax (HE20 MCS11) @EVM≦-35 dB | 12.5 | 14.5 | 16.5 | dBm |
| 11ax (HE40 MCS11) @EVM≦-35 dB | 12 | 14 | 16 | dBm |
| 11ax (HE80 MCS11) @EVM≦-35 dB | 11.5 | 13.5 | 15.5 | dBm |

**6G**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 11ax (HE20 MCS11) @EVM≦-35 dB | 10 | 12 | 14 | dBm |
| 11ax (HE40 MCS11) @EVM≦-35 dB | 9 | 11 | 13 | dBm |
| 11ax (HE80 MCS11) @EVM≦-35 dB | 8 | 10 | 12 | dBm |

[1] Unless otherwise stated, limit values apply for an ambient temperature of +25 °C.


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**Receiver Sensitivity****

**2.4G**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 11b (11Mbps) | | 88 | 85 | dBm |
| 11g (54Mbps) | | 76 | 73 | dBm |
| 11n (HT20 MCS7) | | 74 | 71 | dBm |
| 11ax (HE20 MCS11) | | 63 | 60 | dBm |

**5G**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 11a (54Mbps) | | 74 | 71 | dBm |
| 11n (HT20 MCS7) | | 72 | 69 | dBm |
| 11n (HT40 MCS7) | | 69 | 66 | dBm |
| 11ac (VHT20 MCS8) | | 67 | 64 | dBm |
| 11ac (VHT40 MCS9) | | 63 | 60 | dBm |
| 11ac (VHT80 MCS9) | | 60 | 57 | dBm |
| 11ax (HE20 MCS11) | | 60 | 57 | dBm |
| 11ax (HE40 MCS11) | | 56 | 53 | dBm |
| 11ax (HE80 MCS11) | | 55 | 52 | dBm |

**6G**

| | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 11ax (HE20 MCS11) | | 56 | 53 | dBm |
| 11ax (HE40 MCS11) | | 54 | 51 | dBm |
| 11ax (HE80 MCS11) | | 52 | 49 | dBm |

**Data Rate**

802.11b: 1, 2, 5.5, 11Mbps
802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n: MCS0~7 HT20/HT40
802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11ac: MCS0~8 VHT20
802.11ac: MCS0~9 VHT40/VHT80
802.11ax: MCS10~11 HE20/HE40/HE80

**Security**

- WEP
- WPA/WPA2/WPA3 Enterprise with 192-bit encryption
- WMM, WMM-PS (U-APSD), WMM-SA
- AES (hardware accelerator),
- TKIP (hardware accelerator)
- CKIP (software support)

*** If you have any certification questions about output power please contact FAE directly**
****Tx power variation ±3.0 dB for process, voltage and temperature variation across –40°C to +85°C.**


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### 1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 6.0</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2400~2483.5MHz</td></tr>
<tr><td>Modulation</td><td>GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)</td></tr>
<tr><td>Output Power*</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>3</td><td>6</td><td>9</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td>3</td><td>6</td><td>9</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity**</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td></td><td>-90</td><td>-87</td><td>dBm</td></tr>
<tr><td>EDR</td><td></td><td>-86</td><td>-83</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td></td><td>-92</td><td>-89</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

*** If you have any certification questions about output power please contact FAE directly**
**** Project is in engineering stage, RF performance is still being verified.**

### 1.3.4 Operating Conditions

| Features | Description |
|---|---|
| **Operating Conditions** | |
| **Voltage** | 3.3V |
| **Operating Temperature** | -40℃ to 85℃ |
| **Operating Humidity** | less than 85% R.H. |
| **Storage Temperature** | -40℃ to 125℃ |
| **Storage Humidity** | less than 60% R.H. |
| **ESD Protection** | |
| **Human Body Model** | 1000V |
| **Changed Device Model** | 250V |


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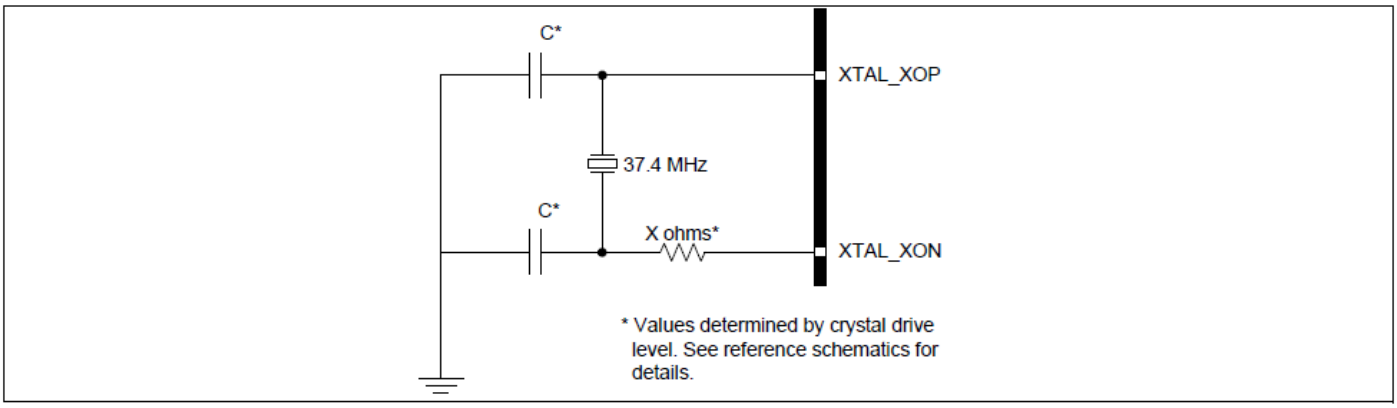
## 1.4 Frequency references

### 1.4.1 XTAL requirements and performance

AW-XM632-PUR can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components. Consult the reference schematics for the latest configuration.




A fractional-N synthesizer in AW-XM632-PUR generates radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.
The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal oscillator interface are listed in Table.

| Parameter | Conditions/Notes | Crystal[1] | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Frequency | 2.4G, 5G, and 6G bands: IEEE 802.11ac/ax operation | - | 37.4 | - | MHz |
| Frequency tolerance over the lifetime of the equipment, including temperature[2] | Without trimming | -20.0 | - | 20.0 | ppm |
| Crystal load capacitance | - | - | 12.0 | - | pF |
| ESR | - | - | - | 60.0 | Ω |
| Drive level | External crystal must be able to tolerate this drive level. | 200 | - | - | μW |
| Input impedance XTAL_XOP | Resistive | - | - | - | kΩ |
| | Capacitive | - | - | 7.5 | pF |

Notes:
1. Use XTAL_XOP and XTAL_XON.
2. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.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### 1.4.2 External 32.768 kHz sleep clock specifications

AW-XM632-PUR requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed must be used.

| Parameter | LPO clock | Unit |
|---|---|---|
| Nominal input frequency | 32.768 | kHz |
| Frequency accuracy | ±250 | ppm |
| Duty cycle | 30 – 70 | % |
| Input signal amplitude | 200–1800 | mV, p–p |
| Signal type | Square-wave or sine-wave | - |
| Input impedance[1] | > 100k | Ω |
| Clock jitter[2] (during initial startup) | < 5 | pF |
| | < 10,000 | ppm |

Notes:
1. When power is applied or switched off.
2. The LPO_IN input receiver has ac-coupled capacitance on the input with the feedback resistor to maintain the common mode around VDDIO/2 and power supply noise should be maintained less than 100mV to avoid any false glitches before the time constant (ac- coupled capacitance * feedback resistor, i.e., 100 µs) settles down.


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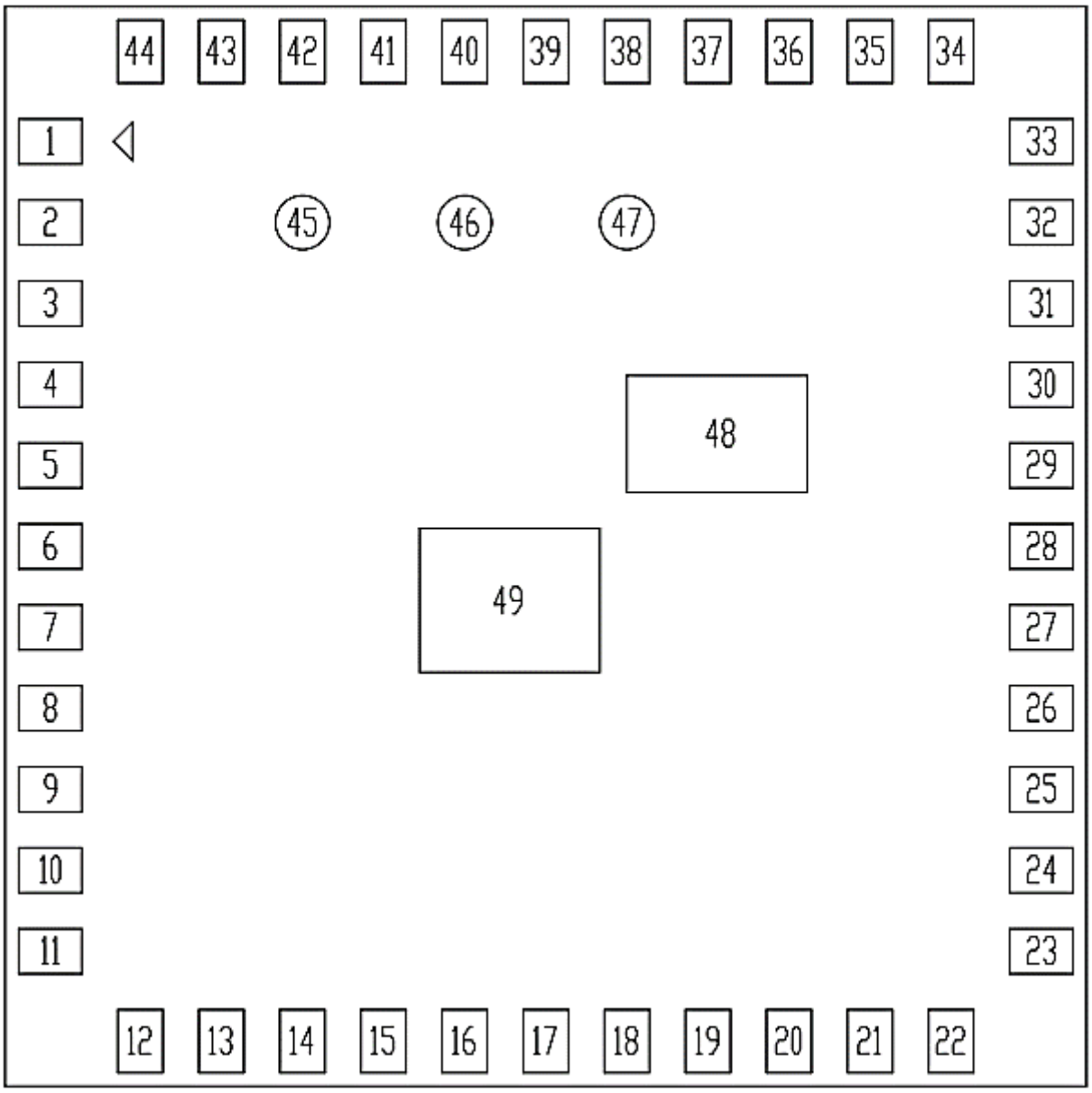
# 2. Pin Definition

## 2.1 Pin Map




**AW-XM632-PUR Pin Map (Top View)**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## 2.2 Pin Table

| Pin No | Definition | Basic Description | Voltage | Type |
|---|---|---|---|---|
| **1** | GND | Ground. | - | GND |
| **2** | NC | Floating | | - |
| **3** | GND | Ground. | - | GND |
| **4** | GND | Ground. | - | GND |
| **5** | ANT | WLAN/BT RF ANT. | | RF |
| **6** | GND | Ground. | - | GND |
| **7** | GND | Ground. | - | GND |
| **8** | BT_PCM_OUT | PCM data output. | VDDIO | O |
| **9** | BT_PCM_CLK | PCM clock; can be master (output) or slave (input). | VDDIO | I/O |
| **10** | BT_PCM_IN | PCM data input. | VDDIO | I |
| **11** | BT_PCM_SYNC | PCM sync, can be master (output) or slave (input). | VDDIO | I/O |
| **12** | BT_UART_CTS_N | UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface. | VDDIO | I |
| **13** | BT_UART_RXD | UART serial input. Serial data input for the HCI UART interface. | VDDIO | I |
| **14** | BT_UART_TXD | UART Serial Output. Serial data output for the HCI UART interface. | VDDIO | O |
| **15** | BT_UART_RTS_N | UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin. | VDDIO | O |
| **16** | BT_DEV_WAKE | Bluetooth DEVICE WAKE. | VDDIO | I/O |
| **17** | BT_REG_ON | Used by the PMU to power up or power down the internal regulators used by the Bluetooth® section. When deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming. | VDDIO | I |
| **18** | GND | Ground. | - | GND |
| **19** | WL_HOST_WAKE | WLAN HOST_WAKE. | VDDIO | I/O |
| **20** | VBAT | 3.3V power pin. | 3.3V | PWR |
| **21** | GND | Ground. | - | GND |
| **22** | CSR_VLX | CSR Power Stage Output to Inductor. | 0.9V | O |


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| | | | | |
|---|---|---|---|---|
| **23** | CBUCK_0P9 | Internal Buck 0.9V voltage generation pin. | 0.9V | I |
| **24** | GND | Ground. | - | GND |
| **25** | PCIE_TDP | PCIE Transmitter Differential Pair Positive Output. | - | O |
| **26** | PCIE_TDN | PCIE Transmitter Differential Pair Negative Output. | - | O |
| **27** | GND | Ground. | - | GND |
| **28** | PCIE_RDP | PCIE Receiver Differential Pair Negative Input. | - | I |
| **29** | PCIE_RDN | PCIE Receiver Differential Pair Positive Input. | | I |
| **30** | GND | Ground. | - | GND |
| **31** | PCIE_REFCLKN | PCI Express differential clock input Negative. | - | I |
| **32** | PCIE_REFCLKP | PCI Express differential clock input Positive. | - | I |
| **33** | GND | Ground. | - | GND |
| **34** | LPO_IN | External Low Power Clock input (32.768KHz). | - | I |
| **35** | GND | Ground. | - | GND |
| **36** | XTAL_OUT | External Xtal Output (37.4MHz). | | O |
| **37** | XTAL_IN | External Oscillator Input. (37.4MHz). | - | I |
| **38** | GND | Ground. | - | GND |
| **39** | BT_HOST_WAKE | Bluetooth HOST WAKE. | - | I/O |
| **40** | PCIE_CLKREQ_L | PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated.<br>1 = the clock can be gated.<br>0 = the clock is required. | - | OD |
| **41** | PCIE_PME_L | PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3. | - | OD |
| **42** | PCIE_PREST_L | PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1 | - | I |
| **43** | VDDIO | 1.8 V IO Supply for WLAN GPIOs. | 1.8V | PWR |
| **44** | WL_REG_ON | Used by the PMU to power up or power down the internal AW-XM632-PUR regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in | VDDIO | I |


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| | | | | |
|---|---|---|---|---|
| | | reset. This pin has an internal 50 KΩ pull-down resistor that is auto enabled/disabled by programming. | | |
| **45** | GPIO_2 | GPIO configuration pin | VDDIO | I/O |
| **46** | GPIO_3 | GPIO configuration pin | VDDIO | I/O |
| **47** | GPIO_4 | GPIO configuration pin | VDDIO | I/O |
| **48** | GND | Ground. | - | GND |
| **49** | GND | Ground. | - | GND |


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# 3. Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **VBAT** | DC supply for the VBAT and PA driver supply | -0.5 | - | 6.0 | V |
| **VDDIO** | DC supply voltage for digital I/O | -0.5 | - | 2.2 | V |
| **$T_j$** | Maximum junction temperature | - | - | 125 | °C |

## 3.2 Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **VBAT** | Power supply for Internal Regulator | 3.13 | 3.3 | 3.47 | V |
| **VDDIO** | DC supply voltage for digital I/O | 1.71 | 1.8 | 1.89 | V |

## 3.3 Digital IO Pin DC Characteristics

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **Digital I/O pins, VDDIO=1.8V** | | | | | |
| **$V_{IH}$** | Input high voltage | 0.65 × VDDIO | - | - | V |
| **$V_{IL}$** | Input low voltage | - | - | 0.35 × VDDIO | V |
| **$V_{OH}$** | Output high voltage | VDDIO – 0.40 | - | - | V |
| **$V_{OL}$** | Output Low Voltage | - | - | 0.45 | V |
| **WL_REG_ON & BT_REG_ON Pins** | | | | | |
| **-** | Input high voltage | 1.2 | - | VBAT | - |
| **-** | Input low voltage | - | - | 0.3 | - |


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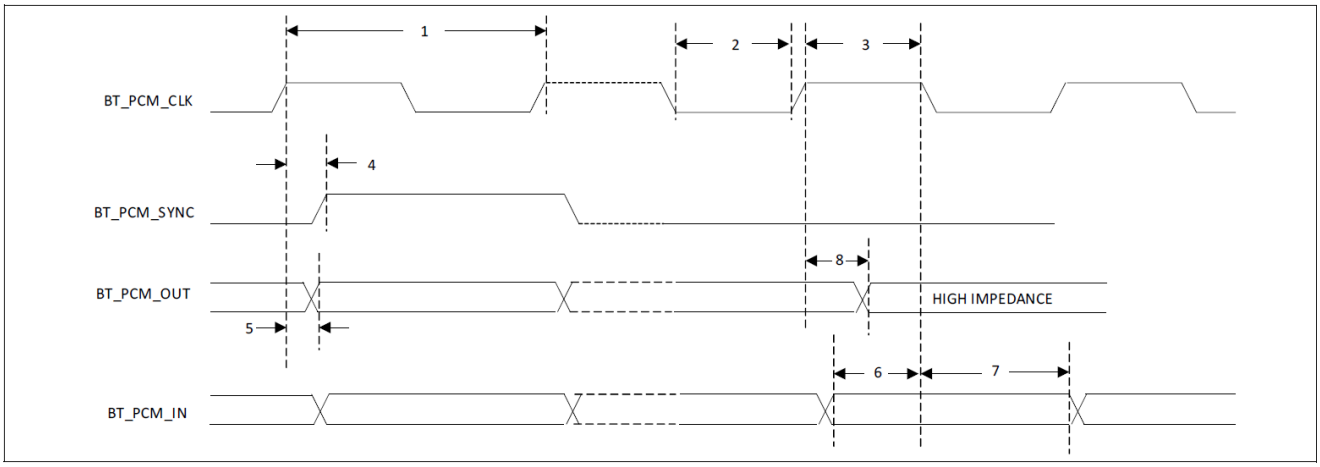
## 3.4 Host Interface

### 3.4.1 PCM Interface Timing

PCM Timing Diagram (Short Frame Sync, Master Mode)




PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | – | – | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | – | – | ns |
| 3 | PCM bit clock HIGH | 41 | – | – | ns |
| 4 | PCM_SYNC delay | 0 | – | 25 | ns |
| 5 | PCM_OUT delay | 0 | – | 25 | ns |
| 6 | PCM_IN setup | 8 | – | – | ns |
| 7 | PCM_IN hold | 8 | – | – | ns |
| 8 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | – | 25 | ns |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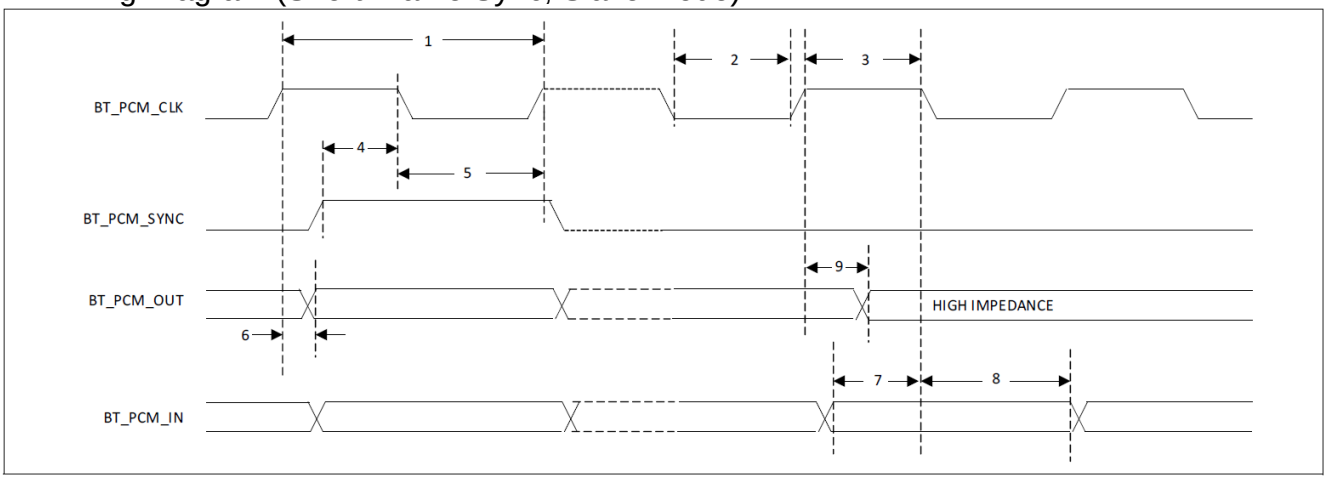
PCM Timing Diagram (Short Frame Sync, Slave Mode)




PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | – | – | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | – | – | ns |
| 3 | PCM bit clock HIGH | 41 | – | – | ns |
| 4 | PCM_SYNC setup | 8 | – | – | ns |
| 5 | PCM_SYNC hold | 8 | – | – | ns |
| 6 | PCM_OUT delay | 0 | – | 25 | ns |
| 7 | PCM_IN setup | 8 | – | – | ns |
| 8 | PCM_IN hold | 8 | – | – | ns |
| 9 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | | 25 | ns |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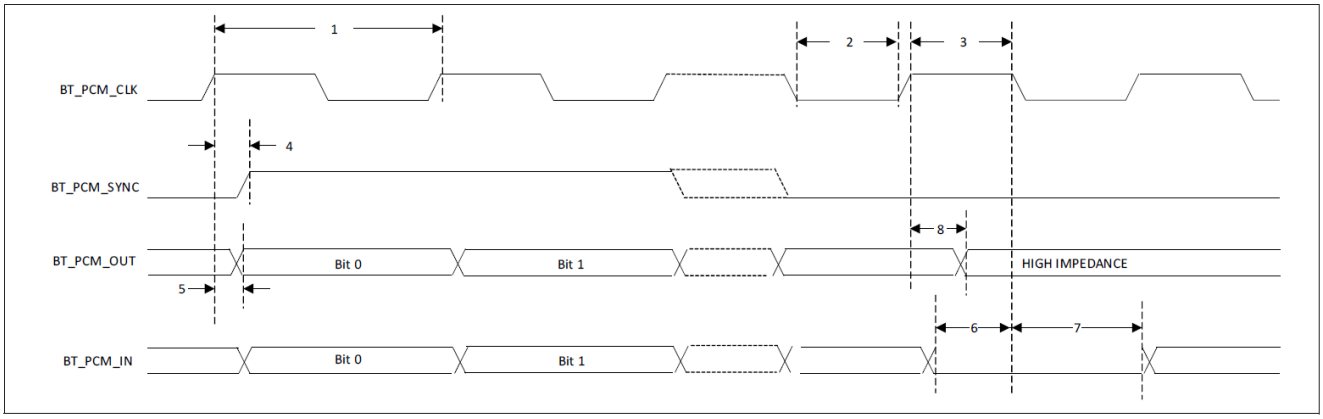
PCM Timing Diagram (Long Frame Sync, Master Mode)




PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | – | – | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | – | – | ns |
| 3 | PCM bit clock HIGH | 41 | – | – | ns |
| 4 | PCM_SYNC delay | 0 | – | 25 | ns |
| 5 | PCM_OUT delay | 0 | – | 25 | ns |
| 6 | PCM_IN setup | 8 | – | – | ns |
| 7 | PCM_IN hold | 8 | – | – | ns |
| 8 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | – | 25 | ns |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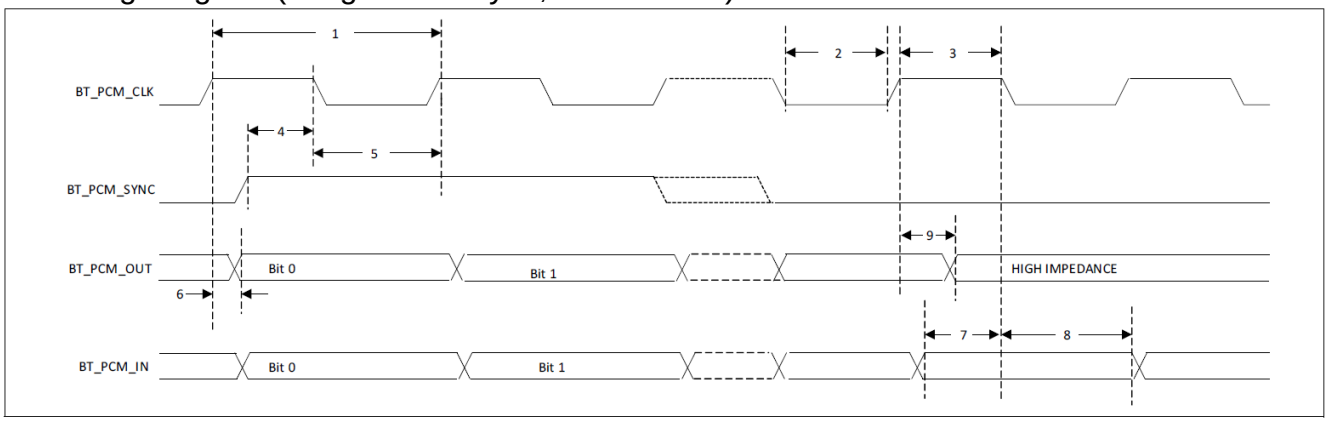
PCM Timing Diagram (Long Frame Sync, Slave Mode)




PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | – | – | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | – | – | ns |
| 3 | PCM bit clock HIGH | 41 | – | – | ns |
| 4 | PCM_SYNC setup | 8 | – | – | ns |
| 5 | PCM_SYNC hold | 8 | – | – | ns |
| 6 | PCM_OUT delay | 0 | – | 25 | ns |
| 7 | PCM_IN setup | 8 | – | – | ns |
| 8 | PCM_IN hold | 8 | – | – | ns |
| 9 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | | 25 | ns |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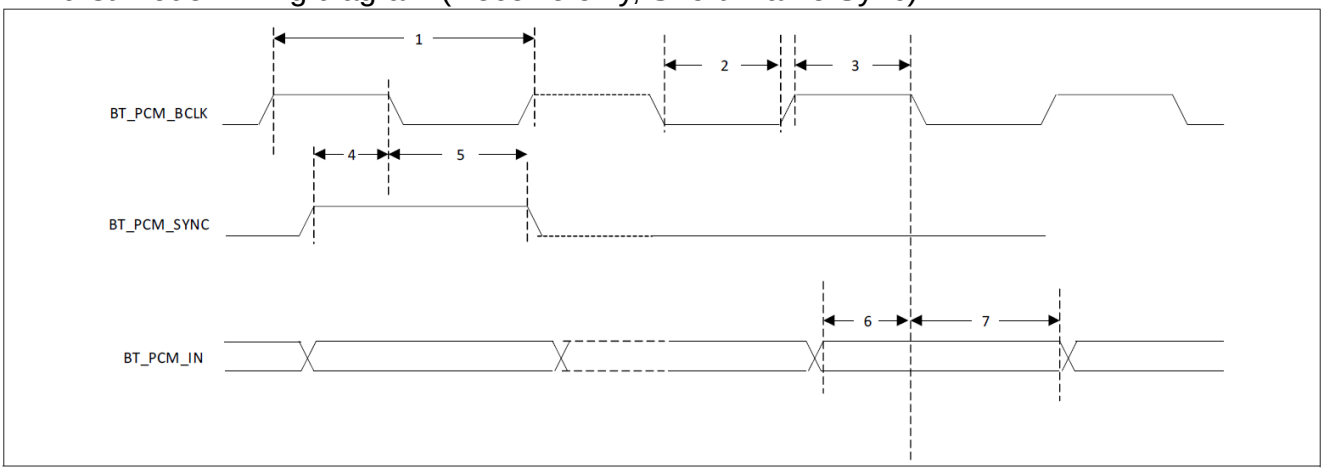
PCM Burst Mode Timing diagram (Receive only, Short Frame Sync)




PCM Burst Mode (Receive Only, Short Frame Sync)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | – | – | 24 | MHz |
| 2 | PCM bit clock LOW | 20.8 | – | – | ns |
| 3 | PCM bit clock HIGH | 20.8 | – | – | ns |
| 4 | PCM_SYNC setup | 8 | – | – | ns |
| 5 | PCM_SYNC hold | 8 | – | – | ns |
| 6 | PCM_IN setup | 8 | – | – | ns |
| 7 | PCM_IN hold | 8 | – | – | ns |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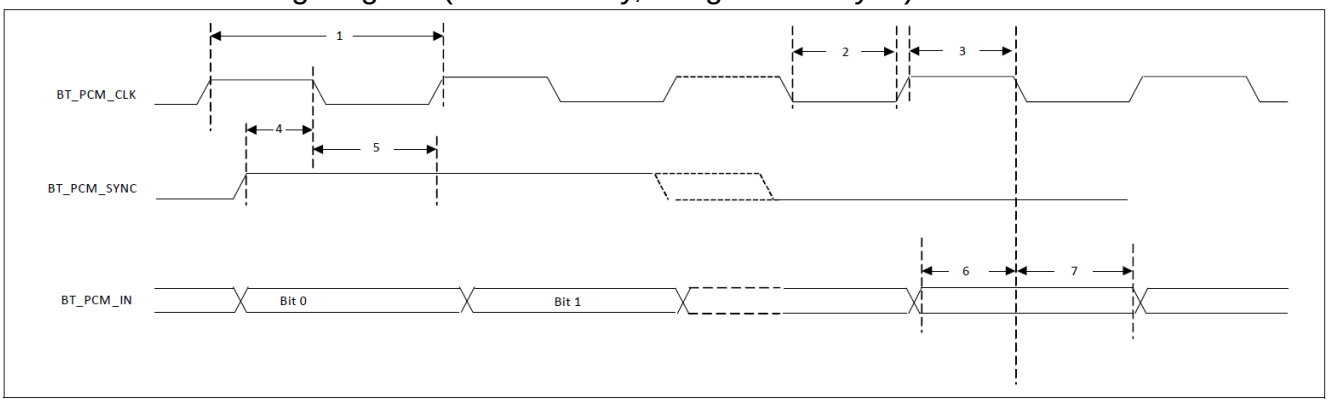
PCM Burst Mode Timing diagram (Receive only, Long Frame Sync)




PCM Burst Mode (Receive Only, Long Frame Sync)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | – | – | 24 | MHz |
| 2 | PCM bit clock LOW | 20.8 | – | – | ns |
| 3 | PCM bit clock HIGH | 20.8 | – | – | ns |
| 4 | PCM_SYNC setup | 8 | – | – | ns |
| 5 | PCM_SYNC hold | 8 | – | – | ns |
| 6 | PCM_IN setup | 8 | – | – | ns |
| 7 | PCM_IN hold | 8 | – | – | ns |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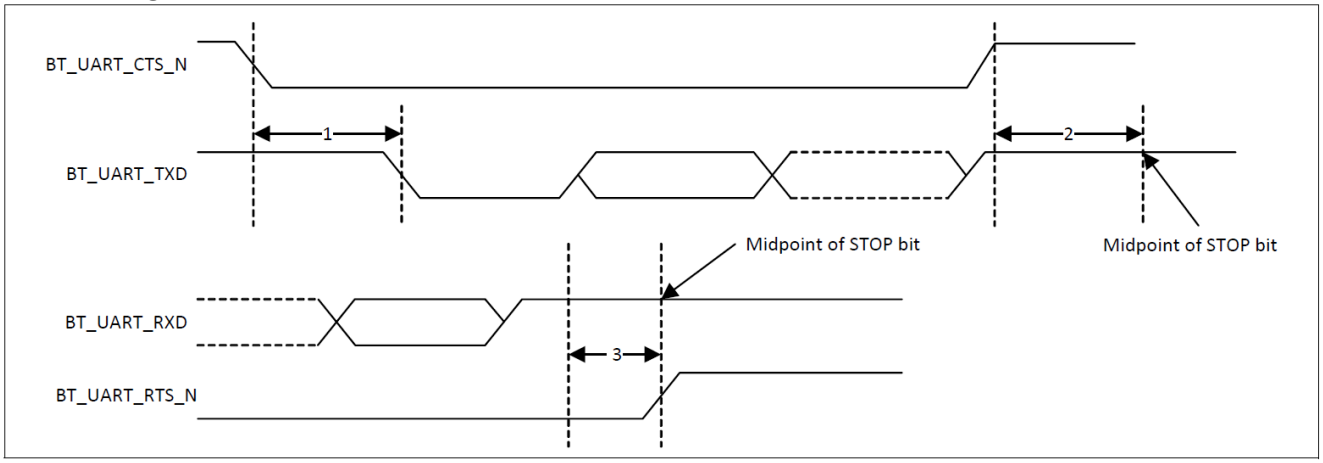
### 3.4.2 UART Interface

The AW-XM632-PUR UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The baud rate may be selected through a vendor-specific UART HCI command. UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 6.0 UART HCI specification. The default baud rate is 115.2 Kbaud.
The AW-XM632-PUR UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.
Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-XM632-PUR UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

**UART Timing**




**UART Timing specifications**

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **1** | Delay time, BT_UART_CTS_N low to BT_UART_TXD valid | – | – | 1.5 | Bit periods |
| **2** | Setup time, BT_UART_CTS_N high before midpoint of stop bit | – | – | 0.5 | Bit periods |
| **3** | Delay time, midpoint of stop bit to BT_UART_RTS_N high | – | – | 0.5 | Bit periods |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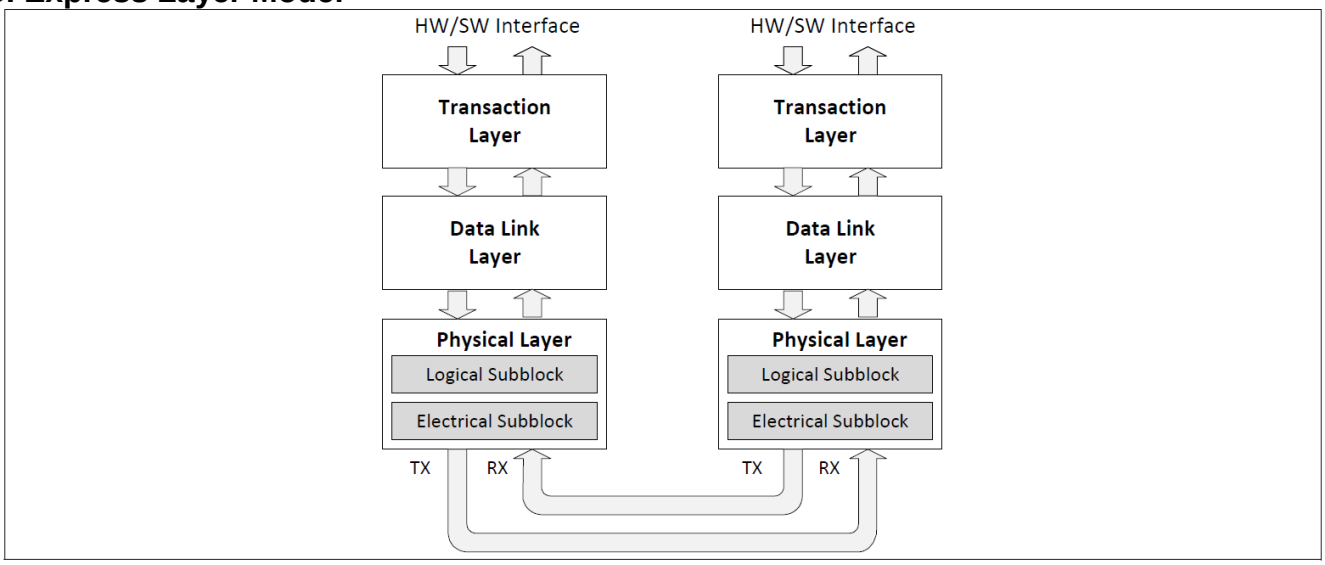
### 3.4.3 PCI Express Interface

The PCI Express (PCIe) core on the AW-XM632-PUR is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0. This core contains all the necessary blocks, including logical and electrical functional sub-blocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and AW-XM632-PUR device. The transmit side processes outbound packets while the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

**PCI Express Layer Model**





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## 3.5 Power up Timing Sequence

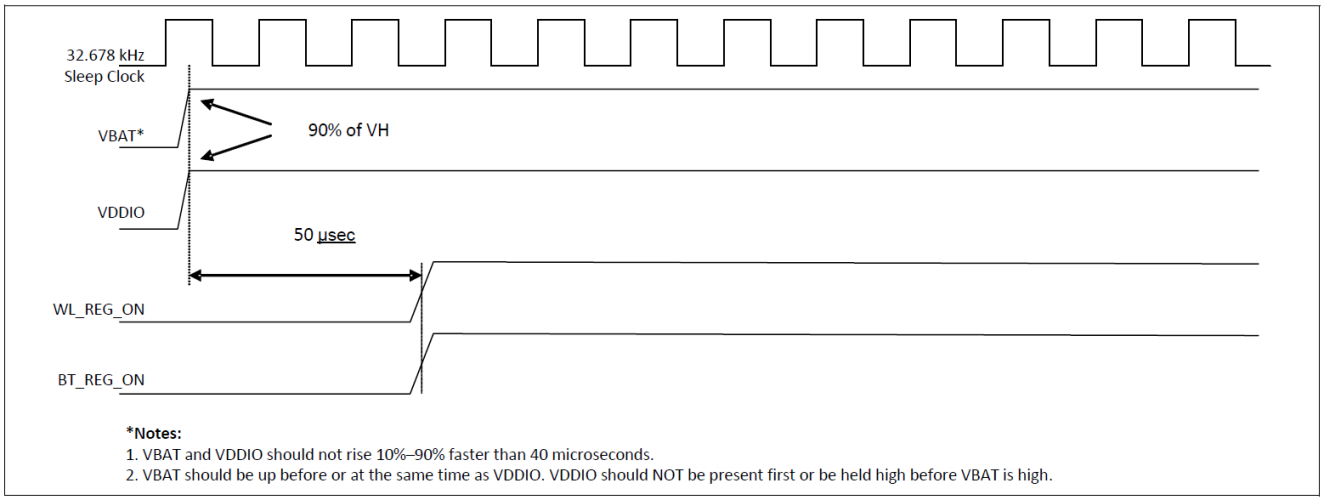
AW-XM632-PUR has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

### 3.5.1 Description of Control Signals

■ WL_REG_ON: Used by the PMU to power up the WLAN section. It is also OR–gated with the BT_REG_ON input to control the internal AW-XM632-PUR regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
■ BT_REG_ON: Used by the PMU (OR–gated with WL_REG_ON) to power up the internal AW-XM632-PUR regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the Bluetooth section is in reset.
■ Note
VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.

### 3.5.2 Control Signal Timing Diagrams

■ **WLAN = ON, Bluetooth = ON**





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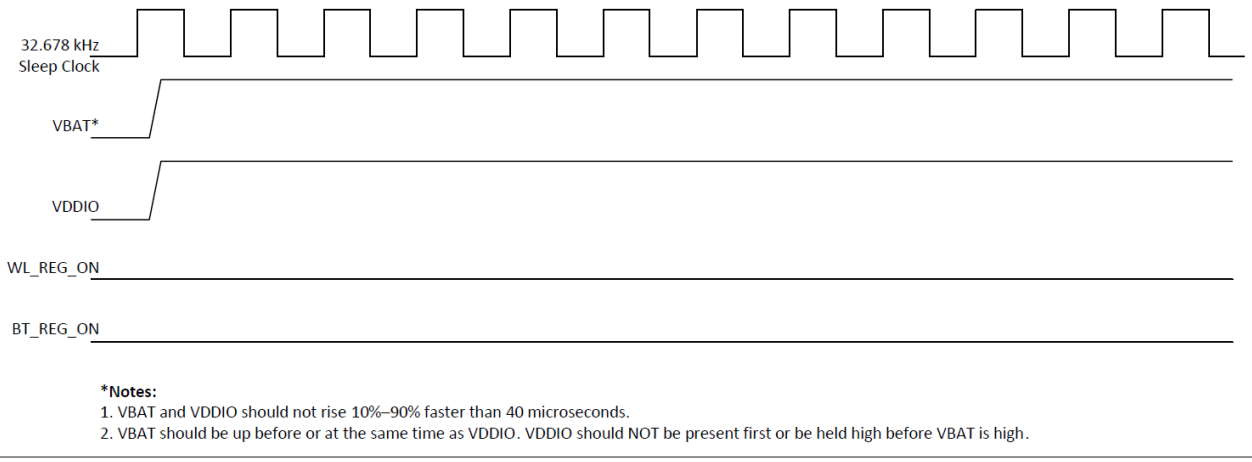
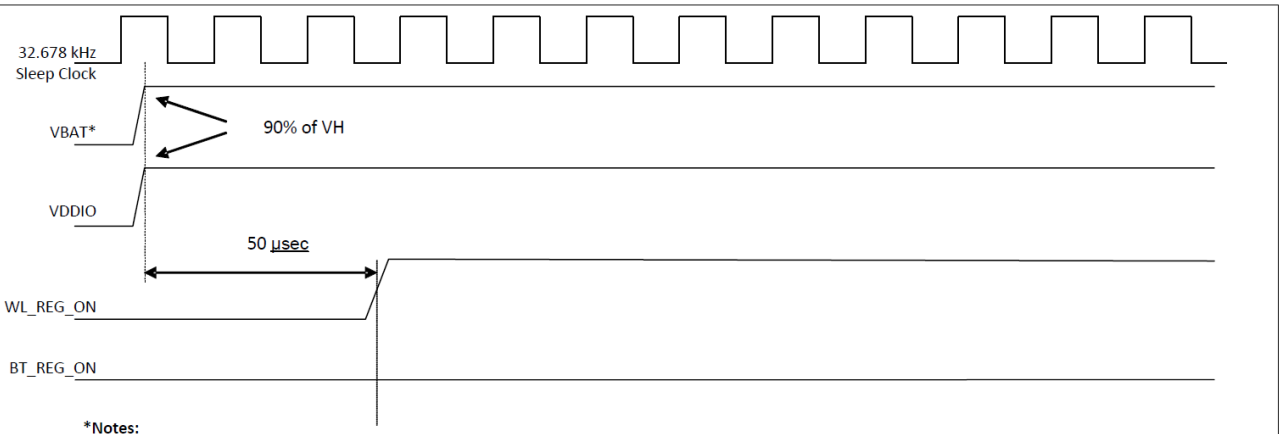
## ■ WLAN = OFF, Bluetooth = OFF



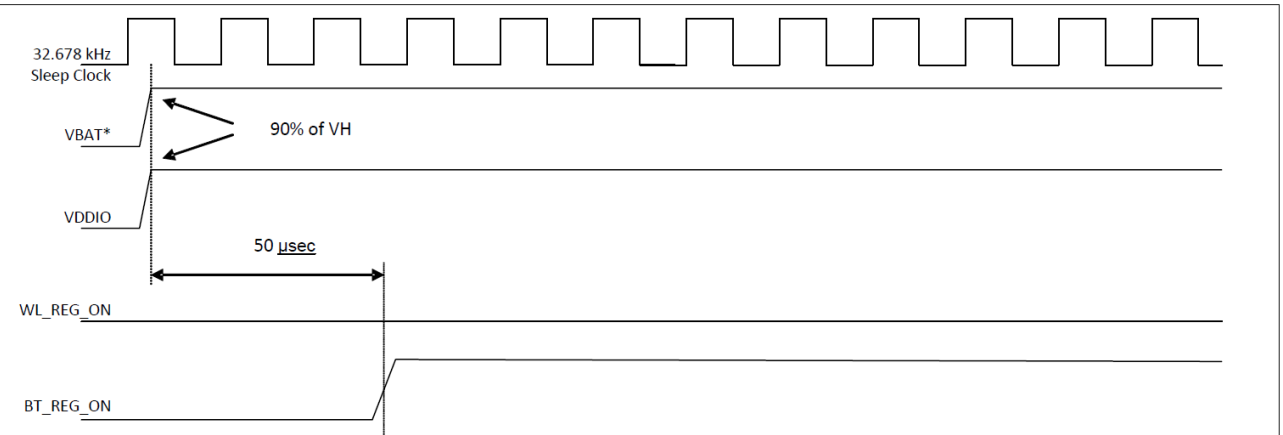

***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

## ■ WLAN = ON, Bluetooth = OFF




***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

## ■ WLAN = OFF, Bluetooth = ON




***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.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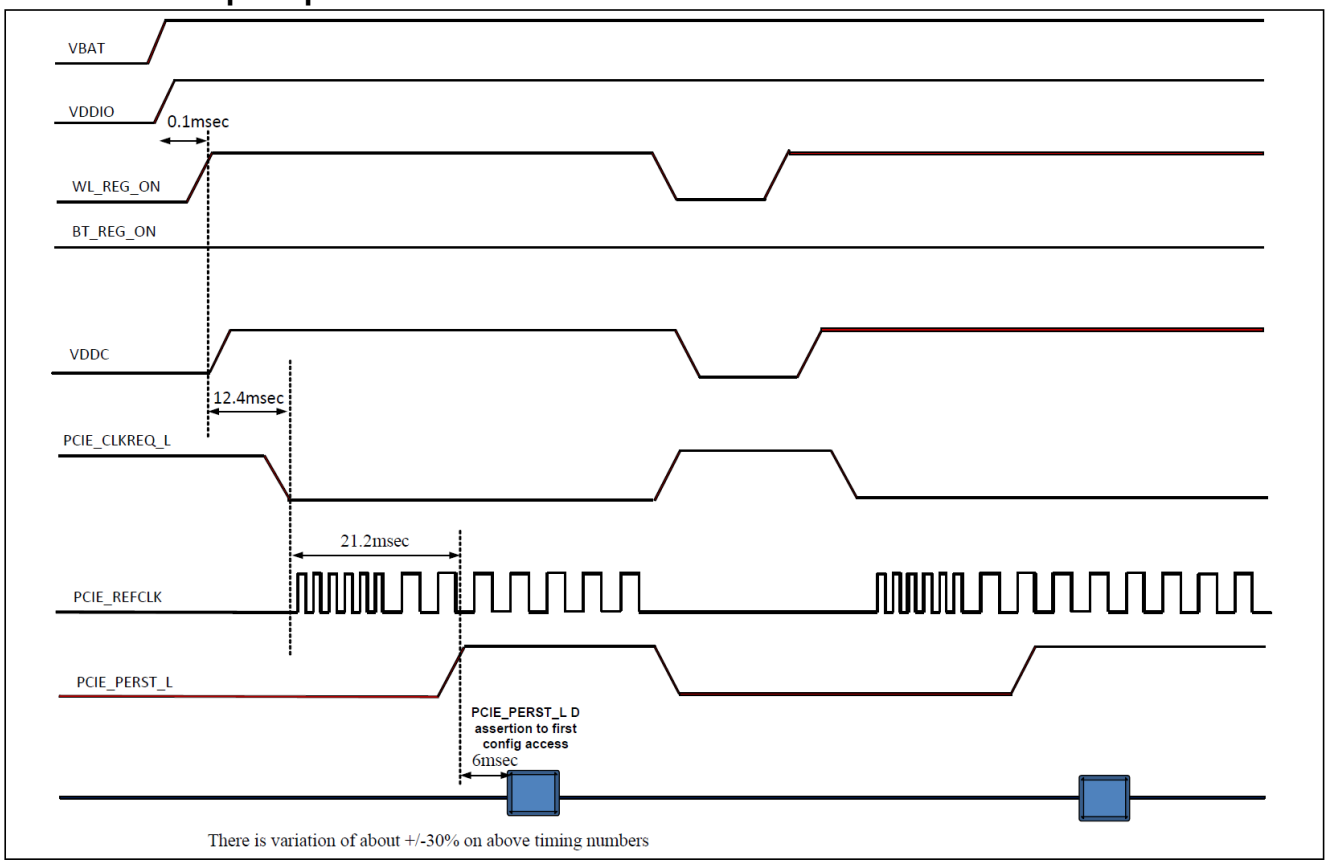
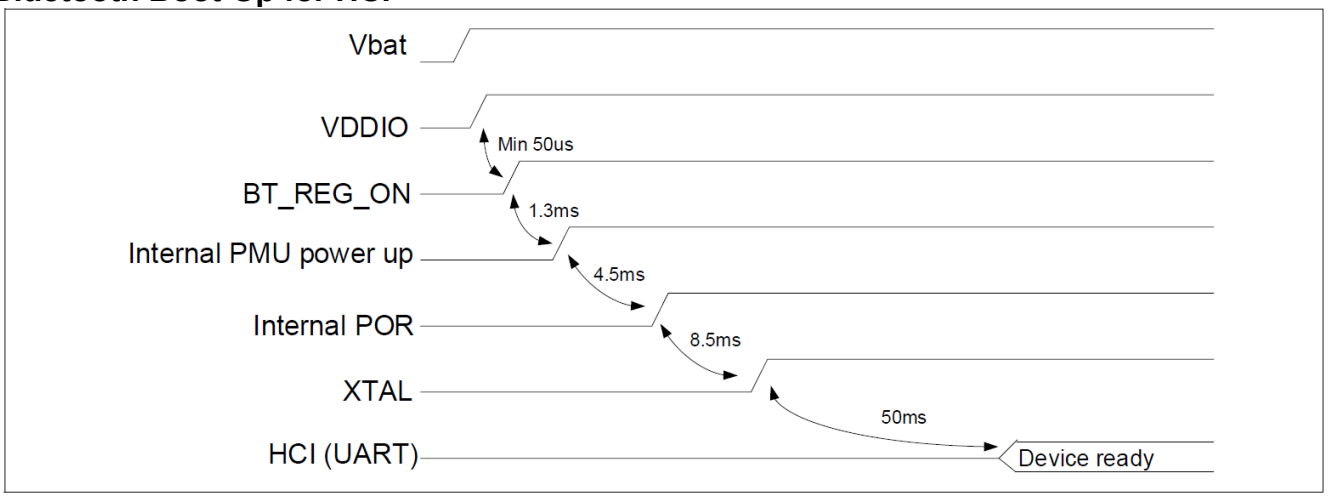
## ■ WLAN Power-Up Sequence for PCIe Host




## ■ Bluetooth Boot-Up for HCI





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## 3.6 Power Consumption*

### 3.6.1 WLAN

| No. | Item | | | VBAT_IN=3.3 V | |
|---|---|---|---|---|---|
| | | | | Max. | Avg. |
| 1 | Pdn *(1) (2) (5) | | | 0.02 | 0.0002 |
| 2 | Deep Sleep *(2) (3) (5) (7) (Not associated with AP) | | | 57.3 | 8.8 |
| 3 | Power Save DTIM 1 (2.4GHz)*(2) (4)(5) (7) | | | 28.7 | 8.6 |
| 4 | Power Save DTIM 1 (5GHz) *(2) (4)(5) (7) | | | 25.1 | 8.5 |
| 5 | Power Save DTIM 1 (6GHz) *(2) (4)(5) (6) (7) | | | 85.2 | 9.6 |
| **Band (GHz)** | **Mode** | **BW (MHz)** | **RF Power (dBm)** | **Transmit*(7)** | |
| | | | | **Max.** | **Avg.** |
| 2.4 | 11b@11Mbps | 20 | 18 | 303 | 285 |
| | 11g@54Mbps | 20 | 17 | 276 | 194 |
| | 11n@MCS7 | 20 | 16.5 | 276 | 186 |
| | 11ax@MCS0 NSS1 | 20 | 14 | 250 | 215 |
| | 11ax@MCS11 NSS1 | 20 | 14 | 254 | 165 |
| 5 | 11a@6Mbps | 20 | 16 | 362 | 310 |
| | 11n@MCS7 | 40 | 16 | 379 | 220 |
| | 11ac@MCS0 NSS1 | 80 | 14 | 370 | 295 |
| | 11ac@MCS9 NSS1 | 80 | 14 | 363 | 215 |
| | 11ax@MCS0 NSS1 | 80 | 13.5 | 373 | 287 |
| | 11ax@MCS11 NSS1 | 80 | 13.5 | 364 | 212 |
| 6 | 11ax@MCS0 NSS1 | 20 | 12 | 310 | 268 |
| | 11ax@MCS11 NSS1 | 20 | 12 | 309 | 196 |
| | 11ax@MCS0 NSS1 | 40 | 11 | 310 | 254 |
| | 11ax@MCS11 NSS1 | 40 | 11 | 305 | 182 |
| | 11ax@MCS0 NSS1 | 80 | 10 | 305 | 236 |
| | 11ax@MCS11 NSS1 | 80 | 10 | 304 | 187 |
| **Band (GHz)** | **Mode** | **BW(MHz)** | | **Receive*(7)** | |
| | | | | **Max.** | **Avg.** |
| 2.4 | 11b@11Mbps | 20 | | 71 | 68 |
| | 11n@MCS7 | 20 | | 75 | 71 |
| | 11ax@MCS11 NSS1 | 20 | | 76 | 70 |
| 5 | 11a@54Mbps | 20 | | 80 | 76 |
| | 11n@MCS7 | 40 | | 90 | 84 |
| | 11ac@MCS9 NSS1 | 80 | | 102 | 95 |
| | 11ax@MCS11 NSS1 | 80 | | 109 | 94 |
| 6 | 11ax@MCS11 NSS1 | 20 | | 83 | 77 |
| | 11ax@MCS11 NSS1 | 40 | | 95 | 84 |
| | 11ax@MCS11 NSS1 | 80 | | 109 | 93 |

***Current Unit: mA**



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| No. | Item | | | VDDIO=1.8 V | |
|---|---|---|---|---|---|
| | | | | Max. | Avg. |
| 1 | Pdn *(1) (2) (5) | | | 0.014 | 0.00048 |
| 2 | Deep Sleep *(2) (3) (5) (7) (Not associated with AP) | | | 1.2 | 1.2 |
| 3 | Power Save DTIM 1 (2.4GHz)*(2) (4)(5) (7) | | | 1.3 | 1.2 |
| 4 | Power Save DTIM 1 (5GHz) *(2) (4)(5) (7) | | | 1.3 | 1.2 |
| 5 | Power Save DTIM 1 (6GHz) *(2) (4)(5) (6) (7) | | | 1.3 | 1.2 |
| Band (GHz) | Mode | BW (MHz) | RF Power (dBm) | Transmit*(7) | |
| | | | | Max. | Avg. |
| 2.4 | 11b@1Mbps | 20 | 18 | 5.3 | 5.1 |
| | 11ax@MCS11 NSS1 | 20 | 14 | 5.3 | 5.2 |
| 5 | 11a@6Mbps | 20 | 16 | 5.3 | 5.0 |
| | 11ax@MCS11 NSS1 | 80 | 13.5 | 5.3 | 5.2 |
| 6 | 11ax@MCS11 NSS1 | 80 | 10 | 5.3 | 5.2 |
| Band (GHz) | Mode | BW(MHz) | | Receive*(7) | |
| | | | | Max. | Avg. |
| 2.4 | 11b@11Mbps | 20 | | 1.3 | 1.2 |
| 5 | 11ax@MCS11 NSS1 | 80 | | 1.3 | 1.2 |
| 6 | 11ax@MCS11 NSS1 | 80 | | 1.3 | 1.2 |

***Current Unit: mA**

### 3.6.2 Bluetooth

| Mode | Packet Type | RF Power (dBm) | VBAT_IN=3.3 V | |
|---|---|---|---|---|
| | | | Max. | Avg. |
| Sleep*(1) | N/A | N/A | 0.457 | 0.036 |
| Transmit*(1) (2) | DH5 | 6 | 24 | 16 |
| Receive*(1) (2) | DH5 | N/A | 24 | 13 |

***Current Unit: mA**

| Mode | Packet Type | RF Power (dBm) | VDDIO=1.8 V | |
|---|---|---|---|---|
| | | | Max. | Avg. |
| Sleep*(1) | N/A | N/A | 22.6 | 13.0 |
| Transmit*(1) (2) | DH5 | 6 | 313 | 281 |
| Receive*(1) (2) | DH5 | N/A | 311 | 277 |

***Current Unit: mA**


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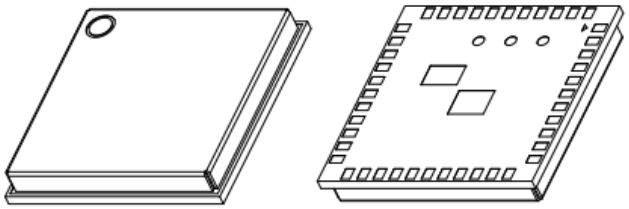
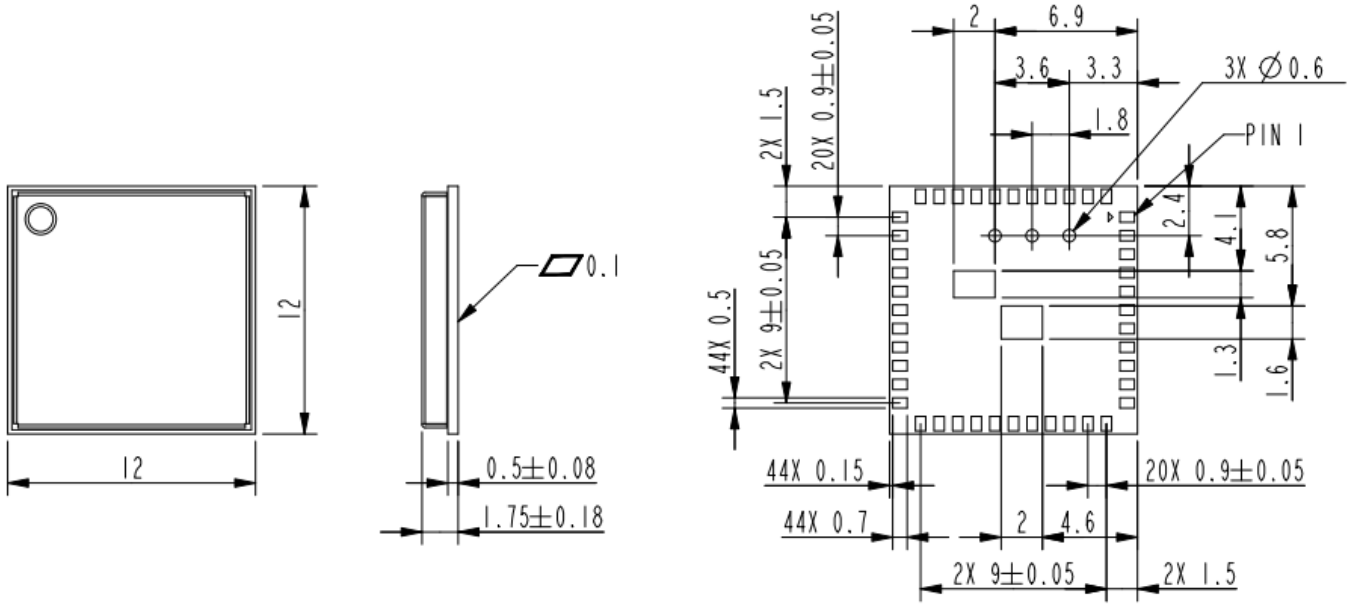
# 4. Mechanical Information

## 4.1 Mechanical Drawing






TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm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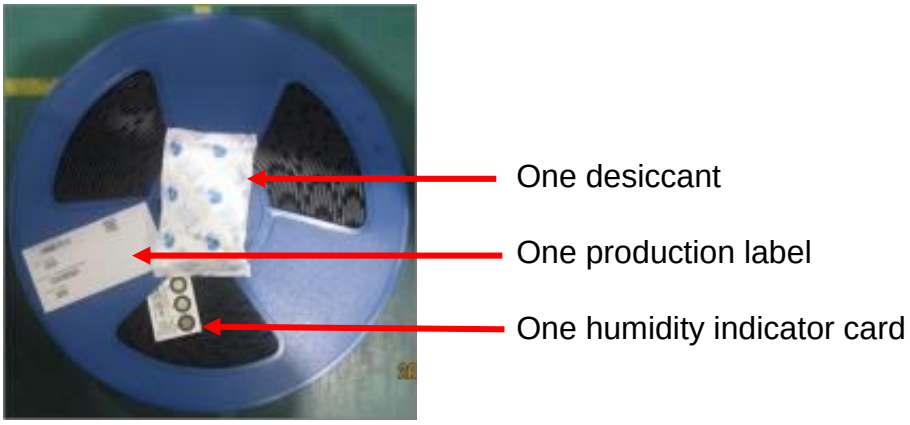
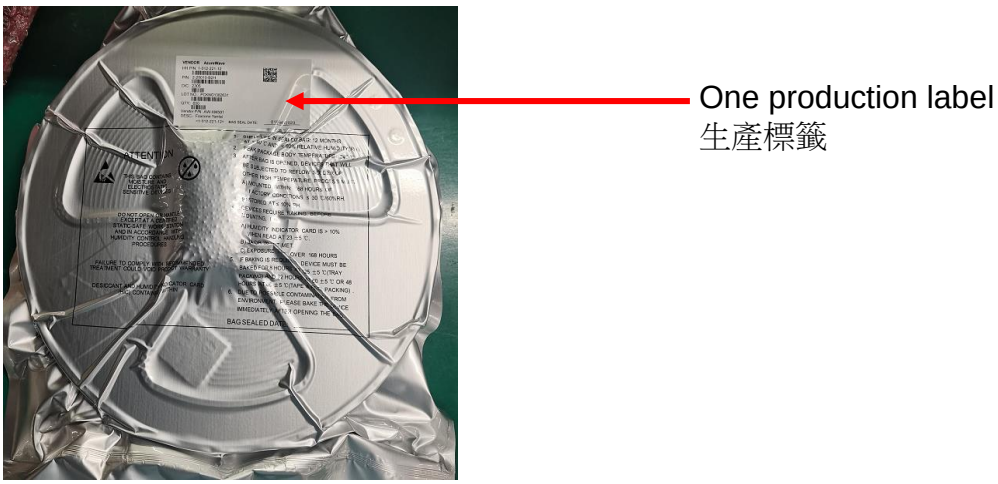
# 5. Packaging Information

1. One reel can pack 1,500pcs 12x12 stamp/LGA modules
   (整軸產品數量為 1500pcs)

2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel
   (卷軸貼上一張生產標籤，並放上一包防潮包及濕度指示卡)




3. One reel is put into the anti-static moisture barrier bag, and then one production label is pasted on the bag
   (卷軸放進防靜電鋁箔袋，再貼上一張生產標籤)




4. A bag is put into the anti-static pink bubble wrap
   (防靜電鋁箔袋放進氣泡袋內)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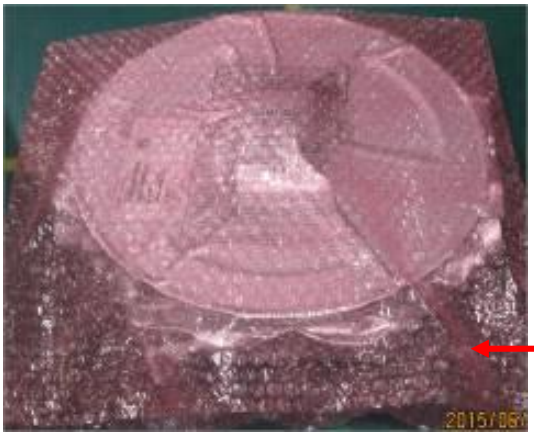

One anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box

(氣泡袋放進內箱中，再貼上一張生產標籤)


One production label

6. **5 inner boxes** could be put into one carton

(五個內箱可以放進一個外箱)



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7. Sealing the carton by transparent tape
   (使用透明膠帶將外箱進行工字型封箱)

8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton
   (外箱上貼附出貨標籤和箱號標籤；如不滿箱，需貼附尾數標籤)

One carton label
出貨標籤 →

One box label
箱號標籤 →



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