AW-XHA01

IEEE 802.11 a/b/g/n/ac/ax Wi-Fi 6E

+ Bluetooth 5.3 Combo SiP Module

Datasheet

Rev.B

DF

(For Standard)

Features

Wi-Fi

- 802.11a/b/g/n/ac/ax compliant, dual-band capable (2.4/5/6 GHz).
- 5/6 GHz: 20/40/80-MHz channels, 1024-QAM, 2x2 MIMO providing up to 1.2 Gbps PHY data rate.
- 2.4 GHz: 20/40-MHz channels, 1024-QAM, 2x2 MIMO providing up to 574 Mbps PHY date rate.
- 802.11ax STA mode and Soft AP mode with 11ax scheduled access.
- Supports 802.11d, h, k, r, v, w, ai.
- Zero-wait dynamic frequency selection (DFS): Background channel availability check (CAC) scan for immediate switch to candidate DFS channel.
- On-chip power amplifiers and low-noise amplifiers
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE.
- Fast VSDB (Virtual Simultaneous Dual Band)
- Worldwide regulatory support: Global products supported with worldwide homologated design.
- Integrated Arm® Cortex® R4 processor with tightly coupled memory for complete WLAN subsystem functionality. This architecture offloads the host processor completely from WLAN functionality.
- Transmission and reception of HE-SU and HE-ER-SU PPDU.
- Reception of HE-MU PPDU -OFDMA/MU-MIMO Frame.
- Transmission of HE-TB PPDU (Uplink MU OFDMA).

Bluetooth

- Bluetooth 5.3 (BDR + EDR + BLE).
- All Bluetooth 5.0/5.1/5.2 optional features supported including LE-Audio.
- Dedicated Bluetooth RF path for best WLAN-BT coexistence performance.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM/I2S for audio data.
- Supports multiple simultaneous Advanced Audio Distribution.
- Profiles (A2DP) for stereo sound.
- On-chip memory includes 512 KB SRAM and 2 MB ROM.

Interface

- PCIe Gen2 (3.0 Compliant) for WLAN: complies with PCI Express base specification revision 3.0 for × 1 lane and power management running at Gen2 speeds.
- SDIO 3.0/2.0 for WLAN.

- HCI-UART, PCM/I2S for Bluetooth.

Coexistence

- SDIO 3.0/2.0 for WLAN.
- Built-in advanced algorithms for Wi-Fi + Bluetooth/WLAN coexistence.
- 2-wire SECI for external 3rd party Bluetooth/GPS/LTE radios.

General

- Fully integrated programmable dynamic Power Management Unit.
- Supports VBAT power supply range from 3.0 V to 4.8 V with internal regulator.
- Supports 1.8V VDDIO.
- Supports 1340 Bytes of OTP shared between Bluetooth and.
- WLAN for storing board parameters.

Revision History

Document NO: R2-1A01-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2024/05/30	DCN031644	● Initial Version	YuFu Chen	N.C. Chen
B	2024/07/26	DCN032015	● Pin map modify ● Module size modify ● Block diagram modify	YuFu Chen	N.C. Chen

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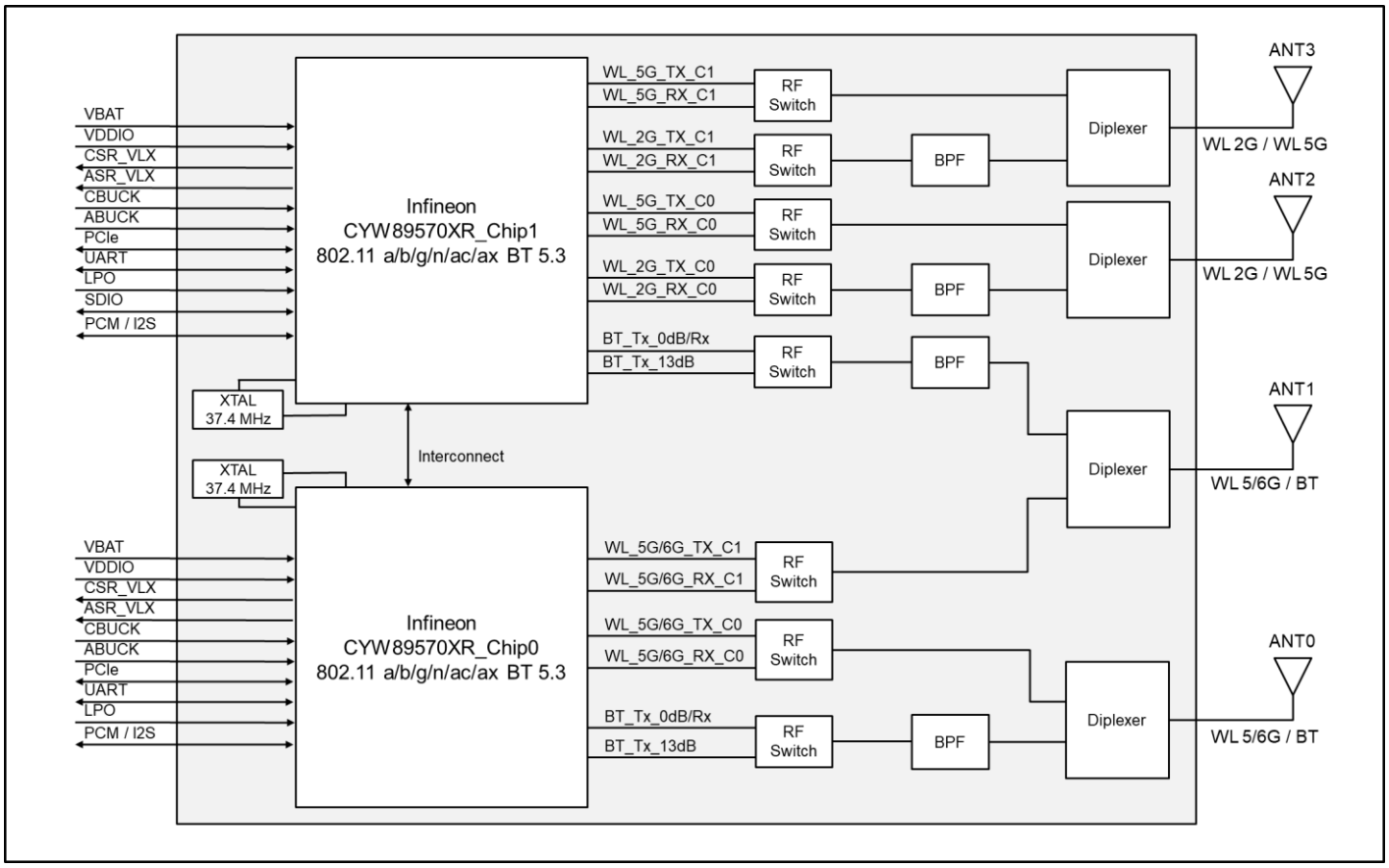
1. Introduction

1.1 Product Overview

The AW-XHA01 device provides the highest level of integration for Automotive and Industrial IoT wireless systems with integrated tri-band 2x2 MIMO Wi-Fi 6E WLAN MAC/baseband/radio, Bluetooth 5.3 MAC/baseband/radio, and integrated Power Management Unit. WLAN and Bluetooth radios also include on-chip power amplifiers and low-noise amplifiers to further reduce the need for external components.

WLAN interfaces to host processor through a PCIe v3.0 Gen2 or SDIO 3.0 interface while Bluetooth host interface is provided through high-speed 4-wire UART interface. Additionally, the Bluetooth section supports PCM and I2S interfaces for audio applications.
AW-XHA01 is based on Infineon CYW89570XR solution. CYW89570XR is qualified to operate across Automotive Grade 3 (-40°C to +85°C) temperature range.

1.2 Block Diagram



AW-XHA01 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	802.11 a/b/g/n/ac/ax Wi-Fi 6E + Bluetooth 5.3 Combo SiP Module
Major Chipset	Infineon CYW89570XR
Host Interface	Wi-Fi + BT ● Chip1: SDIO + UART or PCIe + UART ● Chip0: PCIe + UART
Dimension	20.5 mm x 13 mm x 1.26 mm
Form factor	SiP with LGA,176 pins
Antenna	ANT0 : Wi-Fi → 5G / 6G, Bluetooth ANT1 : Wi-Fi → 5G / 6G, Bluetooth ANT2 : Wi-Fi → 2.4G / 5G ANT3 : Wi-Fi → 2.4G / 5G
Weight	TBD

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac/ax
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	WLAN: 2.4 / 5 / 6 GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9), 1024-QAM(MCS10~11)
Number of Channels	**2.4GHz** ● USA, Canada and Taiwan – 1 ~ 11 ● China, Most European Countries – 1 ~ 13 ● Japan, 1 ~ 13 **5GHz** ● USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

6GHz

- CH1~CH233

Output Power[1]
(Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<8%	TBD	TBD	TBD	dBm
11g (54Mbps) @EVM≦-25 dB	TBD	TBD	TBD	dBm
11n (HT20 MCS7) @EVM≦-27 dB	TBD	TBD	TBD	dBm
11ax (HE20 MCS11) @EVM≦-35 dB	TBD	TBD	TBD	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM<-25 dB	TBD	TBD	TBD	dBm
11n (HT20 MCS7) @EVM≦-27 dB	TBD	TBD	TBD	dBm
11n (HT40 MCS7) @EVM≦-27 dB	TBD	TBD	TBD	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	TBD	TBD	TBD	dBm
11ac (VHT40 MCS9) @EVM≦-32 dB	TBD	TBD	TBD	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	TBD	TBD	TBD	dBm
11ax (HE20 MCS11) @EVM≦-35 dB	TBD	TBD	TBD	dBm
11ax (HE40 MCS11) @EVM≦-35 dB	TBD	TBD	TBD	dBm
11ax (HE80 MCS11) @EVM≦-35 dB	TBD	TBD	TBD	dBm

6G

	Min	Typ	Max	Unit
11ax (HE20 MCS11) @EVM≦-35 dB	TBD	TBD	TBD	dBm
11ax (HE40 MCS11) @EVM≦-35 dB	TBD	TBD	TBD	dBm

[1] Unless otherwise stated, limit values apply for an ambient temperature of +25 °C.

<table>
<tr><td></td><td>
<table>
<tr><td>11ax (HE80 MCS11)
@EVM≦-35 dB</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity**</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS11)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ac (VHT20 MCS8)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ac (VHT40 MCS9)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ax (HE20 MCS11)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ax (HE40 MCS11)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ax (HE80 MCS11)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table>
6G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11ax (HE20 MCS11)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ax (HE40 MCS11)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>11ax (HE80 MCS11)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>802.11b: 1, 2, 5.5, 11Mbps
802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n: MCS0~7 HT20/HT40
802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11ac: MCS0~8 VHT20
802.11ac: MCS0~9 VHT40/VHT80
802.11ax: MCS10~11 HE20/HE40/HE80</td></tr>
<tr><td>Security</td><td>● WEP
● WPA/WPA2/WPA3 Enterprise with 192-bit encryption
● AES (hardware accelerator),
● TKIP (hardware accelerator)
● CKIP (software support)</td></tr>
</table>

*** If you have any certification questions about output power please contact FAE directly**
**** Project is in engineering stage, RF performance is still being verified.**

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Bluetooth 5.3</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2400~2483.5MHz</td></tr>
<tr><td>Modulation</td><td>GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)</td></tr>
<tr><td>Output Power*</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity**</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>EDR</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td>TBD</td><td>TBD</td><td>TBD</td><td>dBm</td></tr>
</table>
</td></tr>
</table>

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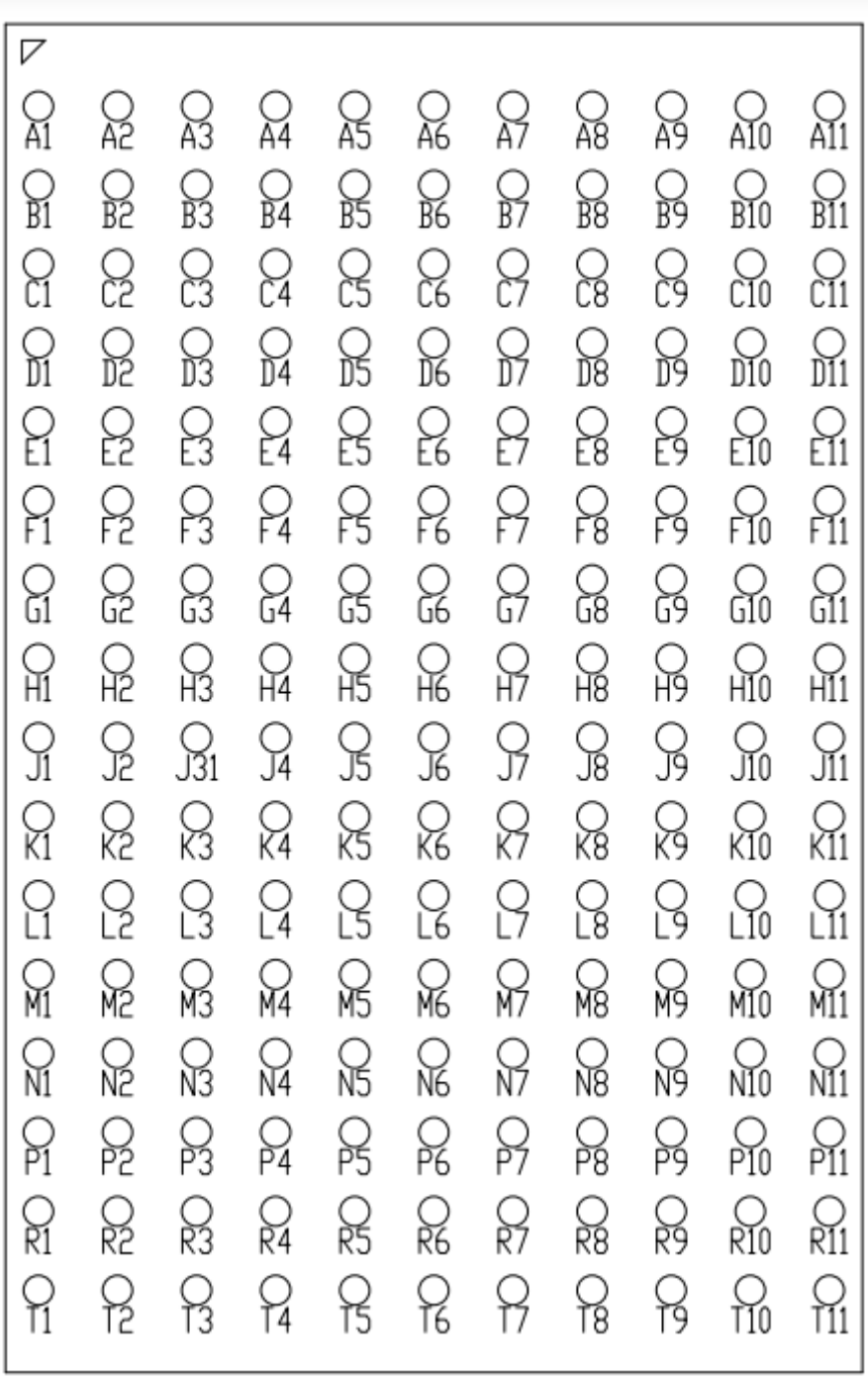
1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V
Operating Temperature	-40℃ to 85℃
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃ to 125℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

2. Pin Definition

2.1 Pin Map



AW-XHA01 Pin Map (Top View)

2.2 Pin Table

*** : CYW89570XR Chip0 Pin
***_1 : CYW89570XR Chip1 Pin

Pin No	Definition	Basic Description	Voltage	Type
A1	GND	Ground.	-	GND
A2	GND	Ground.	-	GND
A3	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	VDDIO	I
A4	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	VDDIO	O
A5	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	VDDIO	I
A6	WL_REG_ON	Used by the PMU to power up or power down the internal CYW89570 regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 KΩ pull-down resistor that is auto enabled/disabled by programming	VDDIO	I
A7	GND	Ground.	-	GND
A8	BT_PCM_SYNC	PCM sync, can be master (output) or slave (input)	VDDIO	I/O
A9	BT_PCM_IN	PCM data input.	VDDIO	I
A10	GND	Ground.	-	GND
A11	PCIE_TDN	PCIE Transmitter Differential Pair Negative Output	-	O
B1	GND	Ground.	-	GND
B2	GND	Ground.	-	GND
B3	BT_DEV_WAKE	Bluetooth DEVICE WAKE	VDDIO	I/O
B4	BT_HOST_WAKE	Bluetooth HOST_WAKE.	VDDIO	I/O
B5	BT_UART_TXD	UART Serial Output. Serial data output for the HCI UART interface.	VDDIO	O
B6	GND	Ground.	-	GND
B7	GND	Ground.	-	GND

B8	BT_PCM_OUT	PCM data output.	VDDIO	O
B9	BT_PCM_CLK	PCM clock; can be master (output) or slave (input).	VDDIO	I/O
B10	GND	Ground.	-	GND
B11	PCIE_TDP	PCIE Transmitter Differential Pair Positive Output	-	O
C1	GND	Ground.	-	GND
C2	GND	Ground.	-	GND
C3	GND	Ground.	-	GND
C4	GND	Ground.	-	GND
C5	GND	Ground.	-	GND
C6	I2S_DI	I2S Serial Data Input	VDDIO	I/O
C7	I2S_SCK	I2S Bit or Serial Clock	VDDIO	I/O
C8	I2S_MCK	I2S Master Clock	VDDIO	I/O
C9	GND	Ground.	-	GND
C10	GND	Ground.	-	GND
C11	PCIE_RDN	PCIE Receiver Differential Pair Positive Input	-	I
D1	ANT0	WLAN/BT RF TX/RX path. Antenna Port0.	-	RF
D2	GND	Ground.	-	GND
D3	PCIE_PERST_L	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1	-	I
D4	PCIE_PME_L	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3	-	OD
D5	GND	Ground.	-	GND
D6	GND	Ground.	-	GND
D7	I2S_DO	I2S Serial Data Output	VDDIO	I/O
D8	I2S_LRCK	I2S Word Clock or Left/Right Clock	VDDIO	I/O

D9	BT_REG_ON	Used by the PMU to power up or power down the internal CYW89570 regulators used by the Bluetooth section. When deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming	VDDIO	I
D10	GND	Ground.	-	GND
D11	PCIE_RDP	PCIE Receiver Differential Pair Negative Input	-	I
E1	GND	Ground.	-	GND
E2	GND	Ground.	-	GND
E3	GND	Ground.	-	GND
E4	PCIE_CLKREQ_L	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.	-	OD
E5	GND	Ground.	-	GND
E6	GND	Ground.	-	GND
E7	WL_DEV_WAKE	WLAN DEVICE WAKE	VDDIO	I/O
E8	LPO_IN	External Sleep Clock Input (32.768 kHz)	-	I
E9	WL_HOST_WAKE	WLAN HOST_WAKE.	VDDIO	I/O
E10	GND	Ground.	-	GND
E11	PCIE_REFCLKN	PCIE Differential Pair Clock Source (100 MHz) Negative Input.	-	I
F1	ANT_1	WLAN/BT RF TX/RX path. Antenna Port1.	-	RF
F2	GND	Ground.	-	GND
F3	BT_PCM_CLK_1	PCM clock; can be master (output) or slave (input).	VDDIO	I/O
F4	GND	Ground.	-	GND
F5	GND	Ground.	-	GND
F6	GND	Ground.	-	GND
F7	GND	Ground.	-	GND
F8	WL_UART_TX	Debug UART Serial Output.	VDDIO	O

F9	WL_UART_RX	Debug UART Serial Input.	VDDIO	I
F10	GND	Ground.	-	GND
F11	PCIE_REFCLKP	PCIE Differential Pair Clock Source (100 MHz) Positive Input.	-	I
G1	GND	Ground.	-	GND
G2	GND	Ground.	-	GND
G3	BT_PCM_OUT_1	PCM data output.	VDDIO	O
G4	BT_PCM_SYNC_1	PCM sync, can be master (output) or slave (input)	VDDIO	I/O
G5	GND	Ground.	-	GND
G6	GND	Ground.	-	GND
G7	GND	Ground.	-	GND
G8	GND	Ground.	-	GND
G9	GND	Ground.	-	GND
G10	ABUCK_1P12	Internal Buck 1.12V voltage generation pin.	1.12V	I
G11	ASR_VLX	ASR Power Stage Output to Inductor	1.12V	O
H1	GND	Ground.	-	GND
H2	GND	Ground.	-	GND
H3	GND	Ground.	-	GND
H4	BT_PCM_IN_1	PCM data input.	VDDIO	I
H5	SDIO_DATA1_1	SDIO Data Line 1	VDDIO	I/O
H6	SDIO_CLK_1	SDIO Clock Input	VDDIO	I
H7	SDIO_CMD_1	SDIO Command Line	VDDIO	I/O
H8	GND	Ground.	-	GND
H9	VDDIO	1.8 V IO Supply for WLAN GPIOs	1.8V	PWR
H10	CBUCK_0P9	Internal Buck 0.9V voltage generation pin.	0.9V	I
H11	CSR_VLX	CSR Power Stage Output to Inductor	0.9V	O

J1	GND	Ground.	-	GND
J2	GND	Ground.	-	GND
J3	BT_HOST_WAKE_1	Bluetooth HOST_WAKE.	VDDIO	I/O
J4	GND	Ground.	-	GND
J5	SDIO_DATA3_1	SDIO Data Line 3	VDDIO	I/O
J6	SDIO_DATA0_1	SDIO Data Line 0	VDDIO	I/O
J7	SDIO_DATA2_1	SDIO Data Line 2	VDDIO	I/O
J8	GND	Ground.	-	GND
J9	GND	Ground.	-	GND
J10	GND	Ground.	-	GND
J11	VBAT	3.3V power pin	3.3V	PWR
K1	GND	Ground.	-	GND
K2	GND	Ground.	-	GND
K3	GND	Ground.	-	GND
K4	BT_DEV_WAKE_1	Bluetooth DEVICE WAKE	VDDIO	I/O
K5	GND	Ground.	-	GND
K6	GND	Ground.	-	GND
K7	BT_UART_RTS_1	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	VDDIO	O
K8	BT_UART_RXD_1	UART serial input. Serial data input for the HCI UART interface.	VDDIO	I
K9	GND	Ground.	-	GND
K10	GND	Ground.	-	GND
K11	PCIE_TDN_1	PCIE Transmitter Differential Pair Negative Output	-	O
L1	GND	Ground.	-	GND
L2	GND	Ground.	-	GND
L3	I2S_SCK_1	I2S Bit or Serial Clock	VDDIO	I/O

L4	I2S_MCK_1	I2S Master Clock	VDDIO	I/O
L5	I2S_DI_1	I2S Serial Data Input	VDDIO	I/O
L6	GND	Ground.	-	GND
L7	BT_UART_CTS_1	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	VDDIO	I
L8	BT_UART_TXD_1	UART Serial Output. Serial data output for the HCI UART interface.	VDDIO	O
L9	GND	Ground.	-	GND
L10	GND	Ground.	-	GND
L11	PCIE_TDP_1	PCIE Transmitter Differential Pair Positive Output	-	O
M1	ANT_2	WLAN RF TX/RX path. Antenna Port2	-	RF
M2	GND	Ground.	-	GND
M3	I2S_DO_1	I2S Serial Data Output	VDDIO	I/O
M4	I2S_LRCK_1	I2S Word Clock or Left/Right Clock	VDDIO	I/O
M5	GND	Ground.	-	GND
M6	PCIE_PERST_L_1	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1	-	I
M7	PCIE_CLKREQ_L_1	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.	-	OD
M8	GND	Ground.	-	GND
M9	GND	Ground.	-	GND
M10	GND	Ground.	-	GND
M11	PCIE_RDN_1	PCIE Receiver Differential Pair Positive Input	-	I
N1	GND	Ground.	-	GND
N2	GND	Ground.	-	GND
N3	GND	Ground.	-	GND
N4	WL_DEV_WAKE_1	WLAN DEVICE WAKE	VDDIO	I/O
N5	GND	Ground.	-	GND

N6	PCIE_PME_L_1	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3	-	OD
N7	GND	Ground.	-	GND
N8	LPO_IN_1	External Sleep Clock Input (32.768 kHz)	-	I
N9	WL_REG_ON_1	Used by the PMU to power up or power down the internal CYW89570 regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 KΩ pull-down resistor that is auto enabled/disabled by programming	VDDIO	I
N10	GND	Ground.	-	GND
N11	PCIE_RDP_1	PCIE Receiver Differential Pair Negative Input	-	I
P1	GND	Ground.	-	GND
P2	GND	Ground.	-	GND
P3	WL_UART_TX_1	Debug UART Serial Output.	VDDIO	O
P4	WL_UART_RX_1	Debug UART Serial Input.	VDDIO	I
P5	GND	Ground.	-	GND
P6	GPIO_1_1	SDIO enabled strapping connect an external resistor to GND, using a 4.7 kΩ resistor.	VDDIO	I/O
P7	BT_REG_ON_1	Used by the PMU to power up or power down the internal CYW89570 regulators used by the Bluetooth section. When deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming	VDDIO	I
P8	GND	Ground.	-	GND
P9	WL_HOST_WAKE_1	WLAN HOST_WAKE.	VDDIO	I/O
P10	ASR_VLX_1	ASR Power Stage Output to Inductor	1.12V	O
P11	PCIE_REFCLKN_1	PCIE Differential Pair Clock Source (100 MHz) Negative Input.	-	I
R1	ANT_3	WLAN RF TX/RX path. Antenna Port3	-	RF

R2	GND	Ground.	-	GND
R3	GND	Ground.	-	GND
R4	GND	Ground.	-	GND
R5	GND	Ground.	-	GND
R6	GND	Ground.	-	GND
R7	GND	Ground.	-	GND
R8	GND	Ground.	-	GND
R9	ABUCK_1P12_1	Internal Buck 1.12V voltage generation pin.	1.12V	I
R10	CSR_VLX_1	CSR Power Stage Output to Inductor	0.9V	O
R11	PCIE_REFCLKP_1	PCIE Differential Pair Clock Source (100 MHz) Positive Input.	-	I
T1	GND	Ground.	-	GND
T2	GND	Ground.	-	GND
T3	GND	Ground.	-	GND
T4	GND	Ground.	-	GND
T5	GND	Ground.	-	GND
T6	VDDIO_1	1.8 V IO Supply for WLAN GPIOs	1.8V	PWR
T7	GND	Ground.	-	GND
T8	GND	Ground.	-	GND
T9	CBUCK_0P9_1	Internal Buck 0.9V voltage generation pin.	0.9V	I
T10	VBAT_1	3.3V power pin	3.3V	PWR
T11	GND	Ground.	-	GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	-0.5	-	6.0	V
VDDIO	DC supply voltage for digital I/O	-0.5	-	2.2	V
Tj	Maximum junction temperature	-	-	125	°C

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulator	3.135	3.3	3.465	V
VDDIO	DC supply voltage for digital I/O	1.71	1.8	1.89	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital I/O pins, VDDIO=1.8V					
V_{IH}	Input high voltage	0.65 × VDDIO	-	-	V
V_{IL}	Input low voltage	-	-	0.35 × VDDIO	V
V_{OH}	Output high voltage	VDDIO - 0.40	-	-	V
V_{OL}	Output Low Voltage	-	-	0.45	V

Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

3.4 WL_REG_ON & BT_REG_ON Pins

Symbol	Parameter	Minimum	Typical	Maximum	Unit
-	Input High Voltage	1.2	-	VBAT	V
-	Input Low Voltage	-	-	0.3	V

3.5 Power up Timing Sequence

AW-XHA01 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

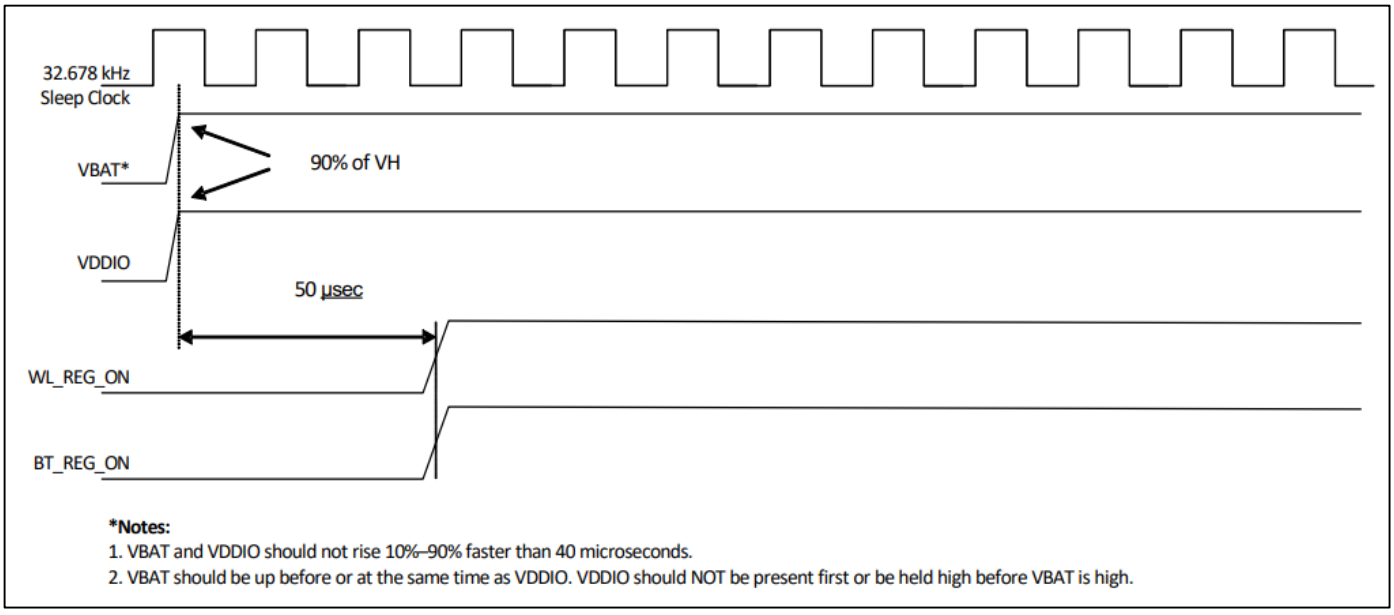
Description of Control Signals

■ **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-XHA01 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

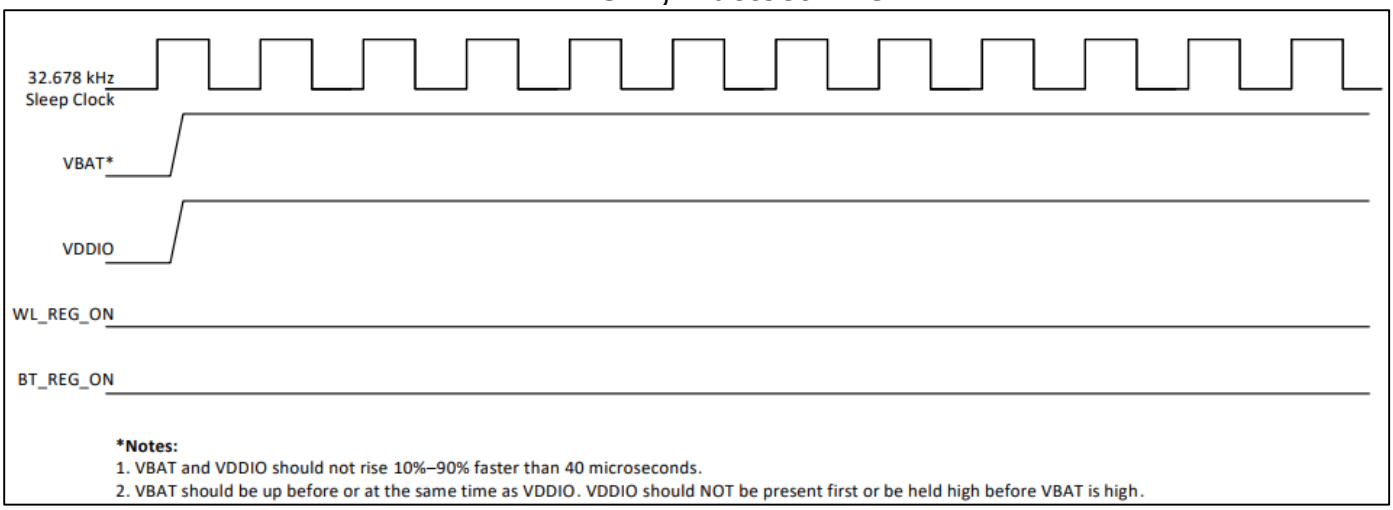
■ **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal AW-XHA01 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note : VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.

WLAN = ON, Bluetooth = ON

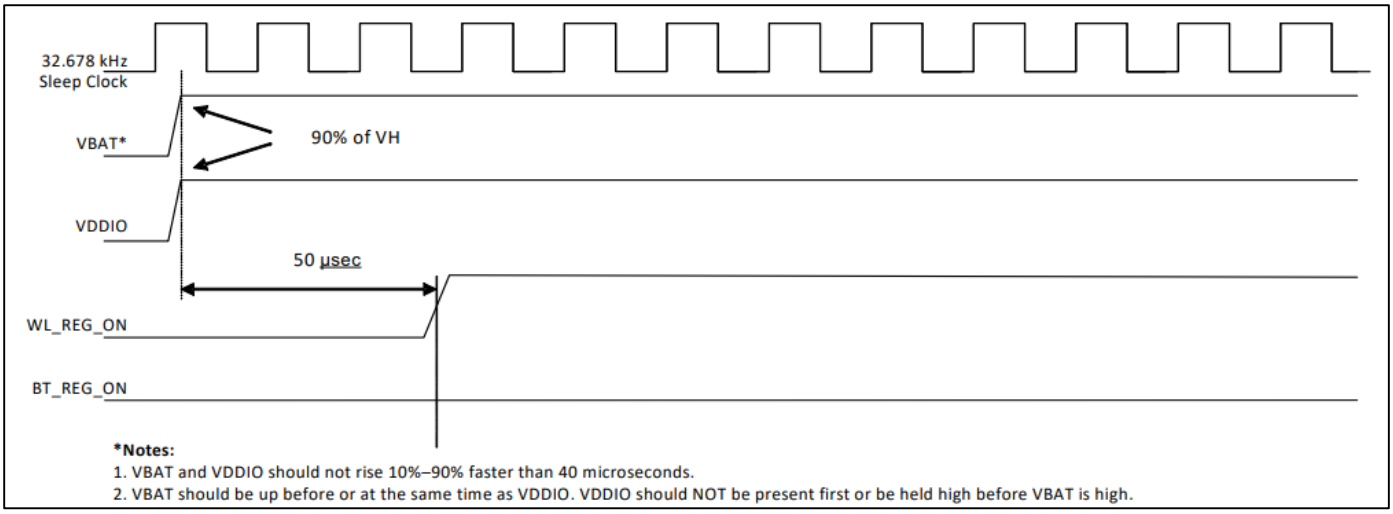


WLAN = OFF, Bluetooth = OFF



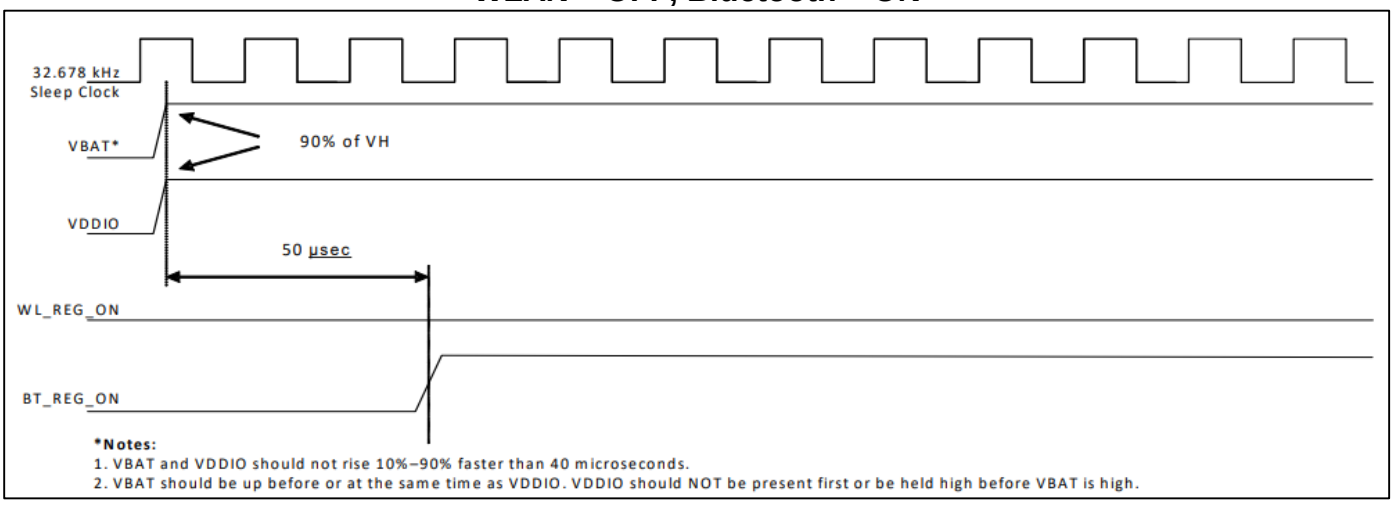
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF



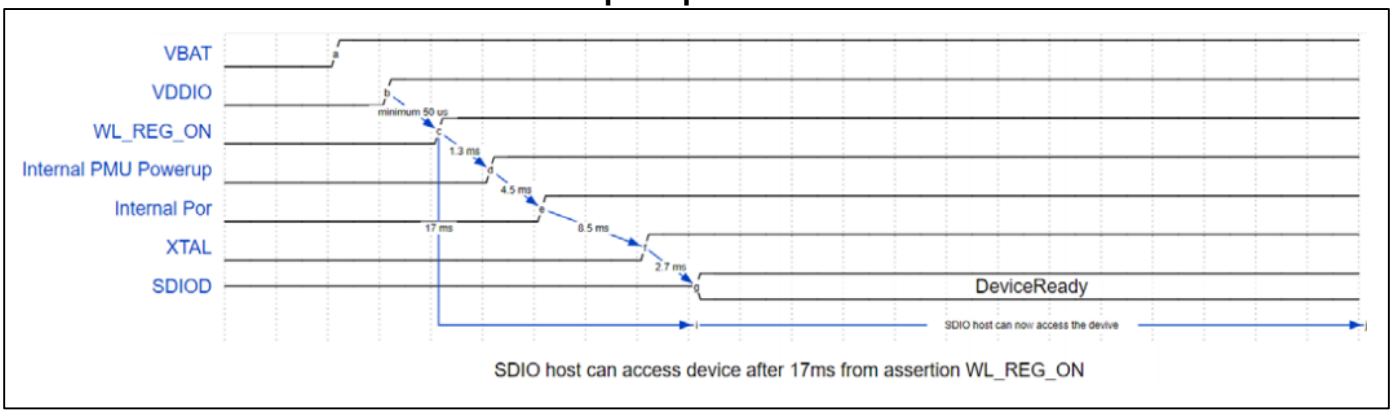
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = ON

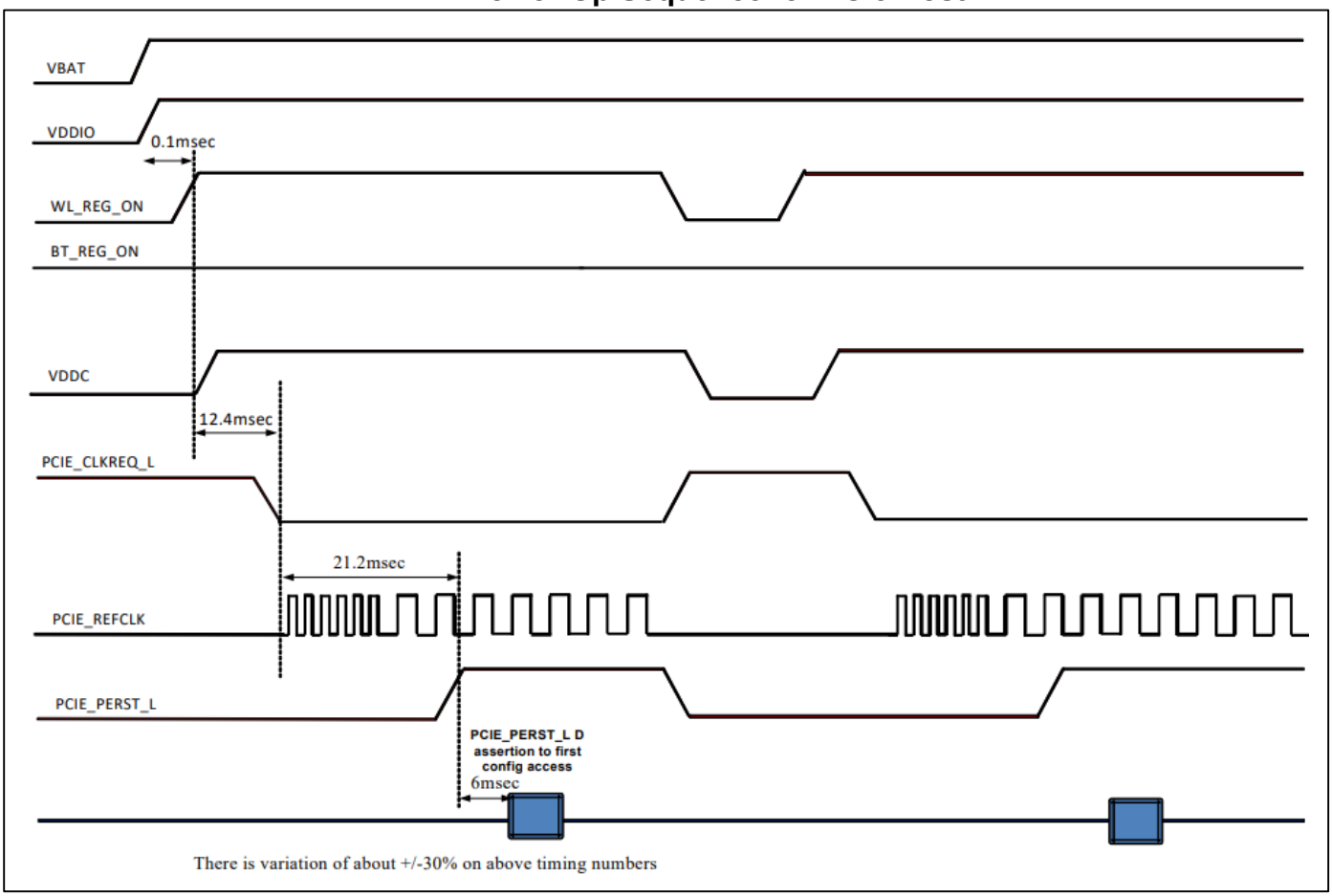


***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

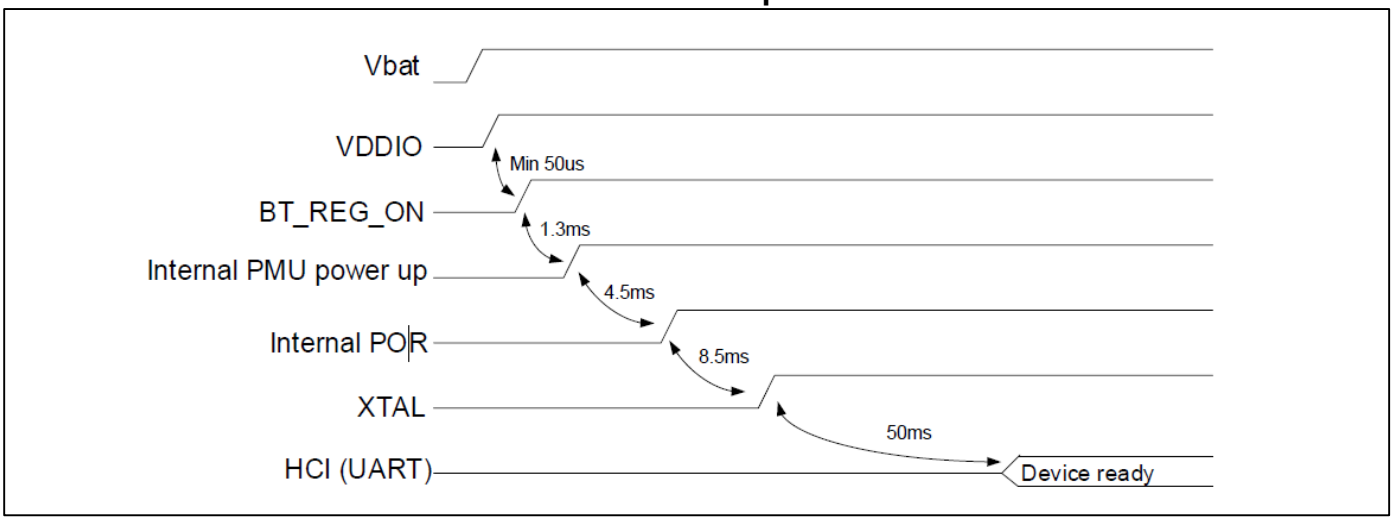
WLAN Boot-Up Sequence for SDIO Host



WLAN Power-Up Sequence for PCIe Host



Bluetooth Boot-Up for HCI



3.6 Power Consumption*

3.6.1 WLAN

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

3.6.2 Bluetooth

TBD

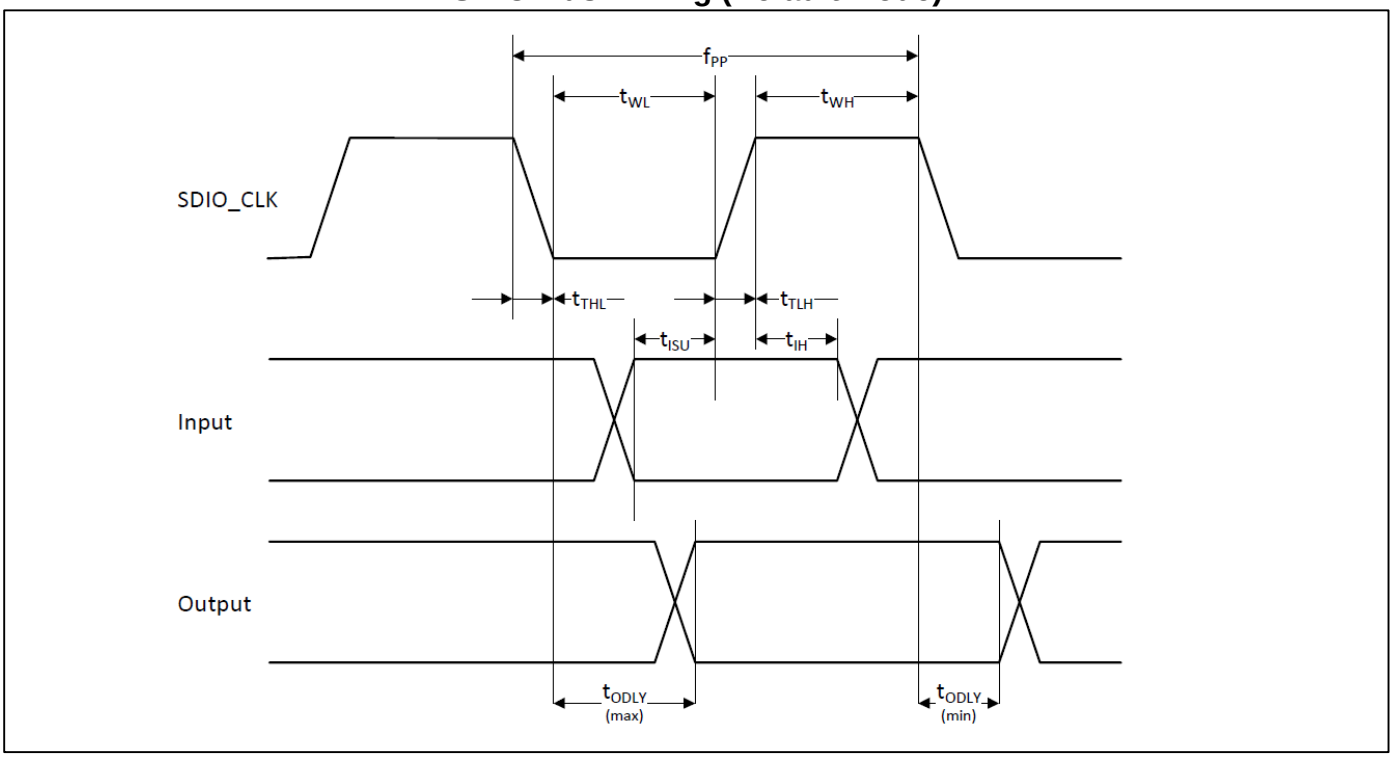
* The power consumption is based on Azurewave test environment, these data for reference only.

4. Interface Timing and AC Characteristics

4.1 SDIO Timing

■ SDIO Default Mode Timing

SDIO Bus Timing (Default Mode)



SDIO Bus Timing[1] Parameters (Default Mode)

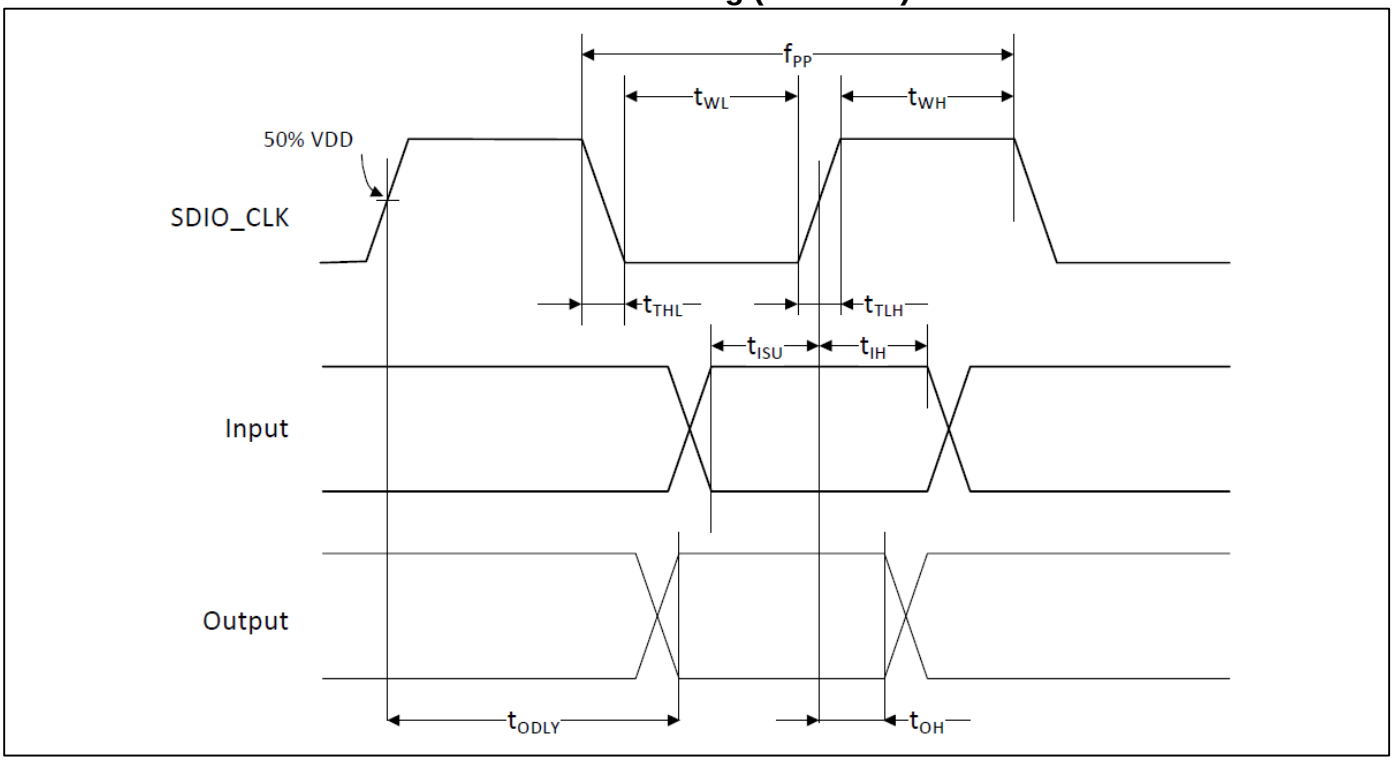
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL)[2]					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					

Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

[1] Timing is based on CL <= 40 pF load on CMD and Data..
[2] Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

■ SDIO High-speed mode timing

SDIO Bus Timing (HS Mode)



SDIO Bus Timing[1] Parameters (HS Mode)

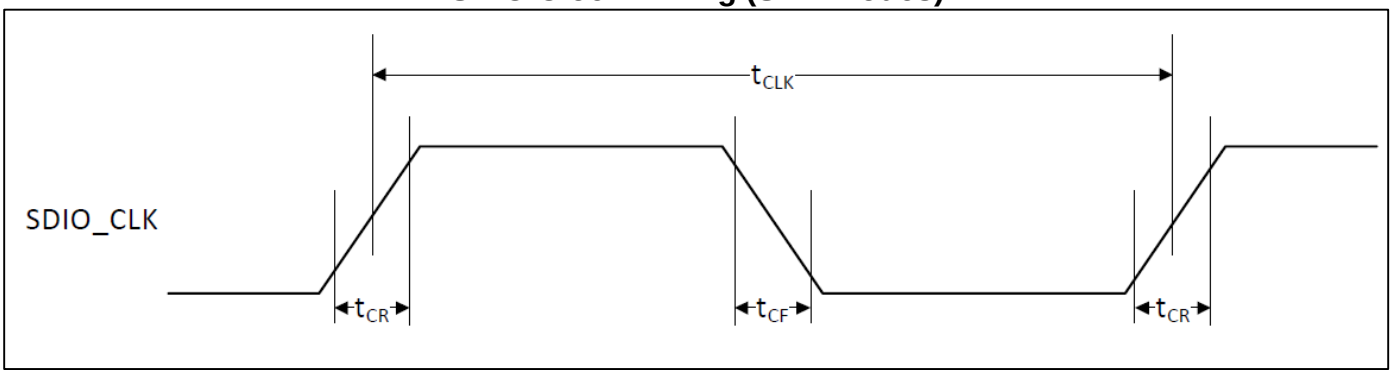
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns

Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

[1] Timing is based on CL <= 40 pF load on CMD and Data..
[2] Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

■ SDIO Bus Timing Specifications in SDR Modes (Clock Timing)

SDIO Clock Timing (SDR Modes)

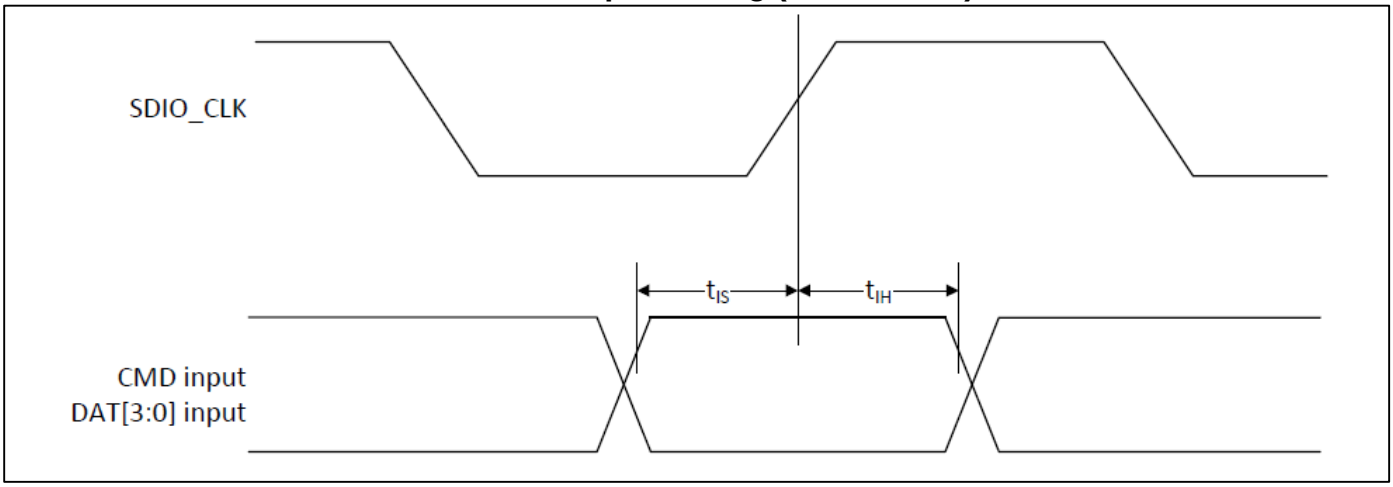


SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Minimum	Typical	Unit	Comments
–	t_{CLK}	40.0	–	ns	SDR12 mode
		20.0	–	ns	SDR25 mode
		10.0	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode

–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, CCARD = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, CCARD = 10 pF
Clock duty	–	30.0	70.0	%	–

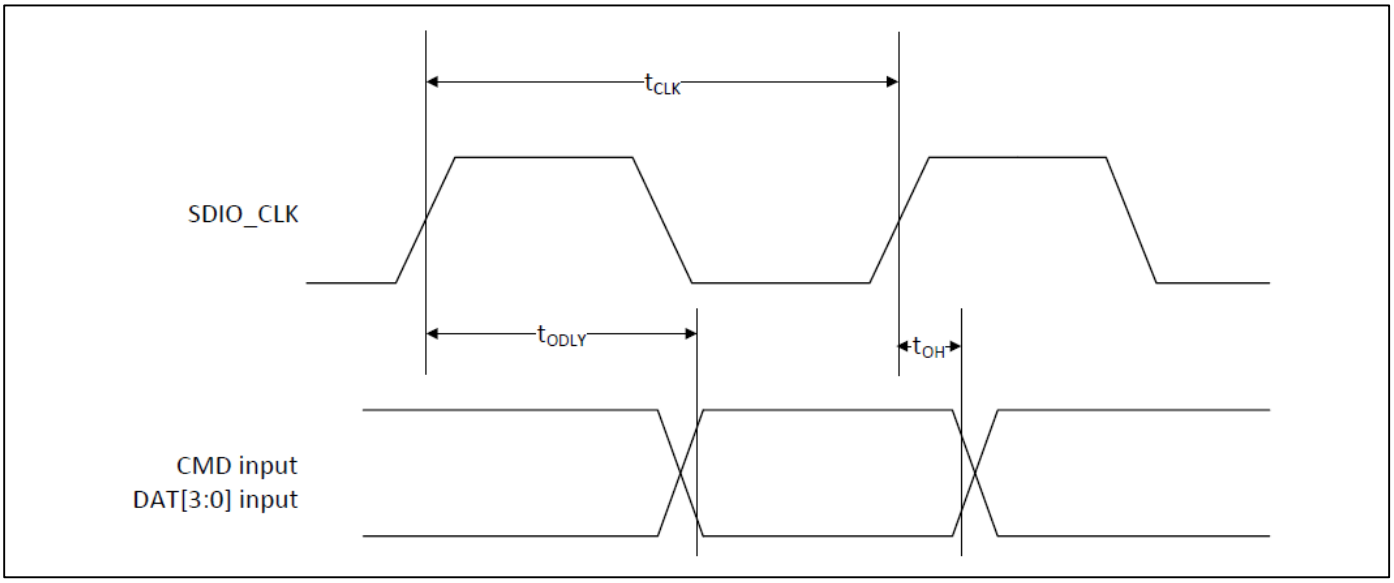
SDIO Bus Input Timing (SDR Modes)



SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975 V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975 V

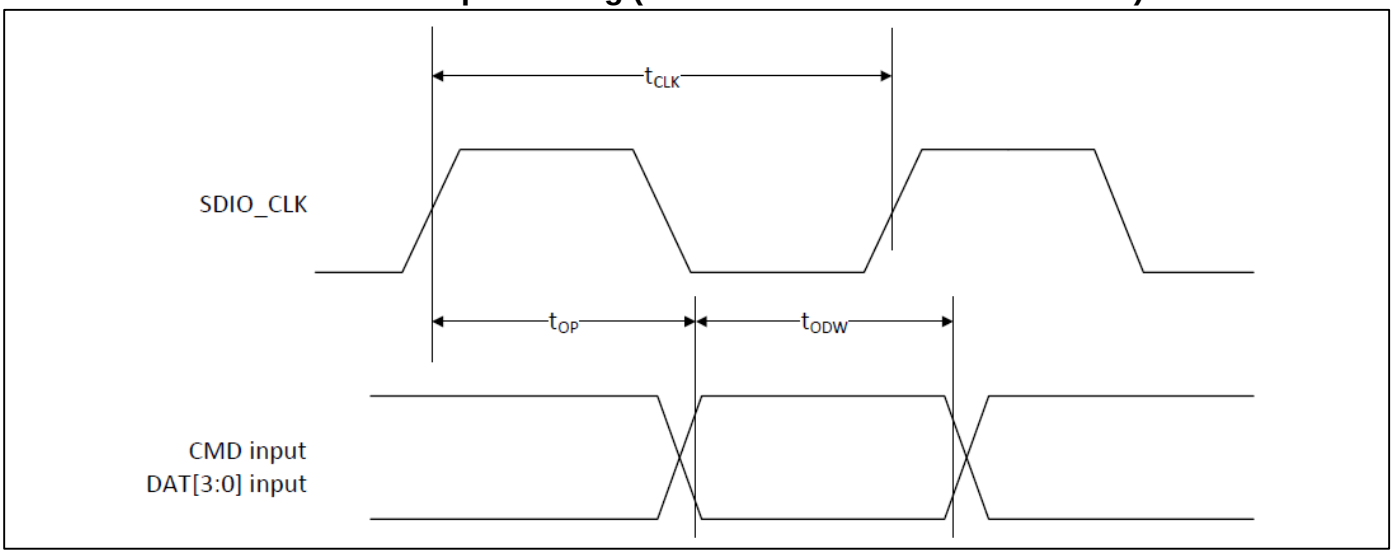
SDIO Bus Output Timing (SDR Modes up to 100 MHz)



SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq$ 10 ns CL= 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq$ 20 ns CL= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) CL= 15 pF

SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

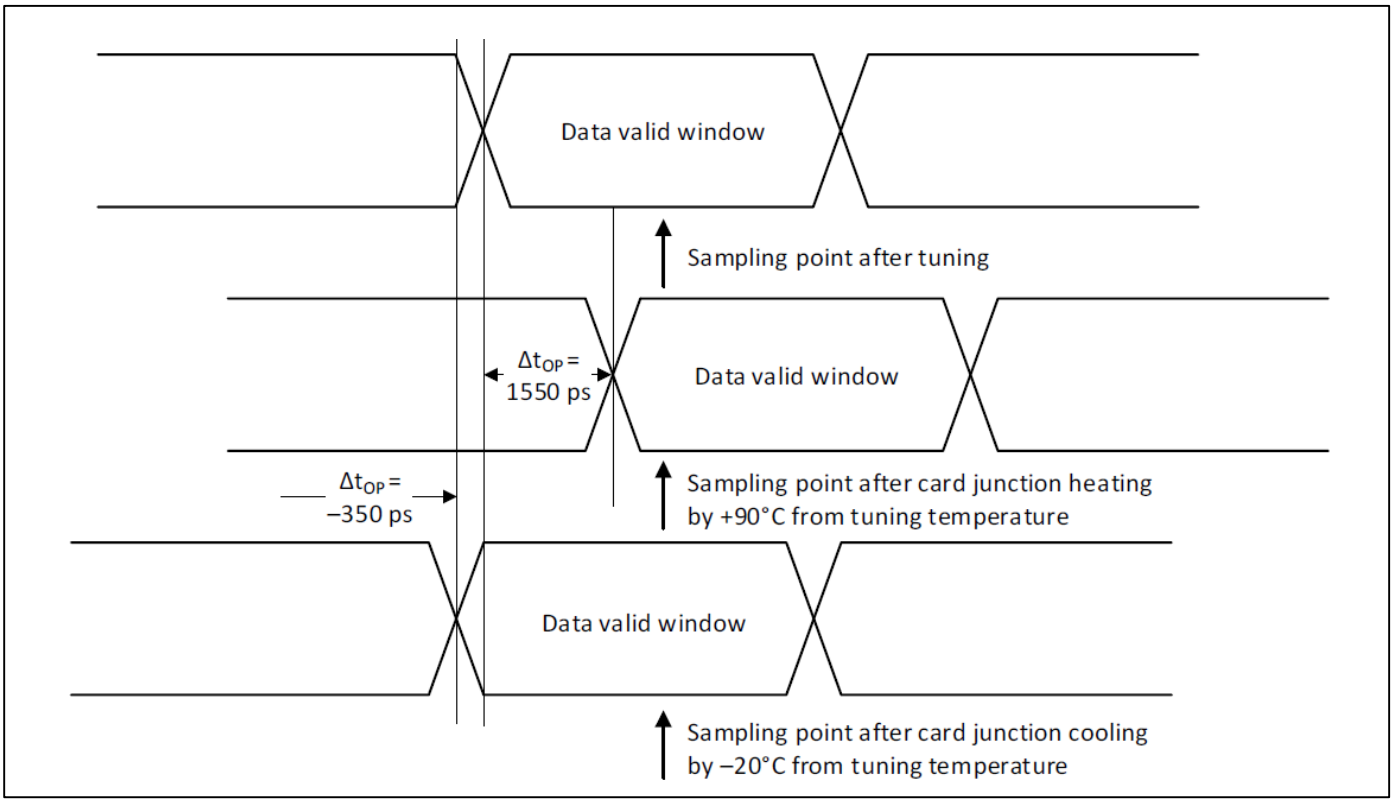


SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2.0	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

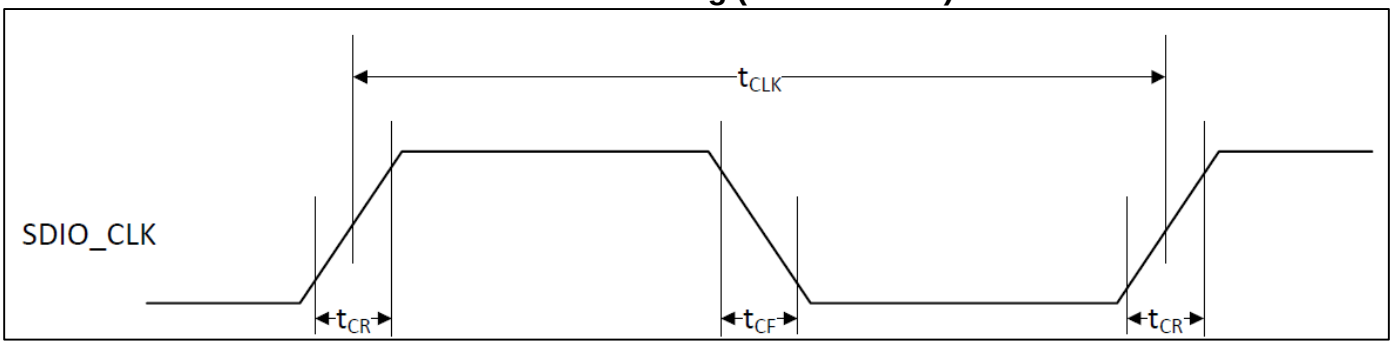
Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
Δt_{OP} = -350 ps for junction temperature of Δt_{OP} = -20 degrees during operation
Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = -20 to +125 degrees during operation

△tOP Consideration for Variable Data Window (SDR 104 Mode)



■ SDIO Bus Timing Specifications in DDR50 Mode

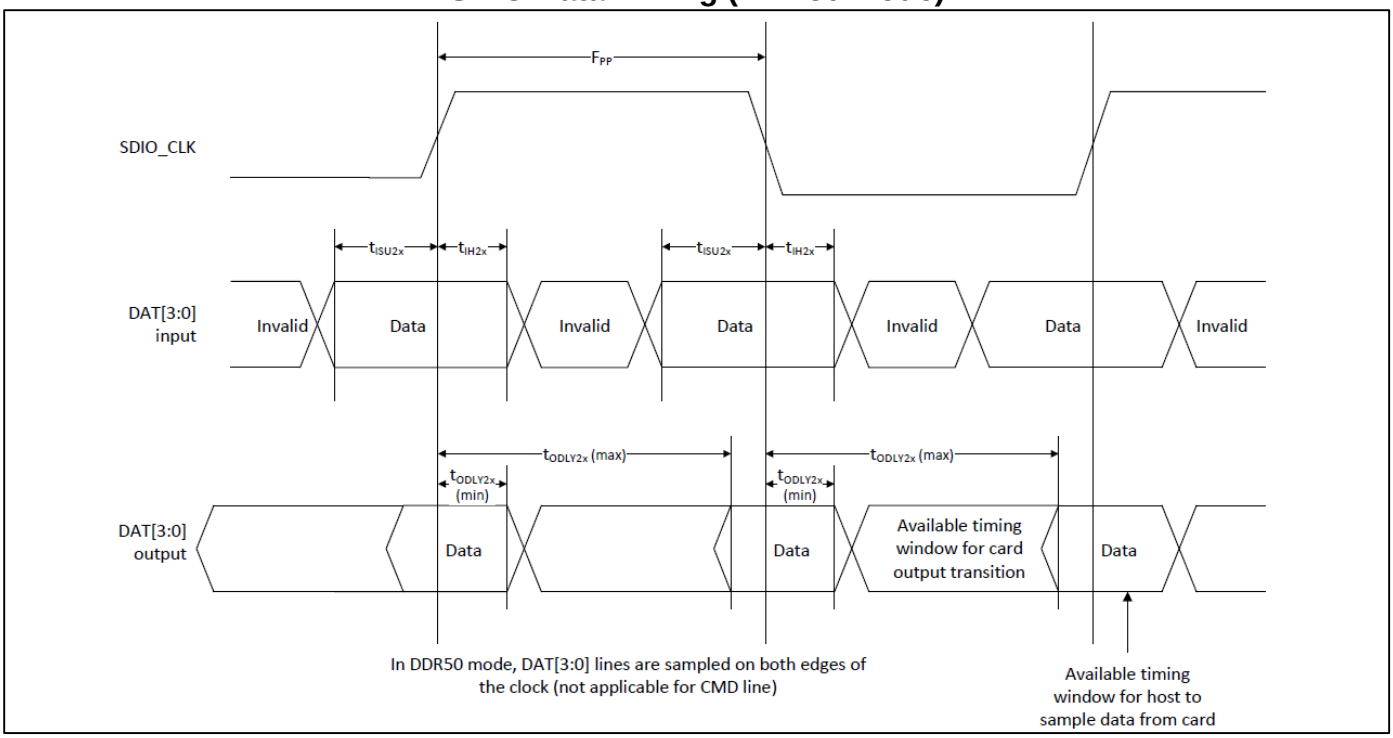
SDIO Clock Timing (DDR50 Mode)



SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20.0	–	ns	DDR50 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45.0	55.0	%	–

SDIO Data Timing (DDR50 Mode)



SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6.0	–	ns	CCARD < 10pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	CCARD < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–		ns	CCARD < 30pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	CCARD < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3.0	–	ns	CCARD < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	CCARD < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	CCARD < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	CCARD < 15pF (1 Card)

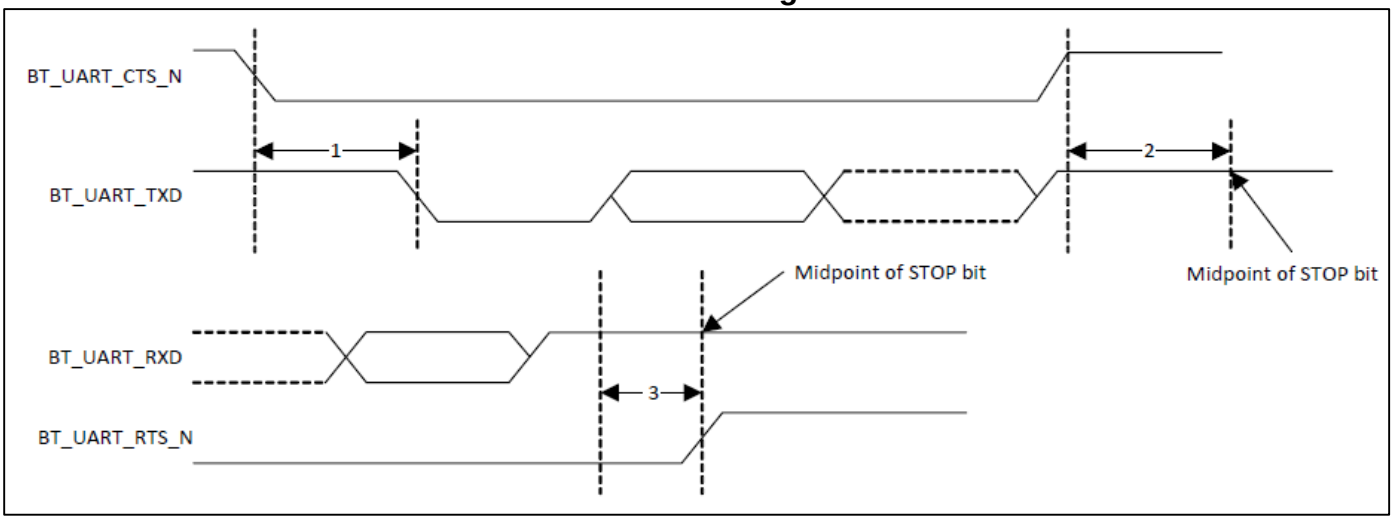
4.2 UART Interface

The AW-XHA01 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The baud rate may be selected through a vendor-specific UART HCI command.
UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.0 UART HCI specification. The default baud rate is 115.2 Kbaud.
The AW-XHA01 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.
Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-XHA01 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

UART Interface Signals

PIN No.	Name	Description	Type
F1	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	O
F2	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	I
G1	BT_UART_TXD	UART Serial Output. Serial data output for the HCI UART interface.	O
G2	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	I

UART Timing



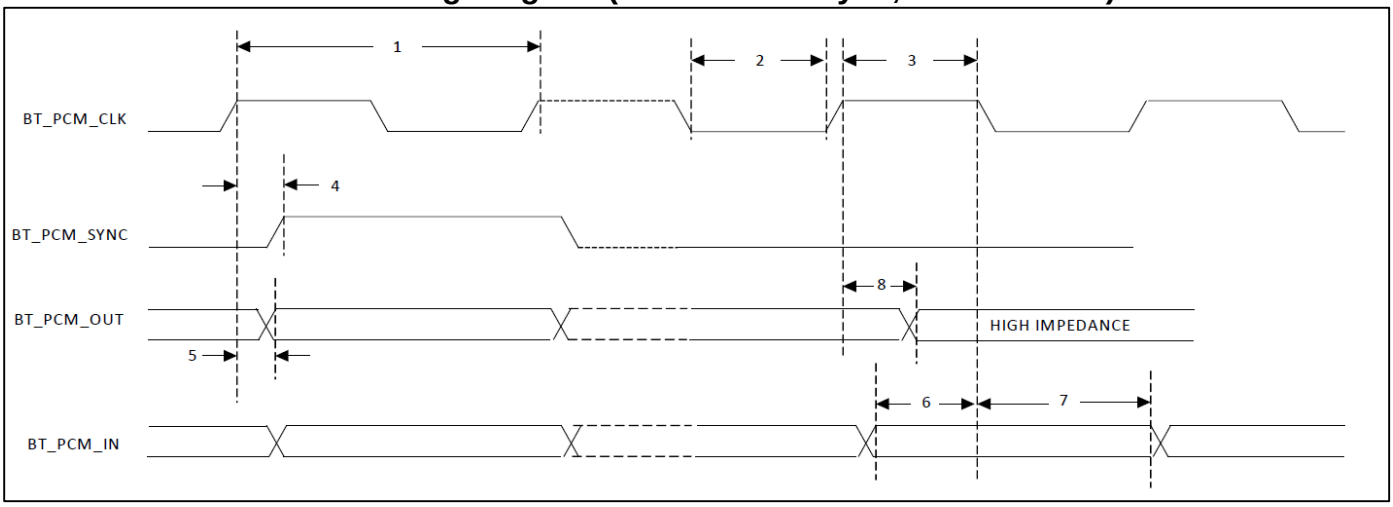
UART Timing Specifications

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

4.3 PCM Interface Timing

■ Short Frame Sync, Master Mode

PCM Timing Diagram (Short Frame Sync, Master Mode)



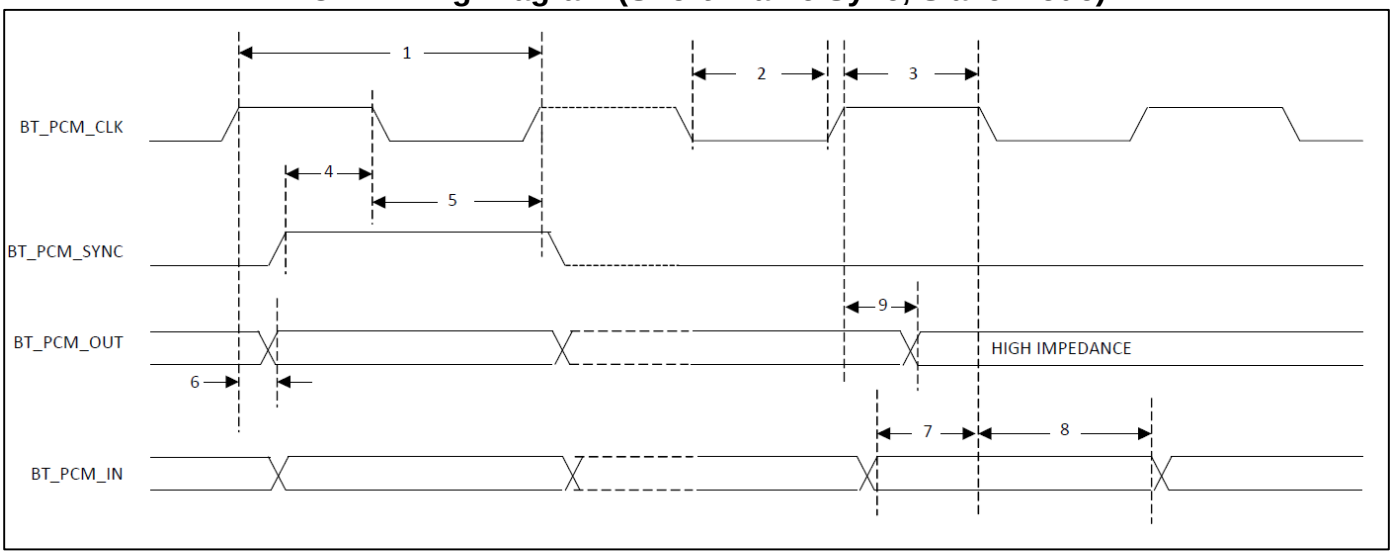
PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns

7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

■ Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

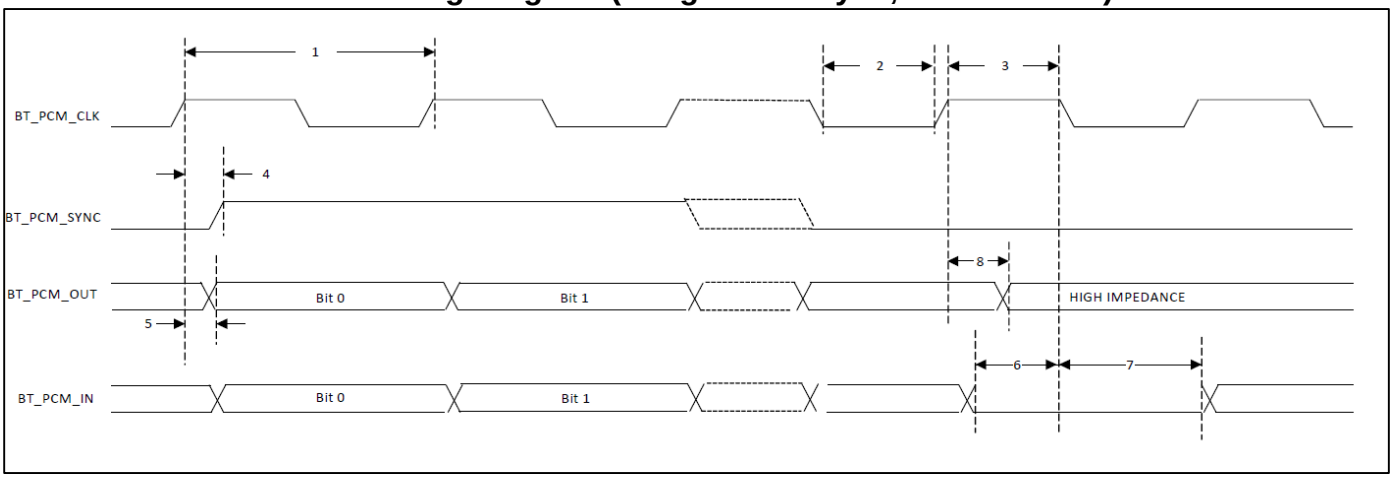


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

■ Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

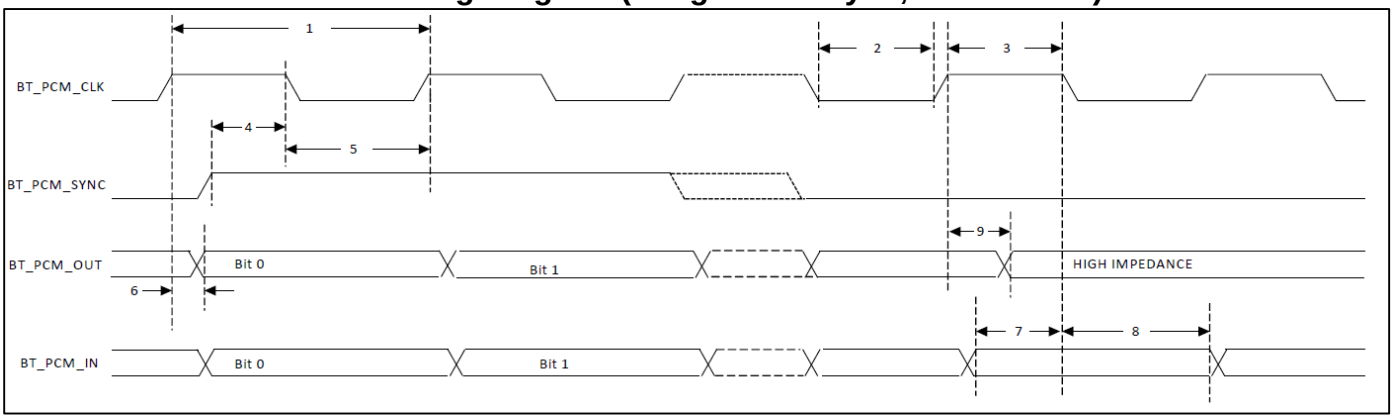


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

■ Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

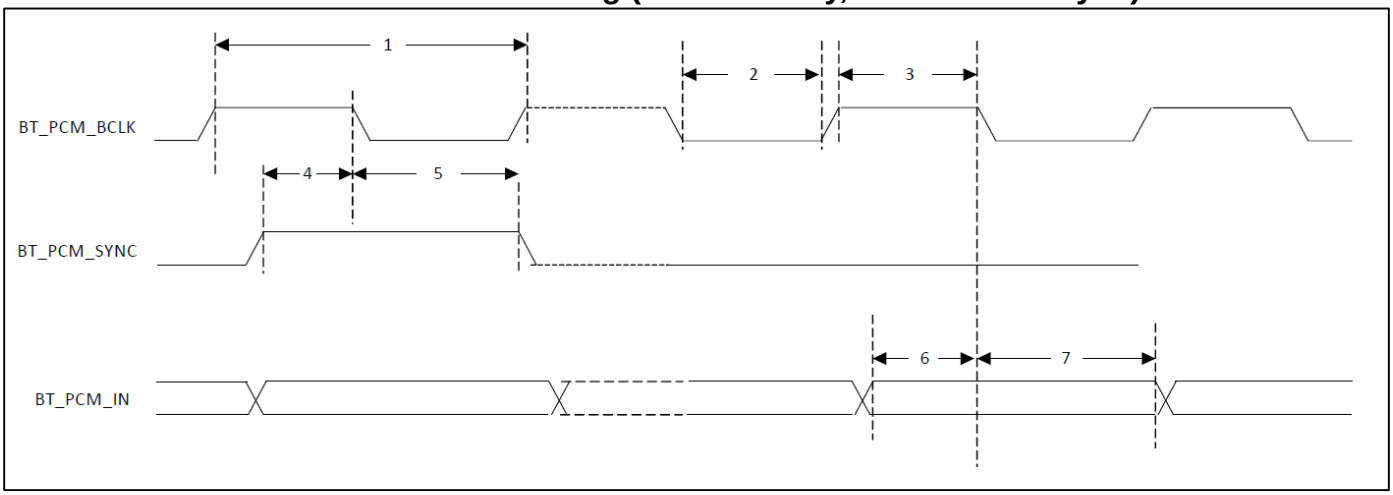


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

■ Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

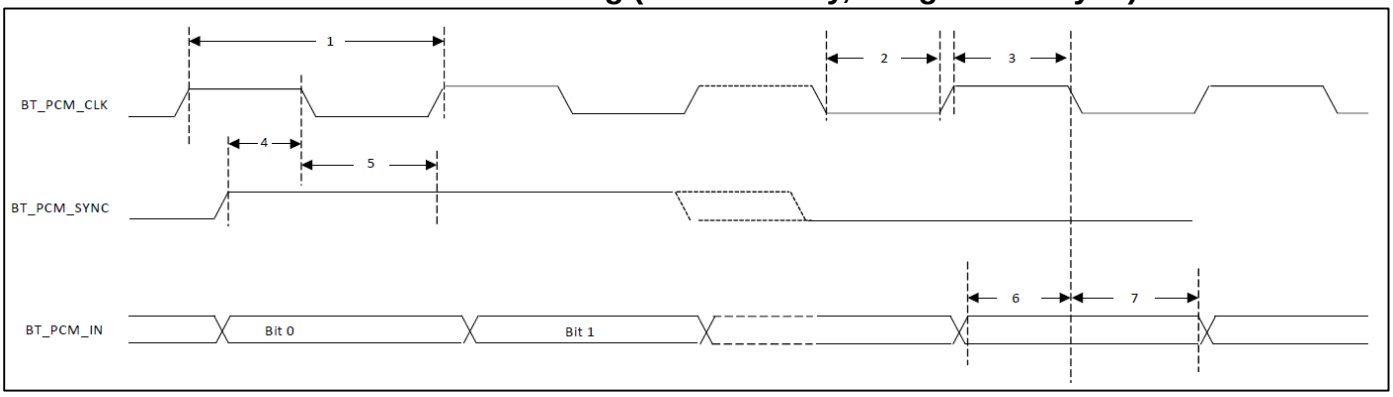


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

■ Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)

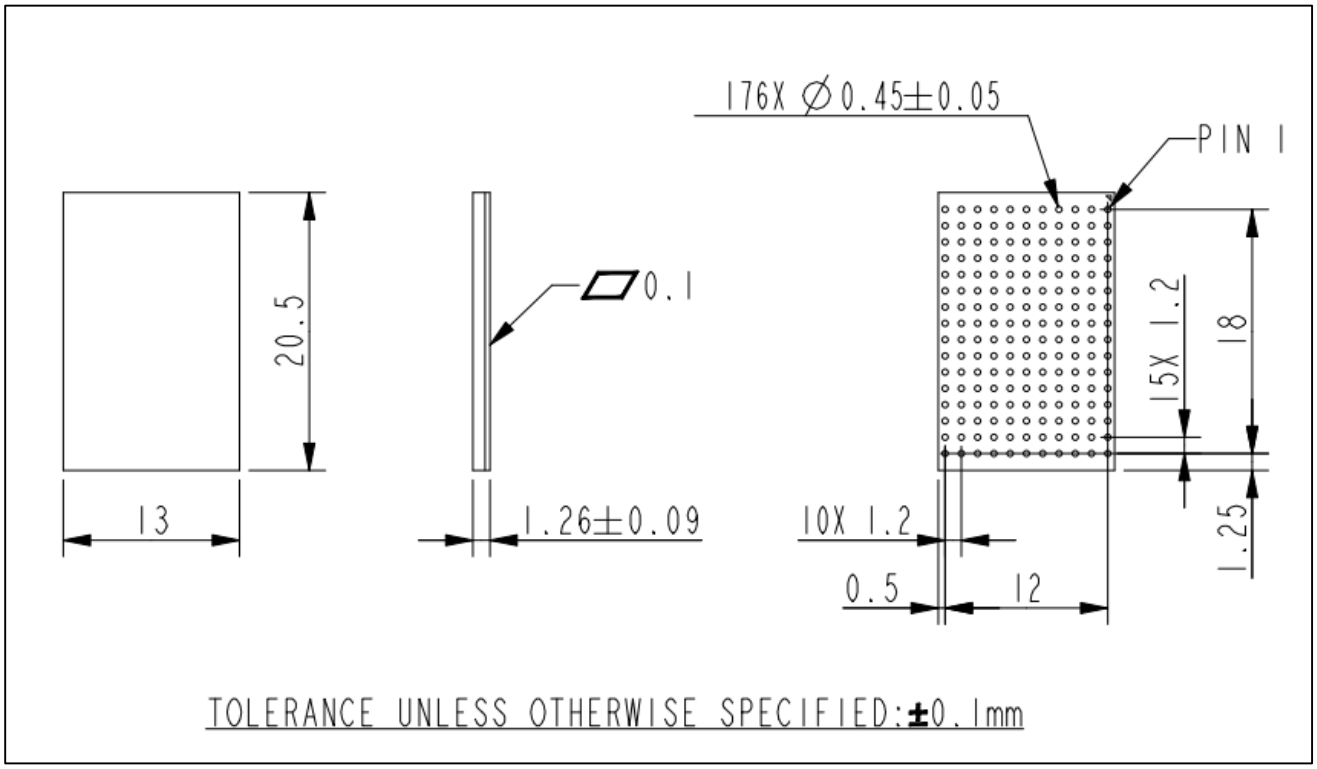


PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

5. Mechanical Information

5.1 Mechanical Drawing



6. Packaging Information

TBD