AzureWave Technologies, Inc.

AW-CU668

IEEE802.11 a/b/g/n/ac/ax and Bluetooth LE 5.4 LGA Module

Datasheet

Rev. B

DF

(For Standard)

Features

MCU

- Cortex®-M33 192 MHz runs Wi-Fi and networking stacks.
- On-chip memory has 2048-KB ROM and 768-KB RAM.
- User available code size support ~300 KB of 768 KB RAM.
- Option to boot and XIP from flash with on-the-fly AES encryption.
- ModusToolbox™ supporting ThreadX RTOS.
- TCP/IP (NetXDuo), TLS 1.3 (NetXSecure), HTTP(S), MQTT support.
- 40 Mbps throughput with TCP/IP, TLS over SDIO.
- 20 Mbps throughput with TCP/IP, TLS over gSPI.
- 4 Mbps throughput with TCP/IP, TLS over SCB UART.

Wi-Fi

- IEEE 802.11a/b/g/n/ac/ax compliant
- Tri-band (2.4 GHz/5~7 GHz)
- 1x1 with 20 MHz channels supporting PHY data rates up to 802.11ax (MCS11 1024-QAM 5/6)
- Transmit (TX) power with internal PA
  - 2.4 GHz: +TBD dBm 1 Mbps DSSS
  - 5 GHz: +TBD dBm 6 Mbps OFDM
- Sensitivity with internal LNA
  - 2.4 GHz: TBD dBm 1 Mbps DSSS
  - 5 GHz: TBD dBm MCS0
- Wi-Fi 6 release features
  - OFDMA uplink and downlink as STA
  - Downlink multi-user MIMO as STA
  - Individual target-wake-time (TWT)
  - BSS color
- Support for switched antenna diversity.
- Interface
  - SDIO shared between Wi-Fi and Bluetooth®
- Mode support:
  - STA
  - SoftAP
  - Wi-Fi Direct
- Security
- TKIP, WEP, WPA2(Personal/Enterprise), WPA3 (Personal/192b)

Bluetooth

- Bluetooth® 5.4 (Bluetooth® Low Energy)
- Bluetooth® 5.0/5.1/5.2/5.3/5.4 features
  - LE long range
  - LE 2 Mbps
  - LE mesh
  - Advertising extensions
  - LE Isochronous Channels
- Bluetooth® LNA can be shared with WLAN LNA for reduced antenna count

- Dedicated Bluetooth® LNA for improved RF and coexistence performance
- +4, +13, and +19 dBm Bluetooth® PA paths optimized for best efficiency, output power options adjustable in 4 dB steps
- Receive sensitivity: Bluetooth® LE 125 kbps TBD dBm
- Bluetooth® LE supported over SDIO shared with Wi-Fi - Four audio controllers available through two audio interfaces.
- TDM1, TDM2 supporting inter-IC sound (I2S) (2-channels) and PCM (8-channels), 8k to 96k sample rates, and 16- and 24-bit sample widths.
- Bidirectional PCM (TDM and I2S) with 8k, 16k sample rates and 16-bit sample width. Multiplexed with TDM2 through second audio interface.
- Single-direction I2S with 48k sample rates and 16-bit sample width. Multiplexed with TDM2 through second audio interface.

Revision History

Document NO: R2-2668-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2024/9/12	DCN032439	● Initial version	Licheng Wang	Renton Tao
B	2025/2/10	DCN033426	● Modify Title ● Remove BER/EDR description. ● Modify 1.3 frequency range, modulation, data rate, security and Bluetooth description. ● Update chapter 2.3 and chapter 3.5.	Licheng Wang	Renton Tao
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1. Introduction

1.1 Product Overview

The AW-CU668 is a ultra-lower power, single-chip, connected MCUs that support 1x1 Wi-Fi 6E, Bluetooth® Low Energy 5.4, Matter, IP networking, with integrated PMU, targeted at Internet-of-Things (IoT) applications for stand-alone operation or to offload a host-processor. An integrated 192 MHz Arm® Cortex®-CM33, runs the Wi-Fi and Networking Stacks, Bluetooth® LE 5.4 and supports a wide array of peripherals. The Wi-Fi supports single stream, 1x1, Wi-Fi 6E (802.11ax), with PHY rates up to 1024 QAM (MCS11) over 20-MHz channels. Included on-chip are 2.4 GHz and 5-6 GHz transmit power amplifiers (PAs), and low-noise amplifiers (LNAs) for best-in-class RF performance. The AW-CU668 supports Tri-Band operation (2.4 GHz and 5-7 GHz).

The AW-CU668 supports Bluetooth® LE 5.4 with support for LE 1 Mbps, LE 2 Mbps, low-energy mesh, low-energy long range (LR), and advertising extensions. The device includes on-chip power amplifiers supporting three different output power paths optimized for best efficiency, 0 dBm, +13 dBm, and +19 dBm path for driving poor antennas in wearable devices or other applications that require longer range for Bluetooth® LE. The device also features a flexible Bluetooth® receiver offering a dedicated Bluetooth® path or a Bluetooth® receive path that can be shared (sLNA) with the 2.4-GHz WLAN receive path.

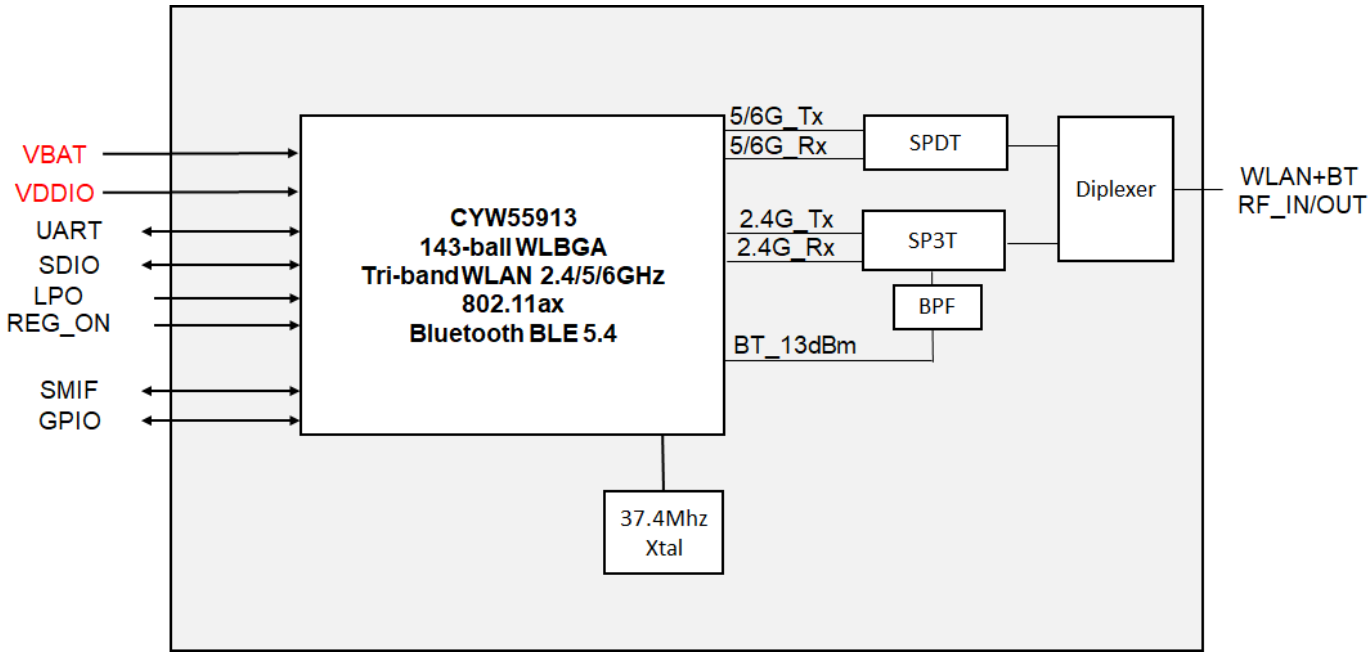
The integrated Arm® Cortex®-CM33 can operate up to 192 MHz, supporting 2048 KB of ROM, 768 KB of SRAM, running Wi-Fi and networking stacks utilizing ThreadX RTOS, NetX Duo TCP/IP network stack and NetX Secure for TLS 1.3 with Arm® Trustzone CryptoCell312. +300 KB of on-chip SRAM is available for customer application code, with optional XIP from external flash with on-the-fly encryption over SMIF if more application space is required. The device is capable to support > 40 Mbps of throughput over SDIO, >20 Mbps over GSPI, or > 4 Mbps over SPI running all Wi-Fi and Networking stacks. The device also supports three Serial Control Blocks (SCB) which each

SCB supporting I2C/SPI/UART, 9x TCPWM blocks, PDM interface for digital microphone support, 12-bit ADC with seven channel mux input for analog microphone support or seven channels of DC sensing. A pair of time-division multiplexing (TDM) interfaces enables a flexible interface for various audio use cases and a PDM interface is available for connecting digital microphones. AW-CU668 does not support Bluetooth® LE Audio. See the AW-CU668 for devices requiring Bluetooth® BR/EDR and Bluetooth® LE Audio support. A 4-wire UART or SDIO (shared with Wi-Fi) interface is available for interfacing with the host processor.

The AW-CU668 also includes a power management unit (PMU) and requires a 37.4 MHz crystal which provides the system reference clock and can operate from an internal high-accuracy (~1%) and external 32.76 kHz crystal (eLPO) for higher accuracy from an external reference clock. The AW-CU668 includes advanced coexistence hardware mechanisms and algorithms which ensure WLAN and Bluetooth® LE simultaneous operation is optimized for maximum performance. In addition, coexistence support is available for external radios such as (LTE, GPS, and ZigBee) via an external interface. The AW-CU668 operates over -40~+85 temperature range.

1.2 Block Diagram

1.2.1 Block Diagram



AW-CU668 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11a/b/g/n/ac/ax Wi-Fi with Bluetooth Combo LGA Module
Major Chipset	Infineon CYW55913 (wlbga 143b)
Host Interface	MCU: SDIO/UART
Dimension	12mm(L)x 12xmm(W) x 1.75 mm(H) (Typical)
Form factor	LGA, 63 pin
Antenna	1T1R for Wi-Fi / BT ANT : RF pad out for Wi-Fi / Bluetooth BLE→ TX/RX
Weight	0.48g (Typical)

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac/ax, Wi-Fi compliant
Frequency Rage	WLAN: 2.4 / 5 / 6 GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9), 1024-QAM(MCS10~11)
Number of Channels	**2.4GHz** ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13 **5GHz** ■ USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165 **6GHz** ■ CH1~CH233

Output Power[1][2] (Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<35%		TBD		dBm
11g (54Mbps) @EVM≦-25 dB		TBD		dBm
11n (HT20 MCS7) @EVM≦-27 dB		TBD		dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM≦-25 dB		TBD		dBm
11n (HT20 MCS7) @EVM≦-27 dB		TBD		dBm
11ac (VHT20 MCS8) @EVM≦-30 dB		TBD		dBm
11ax (HE20 MCS11) @EVM≦-32 dB		TBD		dBm

6G

	Min	Typ	Max	Unit
11ax (HE20 MCS11) @EVM≦-32 dB		TBD		dBm

Receiver Sensitivity

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		TBD		dBm
11g (54Mbps)		TBD		dBm
11n (HT20 MCS7)		TBD		dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		TBD		dBm
11n (HT20 MCS7)		TBD		dBm
11ac[3] (VHT20 MCS8)		TBD		dBm

[1] EVM Spec are under typical test conditions.
[2] Output Power means measurement power inside the range (Min and Max) with spectral mask and EVM compliance.
[3] Tested by BCC instead of LDPC.

	11ax[4] (HE20 MCS11) | | TBD | | dBm **6G** | | Min | Typ | Max | Unit | | 11ax (HE20 MCS11) | | TBD | | dBm |
Data Rate	WLAN: 802.11b : 1, 2, 5.5, 11Mbps 802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n : MCS0~7 (20MHz channel) 802.11ac : MCS0~8 (20MHz channel) 802.11ax : MCS0~11 (20MHz channel)
Security	TKIP, WEP, WPA2(Personal/Enterprise), WPA3 (Personal/192b).

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	**Description**
Bluetooth Standard	BLE 5.4
Bluetooth VID/PID	N/A
Frequency Range	2402MHz~2483MHz
Modulation	GFSK, 1M GFSK, 2M GFSK, 500kbps GFSK, 125kbps
Output Power	| | Min | Typ | Max | Unit | | BLE(1M) | | TBD | | dBm | | BLE(2M) | | TBD | | dBm | | BLE(500k) | | TBD | | dBm | | BLE(125k) | | TBD | | dBm |
Receiver Sensitivity[5]	| | Min | Typ | Max | Unit | | BLE(1M) | | TBD | | dBm | | BLE(2M) | | TBD | | dBm | | BLE(500k) | | TBD | | dBm | | BLE(125k) | | TBD | | dBm |

[4] Tested by BCC instead of LDPC.

[5] Tested by sLNA.

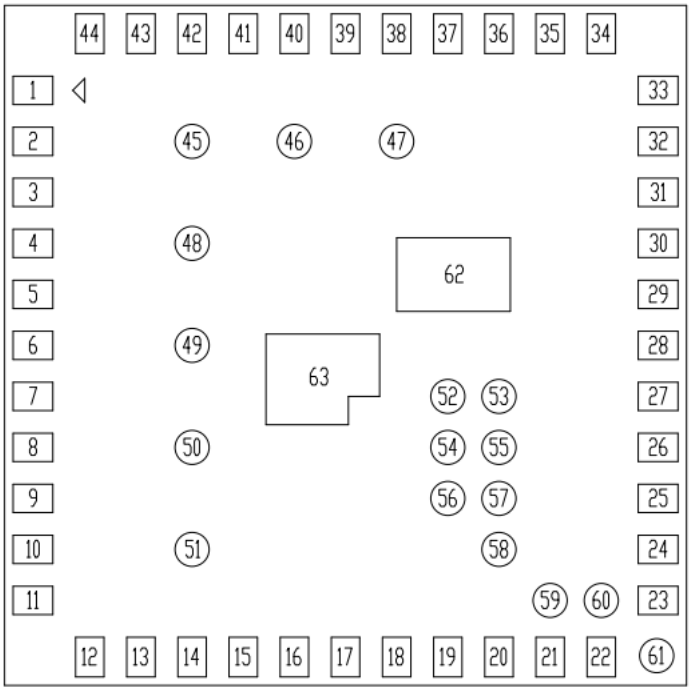
1.3.4 Operating Conditions

Operating Conditions	
Voltage	Power supply for host:3.3V
Operating Temperature	-40~+85 ℃[6]
Operating Humidity	less than 85% R.H.
Storage Temperature	-40~+125 ℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	+/- 2 KV per JEDEC EID/JESD22-A114
Changed Device Model	+/- 300 V per JEDEC EIA/JESD22-C101

[6] TBD℃ is Functional operation, for detail please check with AzureWave FAE.

2. Pin Definition

2.1 Pin Map



AW-CU668 Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	Ground.		GND
2	ANT	2.4G/5G/6G RF_IN/OUT pad.		RF
3	GND	Ground.		GND
4	Reserved	Reserved, do not connect.		
5	BT_GPIO_5	GPIO configuration pin.	VDDIO	I/O
6	GPIO0_WL_HOST_WAKE	GPIO configuration pin.	VDDIO	I/O
7	VDDIO	1.8V VDDIO supply for WLAN and BT.	VDDIO	Power
8	REG_ON	Regulator on, active low.	VDDIO	I
9	VBAT	3.3V main power supply.		Power
10	GND	Ground.		GND
11	ASR_VLX	ASR power stage output to inductor.		O
12	ASR_VLX_IN	Input of ASR power stage.		I
13	GND	Ground.		GND
14	SDIO_DATA_2	SDIO Data Line 2	VDDIO	I/O
15	SDIO_DATA_1	SDIO Data Line 1	VDDIO	I/O
16	SDIO_DATA_0	SDIO Data Line 0	VDDIO	I/O
17	SDIO_DATA_CLK	SDIO Clock Input	VDDIO	I
18	SDIO_DATA_CMD	SDIO Command Input	VDDIO	I/O
19	SDIO_DATA_3	SDIO Data Line 3	VDDIO	I/O
20	GND	GPIO configuration pin	VDDIO	I/O
21	SMIF_SPHB_CLK	SMIF_SPHB_CLK,	VDDIO	I/O
22	SMIF_SPHB_DQ2	SMIF_SPHB_DQ2	VDDIO	I/O
23	SMIF_SPHB_DQ0	SMIF_SPHB_DQ0	VDDIO	I/O

24	SMIF_SPHB_DQ3	SMIF_SPHB_DQ3	VDDIO	I/O
25	SMIF_SPHB_DQ1	SMIF_SPHB_DQ1	VDDIO	I/O
26	SMIF_SPHB_CS0	SMIF_SPHB_CS0	VDDIO	I/O
27	SMIF_SPHB_CS1	SMIF_SPHB_CS1	VDDIO	I/O
28	BT_GPIO7	GPIO configuration pin.	VDDIO	I/O
29	BT_GPIO0	GPIO configuration pin.	VDDIO	I/O
30	LHL_GPIO_8	GPIO configuration pin.	VDDIO	I/O
31	GND	Ground.		GND
32	LHL_GPIO_3	GPIO configuration pin.	VDDIO	I/O
33	LPO_IN	32.768KHz input.	200~3200Vpp	I
34	WL_DEV_WAKE	GPIO configuration pin.	VDDIO	I/O
35	BT_DEV_WAKE	GPIO configuration pin.	VDDIO	I/O
36	LHL_GPIO_4	GPIO configuration pin.	VDDIO	I/O
37	BT_HOST_WAKE	GPIO configuration pin.	VDDIO	I/O
38	BT_GPIO_3	GPIO configuration pin.	VDDIO	I/O
39	Reserved_39	Reserved, do not connect.		
40	BT_UART_RXD	UART_RX.	VDDIO	I
41	BT_UART_CTS	UART_CTS	VDDIO	I
42	BT_UART_RTS	UART_RTS	VDDIO	O
43	BT_UART_TXD	UART_TXD	VDDIO	O
44	BT_GPIO_6	GPIO configuration pin.	VDDIO	I/O
45	TP1	No connect.		
46	TP2	No connect.		
47	TP3	No connect.		
48	GND	Ground.		GND
49	GND	Ground.		GND
50	LHL_GPIO_2	GPIO configuration pin.	VDDIO	I/O

51	GND	Ground.		GND
52	LHL_GPIO_5	GPIO configuration pin.	VDDIO	I/O
53	LHL_GPIO_9	GPIO configuration pin.	VDDIO	I/O
54	BT_GPIO_4	GPIO configuration pin.	VDDIO	I/O
55	LHL_GPIO_6	GPIO configuration pin.	VDDIO	I/O
56	BT_GPIO_2	GPIO configuration pin.	VDDIO	I/O
57	BT_GPIO_17	GPIO configuration pin.	VDDIO	I/O
58	BT_GPIO_16	GPIO configuration pin.	VDDIO	I/O
59	GND	Ground.		GND
60	GND	Ground.		GND
61	GND	Ground.		GND
62	GND	Ground.		GND
63	GND	Ground.		GND

2.3 Pin Multiplexing Tables

Multiple usage pins are used to conserve pin consumption for different features. The AW-CU640 devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be used as a GPIO pin as well.

Table 1 (BT_UART)

No.	Pin Name	FUNCTION#1	FUNCTION#5	FUNCTION#6
41	BT_UART_CTS_N	BT_UART_CTS_N	SCB0-SPI_SEL0	SCB0_UART_CTS
42	BT_UART_RTS_N	BT_UART_RTS_N	SCB0-SPI_CLK	SCB0_UART_RTS
40	BT_UART_RXD	BT_UART_RXD	SCB0-SPI_MOSI	SCB0_UART_RXD
43	BT_UART_TXD	BT_UART_TXD	SCB0-SPI_MISO	SCB0_UART_TXD

Table 2 (BT_GPIO)

No.	Pin Name	FUNCTION#1	FUNCTION#4	FUNCTION#5	FUNCTION#7	FUNCTION#8	FUNCTION#9
29	BT_GPIO_0						
37	BT_HOST_WAKE	BT_GPIO_1					
56	BT_GPIO_2			SCB0-SPI_SEL3	SCB1-SDA	SCB1-SPI_MISO	SCB1_UART_RXD
38	BT_GPIO_3				SCB1-SCL	SCB1-SPI_MOSI	SCB1_UART_TXD
54	BT_GPIO_4		SCB0-SDA	SCB0-SPI_SEL2			SCB1_UART_CTS
5	BT_GPIO_5		SCB0-SCL	SCB0-SPI_SEL1			SCB1_UART_RTS
44	BT_GPIO_6					SCB1-SPI_SEL3	
28	BT_GPIO_7					SCB1-SPI_SEL2	
58	BT_GPIO_16				SCB1-SCL	SCB1-SPI_SEL0	
57	BT_GPIO_17				SCB1-SDA	SCB1-SPI_CLK	

Table 2 (BT_GPIO) continued

No.	Pin Name	FUNCTION#10	FUNCTION#11	FUNCTION#13
29	BT_GPIO_0		SCB2-SPI_SEL3	TCPWM_TR_ALL_5
37	BT_HOST_WAKE			TCPWM_TR_ALL_6
56	BT_GPIO_2			TCPWM_TR_ALL_7
38	BT_GPIO_3			TCPWM_TR_ALL_8
54	BT_GPIO_4			TCPWM_OUT_11
5	BT_GPIO_5			TCPWM_OUT_12
44	BT_GPIO_6	SCB2-SDA		TCPWM_OUT_21
28	BT_GPIO_7	SCB2-SCL		TCPWM_OUT_22
58	BT_GPIO_16			TCPWM_OUT_12/ TCPWM_COMP_OUT_12
57	BT_GPIO_17			TCPWM_OUT_11/ TCPWM_COMP_OUT_21

Table 3 (LHL_GPIO)

No.	Pin Name	FUNCTION#0	FUNCTION#1	FUNCTION#3	FUNCTION#4	FUNCTION#5
34	WL_DEV_WAKE	LHL_GPIO_0				
35	BT_DEV_WAKE	LHL_GPIO_1				
50	LHL_GPIO_2	ADCIn0	LP_COMP_IN_N			
32	LHL_GPIO_3	ADCIn1	LP_COMP_IN_N			
36	LHL_GPIO_4	ADCIn2	LP_COMP_IN_N	DMIC_CK		SCB0-SPI_MOSI
52	LHL_GPIO_5	ADCIn3	LP_COMP_IN_N	DMIC_DQ		SCB0-SPI_MISO
55	LHL_GPIO_6	ADCIn4	LP_COMP_IN_N		SCB0-SCL	SCB0-SPI_SEL0
30	LHL_GPIO_8	ADCIn6	LP_COMP_IN_N			
53	LHL_GPIO_9	ADCIn7	LP_COMP_IN_N			

Table 3 (LHL_GPIO) continued

No.	Pin Name	FUNCTION#8	FUNCTION#9	FUNCTION#10	FUNCTION#13	FUNCTION#14
34	WL_DEV_WAKE					
35	BT_DEV_WAKE					
50	LHL_GPIO_2		SCB1_UART_TXD		TCPWM_TR_ALL_1	
32	LHL_GPIO_3		SCB1_UART_RXD		TCPWM_TR_ALL_2	
36	LHL_GPIO_4		SCB1_UART_CTS		TCPWM_TR_ALL_4	
52	LHL_GPIO_5		SCB1_UART_RTS	SCB2_UART_CTS	TCPWM_TR_ALL_3	
55	LHL_GPIO_6	SCB1-SPI_CLK		SCB2_UART_RTS	TCPWM_COMP_OUT_11	TCPWM_OUT_23
30	LHL_GPIO_8	SCB1-SPI_MOSI		SCB2_UART_RXD	TCPWM_COMP_OUT_21	TCPWM_OUT_25
53	LHL_GPIO_9	SCB1-SPI_MISO		SCB2_UART_TXD	TCPWM_COMP_OUT_22	TCPWM_OUT_26

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply voltage for VBAT.	-0.5	-	+6[7]	V
VDDIO	DC supply voltage for VDDIO	-0.5	-	+2.2	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply voltage for VBAT.	3.0[8]	3.3	4.8	V
VDDIO	DC supply voltage for VDDIO.	1.71	1.8	1.89	V

[7] The maximum continuous voltage is 5.25 V. Voltage transients up to 6.0 V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as HIGH as 5.5 V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.

[8] AW-CU668 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13V < VBAT < 3.5V.

3.3 Digital IO Pin DC Characteristics[9]

VDDIO:

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO=1.8V					
V_{IH}	Input high voltage (V_{DDIO})	0.65 × VDDIO	-	-	V
V_{IL}	Input low voltage (V_{DDIO})	-	-	0.35 × VDDIO	V
V_{OH}	Output High Voltage @ 2mA	VDDIO – 0.40	-	-	V
V_{OL}	Output Low Voltage @ 2mA	-	-	0.45	V

[9] Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

3.4 Interface

3.4.1 UART Interface

The AW-CU668 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.1 UART HCI specification: H4, and H5. The default baud rate is 115.2 Kbaud.

The CYW55913 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP).It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-CU668 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

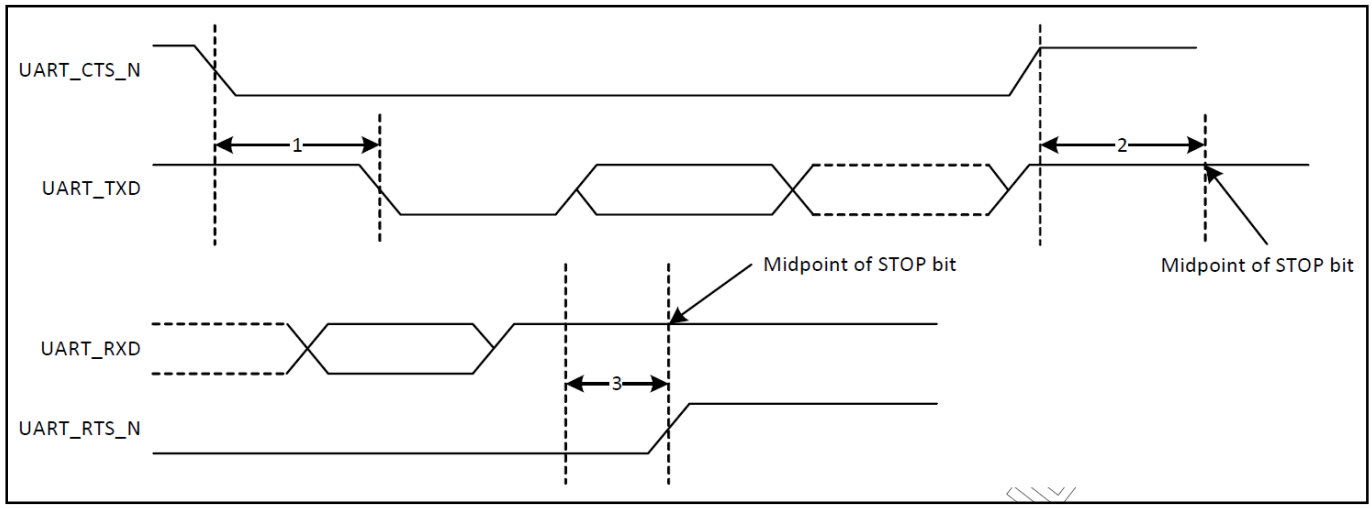
UART Interface Signals

PIN No.	Name	Description	Type
43	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	O
40	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	I
42	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	O
41	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	I

Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing



UART Timing Specifications

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

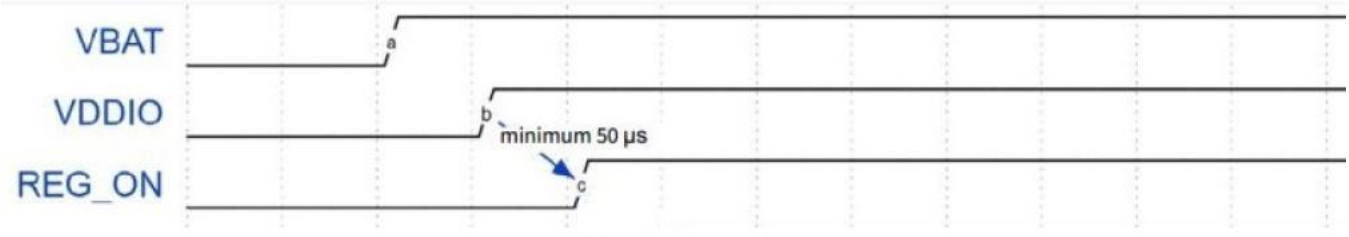
3.5 Power Up Timing Sequence

The AW-CU668 has one signals that enable or disable Bluetooth® and WLAN circuits and internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Power up timing sequence diagram.

Description of Control Signals (Power-Up/Power-Down/Reset Control Signals)

Signal	***Description***
REG_ON	This signal is used by the PMU to power up the device and to control the internal AW-CU640 regulators. When this pin is HIGH, the regulators are enabled, and the core is out of reset. If REG_ON is LOW, all the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and can be disabled up on recognizing high on this pin.

Power up timing sequence diagram



1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

3.6 Power Consumption[10]

3.6.1 WLAN

TBD

3.6.2 BT

TBD

[10] For Details, please contact Azurewave FAE

3.7 Frequency Reference

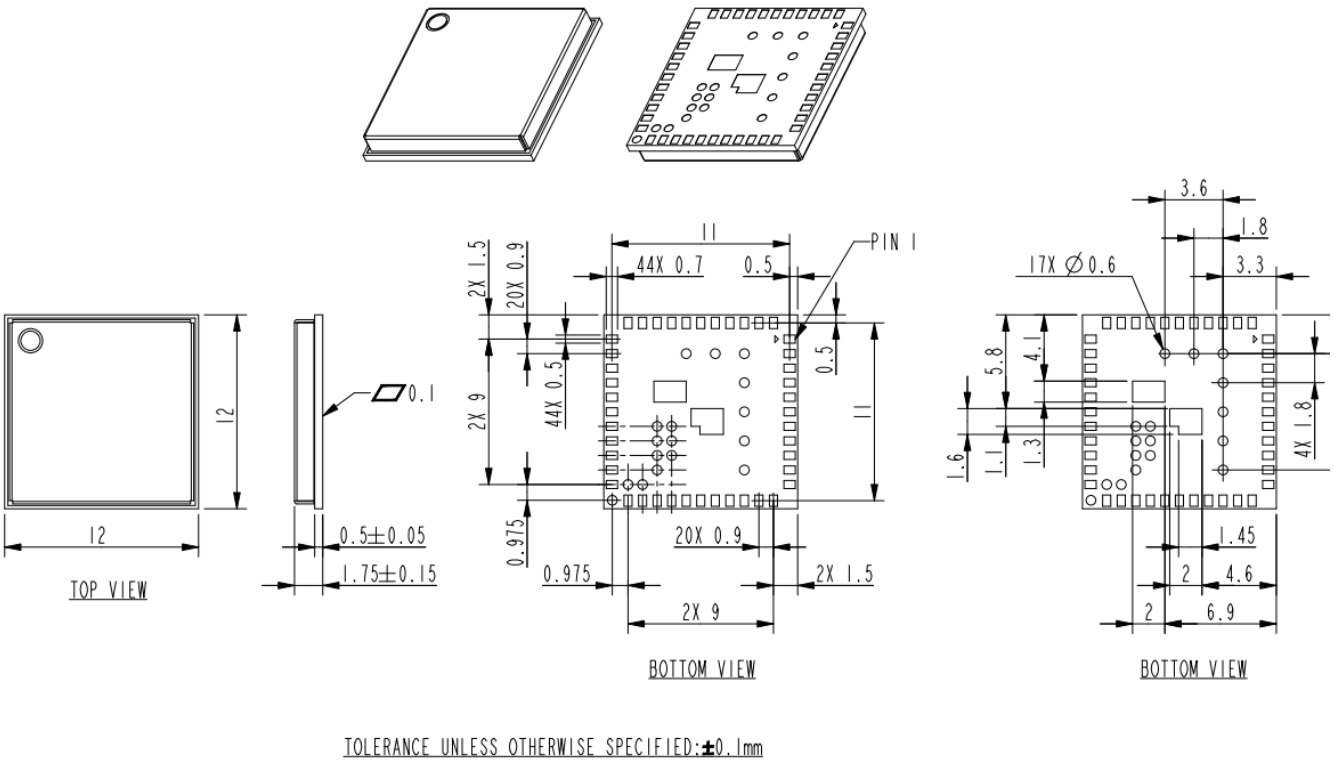
The AW-CU668 requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed in below table must be used.

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance [5]	> 100k	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10,000	ppm

Note
5. When power is applied or switched off.

4. Mechanical Information

4.1 Mechanical Drawing



5. Packaging Information

TBD