AW-CM572

IEEE 802.11 ac 2×2 MAC/Baseband/Radio and Bluetooth 5.1 Combo LGA Module

Datasheet

Rev.D

DF

(For Standard)

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Features

WLAN

- IEEE 802.11ac Wave-2 compliant.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE 802.11ac/n beamforming.
- Supports RSDB (option).
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE and GPS.
- Worldwide regulatory support: Global products supported with worldwide homologated design.
- Integrated Arm® Cortex® -R4 processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wakeup the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features.

Bluetooth

- Complies with Bluetooth Core Specification v5.0 with provisions for supporting future specifications.
- Supports all BT5.0 optional features including LE-2Mbps, LE-Long Range, LE-Advertising extensions.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high speed UART interface and PCM for audio data.

Bluetooth (continue)

- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.

AzureWave Technologies, Inc.

Revision History

Document NO: R2-2572-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2022/1/19	DCN025311	• Initial Version	Barry Tsai	N.C. Chen
B	2022/7/04	DCN026634	• Modify Pin Table • Modify Operating temperature • Modify Block Diagram	Jeff Kuo	N.C. Chen
C	2022/12/22	DCN028031	• Modify Pin Map • Modify Block Diagram • Update Ordering Information • Update Specification Table • Modify Operating temperature	QM.Tan	N.C. Chen
D	2024/01/19	DCN029311	• Modify Title • Modify 1.3.2 WLAN Security Description • Update ESD and Power Consumption WLAN (3.5.1) • Update Annotation	QM.Tan	N.C. Chen
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AzureWave Technologies, Inc.

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1. Introduction

1.1 Product Overview

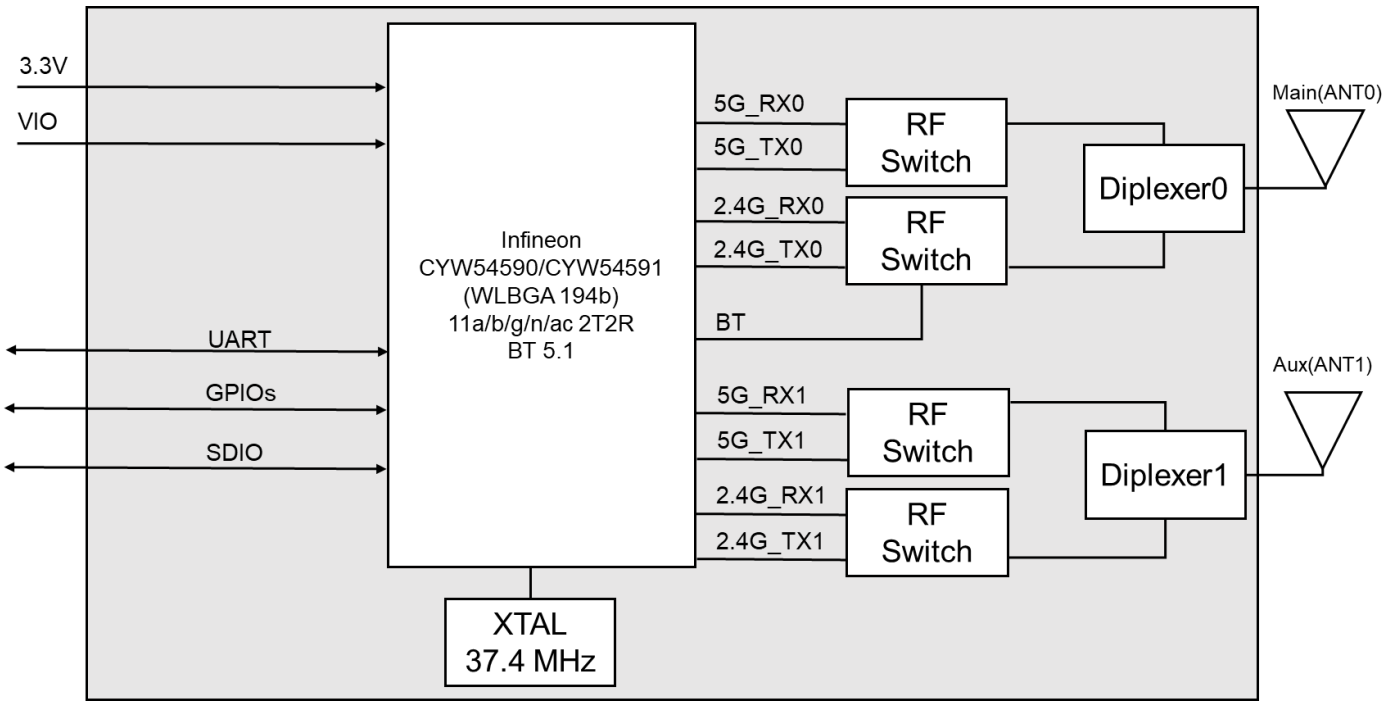
AzureWave Technologies, Inc. introduces the advanced IEEE 802.11 ac/a/b/g/n 2x2 MIMO WLAN and Bluetooth combo module - AW-CM572. The Module is a complete dual-band (2.4 GHz and 5 GHz) Wi-Fi 2×2 MIMO MAC/PHY/Radio system-on-module. This 5G Wi-Fi single-chip device provides a high level of integration with a dual-stream IEEE 802.11ac MAC/baseband/radio and Bluetooth 5.0. In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 867 Mbps. In addition, all the rates specified in IEEE 802.11a/b/g/n are supported. Included on-chip are the 2.4 GHz and 5 GHz transmit power amplifiers and receive low-noise amplifiers. The WLAN operation supports two fully simultaneous SISO channels and real simultaneous dual-band (RSDB) (option).
The WLAN section supports the following host interface options: an SDIO v3.0 interface that can operate in 4bits or 1bit mode.
For the Bluetooth section, Host interface is through a high-speed 4-wire UART interface and PCM interface for audio.
In addition, the AW-CM572 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms that ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. Coexistence support for external radios (such as LTE cellular and GPS) is provided via an external interface. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a Commercial/Consumer systems is achieved.

1.1.1 Ordering Information

Planned versions:

Model Name	IC
AW-CM572	CYW54590
AW-CM572-RSDB	CYW54591

1.2 Block Diagram



AW-CM572 BLOCK DIAGRAM

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac WLAN 2T2R with Bluetooth 5.1 Combo LGA Module
Major Chipset	Infineon CYW54591/CYW54590(wlbga 194b)
Host Interface	Wi-Fi +BT ● SDIO + UART
Dimension	15mm(L) x 13mm(W) x 1.95mm(H) (Tolerance remarked in mechanical drawing)
Form factor	LGA module, 50 pins
Antenna	External Antennas Design ANT0(Main)：WiFi/Bluetooth → TX/RX ANT1(AUX)：WiFi → TX/RX
Weight	TBD

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 a/b/g/n/ac 2T2R
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	2.4 GHz：2.412 ~ 2.484 GHz 5 GHz：4.915 ~5.925GHz
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM, 256-QAM,
Number of Channels	**2.4GHz** ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13 **5GHz** ■ USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

Output Power[1][2] (Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<8%	15.5	17.5	19.5	dBm
11g (54Mbps) @EVM≦-25 dB	14.5	16.5	18.5	dBm
11n (HT20 MCS7) @EVM≦-27 dB	13.5	15.5	17.5	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM<-25 dB	13.5	15.5	17.5	dBm
11n (HT20 MCS7) @EVM≦-27 dB	12.5	14.5	16.5	dBm
11n (HT40 MCS7) @EVM≦-27 dB	12.5	14.5	16.5	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	10.0	12.0	14.0	dBm
11ac (VHT40 MCS9) @EVM≦-32 dB	8.0	10.0	12.0	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	8.0	10.0	12.0	dBm

Receiver Sensitivity

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-89	-86	dBm
11g (54Mbps)		-77	-74	dBm
11n (HT20 MCS7)		-75	-72	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		-75	-72	dBm
11n (HT20 MCS7)		-73	-70	dBm
11n (HT40 MCS7)		-70	-67	dBm
11ac[3] (VHT20 MCS8)		-68	-64	dBm
11ac[4] (VHT40 MCS9)		-64	-61	dBm
11ac[5] (VHT80 MCS9)		-61	-58	dBm

[1] Power setting at typical value, EVM specification will pass with IEEE specification.
[2] Unless otherwise stated, limit values apply for an ambient temperature of +25 °C.
[3] Tested by BCC instead of LDPC.
[4] Tested by BCC instead of LDPC.
[5] Tested by BCC instead of LDPC.

Data Rate	WLAN: 802.11b: 1, 2, 5.5, 11Mbps 802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: up to 150Mbps-single 802.11n: up to 300Mbps-2x2 MIMO 802.11ac:up to 173.3Mbps (20MHz channel) 802.11ac:up to 400Mbps (40MHz channel) 802.11ac:up to 866.7Mbps (80MHz channel)
Security	WPA, WAPI STA, WPA2, WPA3 (Personal/Enterprise) support for powerful encryption and authentication. AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility. Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS).

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>BT5.1+Enhanced Data Rate (EDR)</td></tr>
<tr><td>Bluetooth VID/PID</td><td>N/A</td></tr>
<tr><td>Frequency Rage</td><td>2402~2483MHz</td></tr>
<tr><td>Modulation</td><td>GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps)</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>BDR</td><td>4</td><td>7</td><td>10</td><td>dBm</td></tr>
<tr><td>EDR</td><td>2</td><td>5</td><td>8</td><td>dBm</td></tr>
<tr><td>Low Energy (1MHz)</td><td>4</td><td>7</td><td>10</td><td>dBm</td></tr>
<tr><td>Low Energy (2MHz)</td><td>4</td><td>7</td><td>10</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Receiver Sensitivity[6]</td><td>
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>BDR (BER<0.1%)</td><td></td><td>-86</td><td></td><td>dBm</td></tr>
<tr><td>EDR (π/4 DQPSK) (BER<0.07%)</td><td></td><td>-88</td><td></td><td>dBm</td></tr>
<tr><td>EDR (8PSK) (BER<0.07%)</td><td></td><td>-84</td><td></td><td>dBm</td></tr>
<tr><td>BLE(1M) (PER<-30.8%)</td><td></td><td>-89</td><td></td><td>dBm</td></tr>
<tr><td>BLE(2M) (PER<-30.8%)</td><td></td><td>-86</td><td></td><td>dBm</td></tr>
</table>
</td></tr>
</table>

[6] Tested by sLNA.

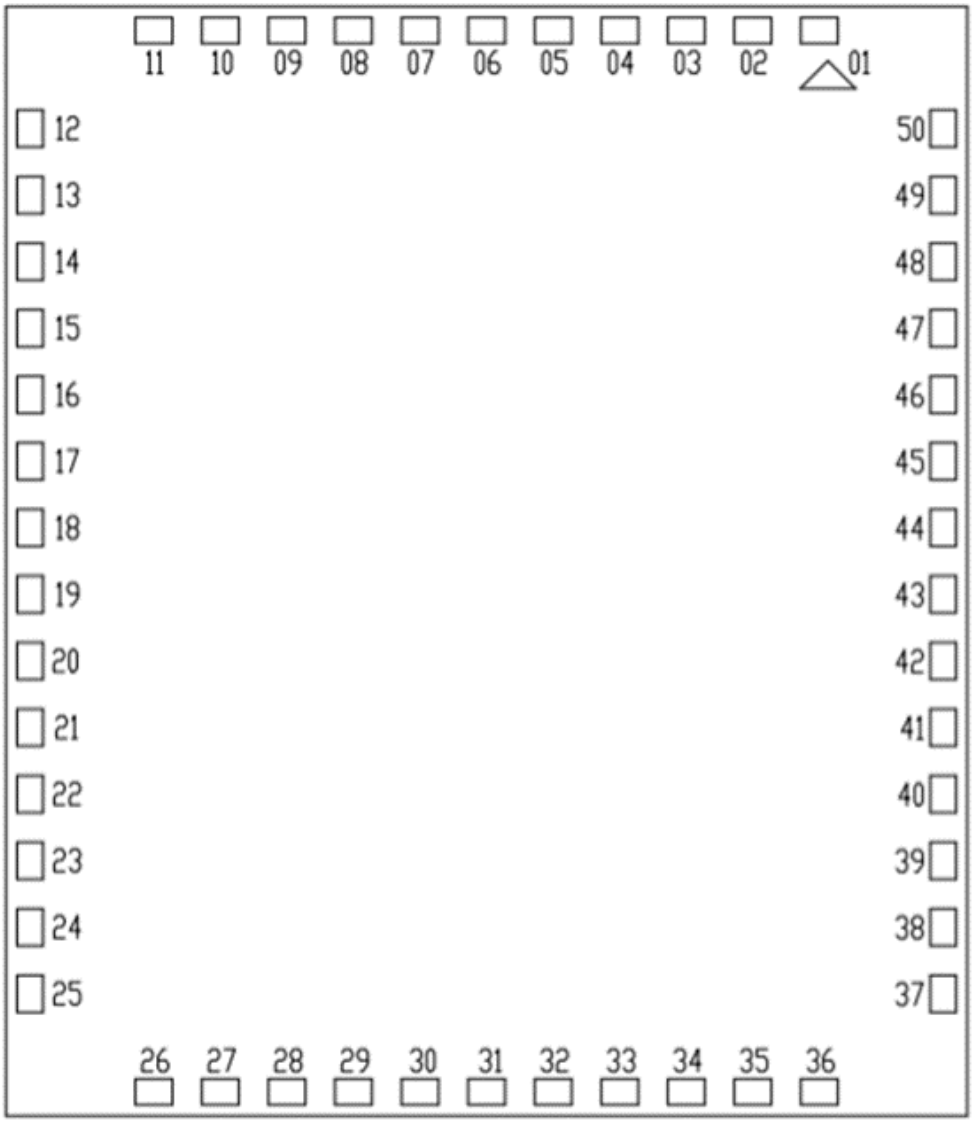
1.3.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	Power supply for host:3.3V
Operating Temperature	-40℃~85℃[7]
Operating Humidity	less than 85%R.H.
Storage Temperature	-40℃~ 85℃
Storage Humidity	less than 60%R.H.
ESD Protection	
Human Body Model	+/-2KV
Changed Device Model	+/-300V

[7] -40℃~85℃ is Functional operation, for detail please check with AzureWave FAE.

2. Pin Definition

2.1 Pin Map



AW-CM572 Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	System Ground Pin	-	-
2	WL_ANT0	RF(BT&WIFI) I/O port0	-	I/O
3	GND	System Ground Pin	-	-
4	GND	System Ground Pin	-	-
5	GND	System Ground Pin	-	-
6	GND	System Ground Pin	-	-
7	GND	System Ground Pin	-	-
8	GND	System Ground Pin	-	-
9	WL_ANT1	RF(WIFI) I/O port1	-	I/O
10	GND	System Ground Pin	-	-
11	GND	System Ground Pin	-	-
12	NC	Floating (Don’t connected to ground)	-	-
13	NC	Floating (Don’t connected to ground)	-	-
14	NC	Floating (Don’t connected to ground)	-	-
15	WL_REG_ON	Low asserting reset for WiFi core	VDDIO	I
16	WL_HOST_WAKE	WLAN to wake-up HOST	VDDIO	O
17	SDIO_DATA_CMD	SDIO command line	VDDIO	I/O
18	SDIO_DATA_CLK	SDIO clock line	VDDIO	I/O
19	SDIO_DATA_3	SDIO data line 3	VDDIO	I/O
20	SDIO_DATA_2	SDIO data line 2	VDDIO	I/O
21	SDIO_DATA_0	SDIO data line 0	VDDIO	I/O
22	SDIO_DATA_1	SDIO data line 1	VDDIO	I/O
23	GND	System Ground Pin	-	-

24	SDIO_VSEL	SDIO voltage select: 0: 3.3V 1:1.8V	VDDIO	I
25	VIN_LDO	Internal Buck voltage generation pin	1V35	P
26	VIN_LDO_OUT	Internal Buck voltage generation pin	1V35	P
27	PCM_SYNC	PCM sync signal	VDDIO	I/O
28	PCM_IN	PCM data input	VDDIO	I
29	PCM_OUT	PCM Data output	VDDIO	O
30	PCM_CLK	PCM clock	VDDIO	I/O
31	LPO	External Low Power Clock input (32.768KHz)	-	I
32	GND	System Ground Pin	-	-
33	NC	Floating (Don’t connected to ground)	-	-
34	VDDIO	I/O Voltage supply input	VDDIO	P
35	NC	Floating (Don’t connected to ground)	-	-
36	VBAT	Main power voltage source input	3V3	P
37	NC	Floating (Don’t connected to ground)	-	-
38	BT_REG_ON	Low asserting reset for Bluetooth core	VDDIO	I
39	GND	System Ground Pin	-	-
40	UART_TXD	UART serial output. Serial data output for the HCI UART interface.	VDDIO	O
41	UART_RXD	UART serial input. Serial data input for the HCI UART interface.	VDDIO	I
42	UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	VDDIO	O
43	UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	VDDIO	I
44	WL_UART_TX	WL_UART_TX	VDDIO	O

45	WL_UART_RX	WL_UART_RX	VDDIO	I
46	NC	Floating (Don’t connected to ground)	-	-
47	GND	System Ground Pin	-	-
48	NC	Floating (Don’t connected to ground)	-	-
49	BT_WAKE	HOST wake-up Bluetooth device	VDDIO	I
50	BT_HOST_WAKE	Bluetooth device to wake-up HOST	VDDIO	O

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO	DC supply voltage for VDDIO.	-0.5	-	3.9	V
VBAT	DC supply voltage for VBAT.	-0.5	-	6.0	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply voltage for VBAT	3.2[8]	-	4.8[9]	V
VDDIO	DC supply voltage for Digital I/O	3.2	-	4.8	V
		1.67	1.80	1.98	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital I/O pins, VDDIO=1.8V					
V_{IH}	Input high voltage	0.65 × VDDIO	-	-	V
V_{IL}	Input low voltage	-	-	0.35 × VDDIO	V
V_{OH}	Output high voltage	VDDIO – 0.45	-	-	V
V_{OL}	Output Low Voltage	-	-	0.45	V
Digital I/O pins, VDDIO=3.3V					
V_{IH}	Input high voltage	2.00	-	-	V
V_{IL}	Input low voltage	-	-	0.80	V
V_{OH}	Output high voltage	VDDIO – 0.4	-	-	V
V_{OL}	Output low Voltage	-	-	0.40	V

8 The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.

9 AW-CM572 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 4.5V.

3.4 Power up Timing Sequence

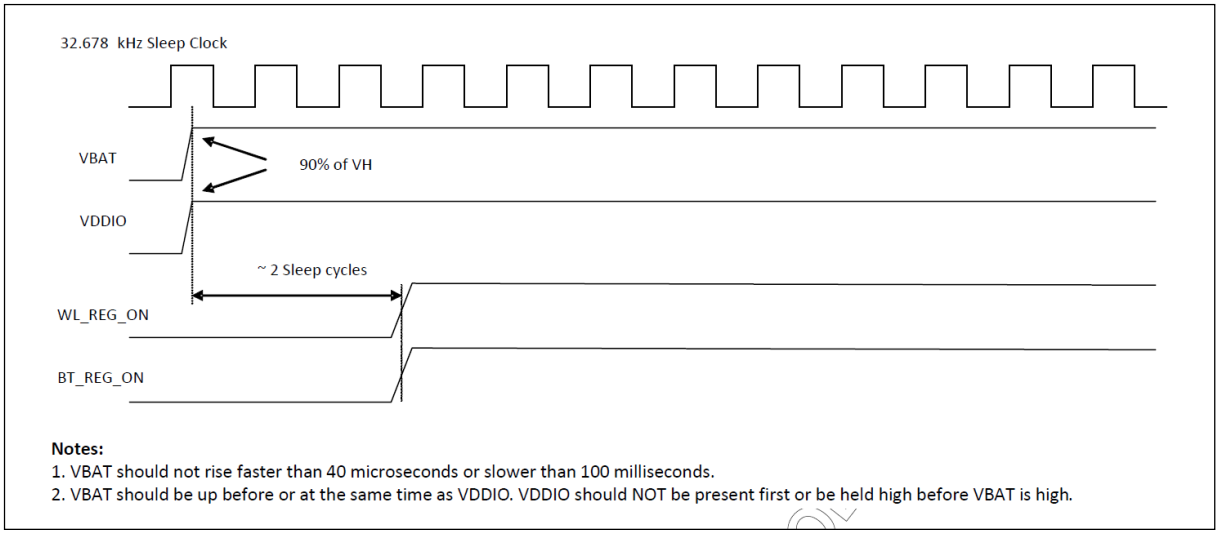
The AW-CM572 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals (Power-Up/Power-Down/Reset Control Signals)

Signal	***Description***
W_DISABLE1 (WL_REG_ON)	Used by the PMU to power up the WLAN section. It is also OR-gated with the W_DISABLE2 (BT_REG_ON) input to control the internal AW-CM572 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the W_DISABLE2 (BT_REG_ON) and W_DISABLE1 (WL_REG_ON) pins are low, the regulators are disabled.
W_DISABLE2 (BT_REG_ON)	Used by the PMU (OR-gated with W_DISABLE1) to power up the internal AW-CM572 regulators. If both the W_DISABLE2 (BT_REG_ON) and W_DISABLE1 (WL_REG_ON) pins are low, the regulators are disabled. When this pin is low and W_DISABLE1 (WL_REG_ON), the BT section is in reset.

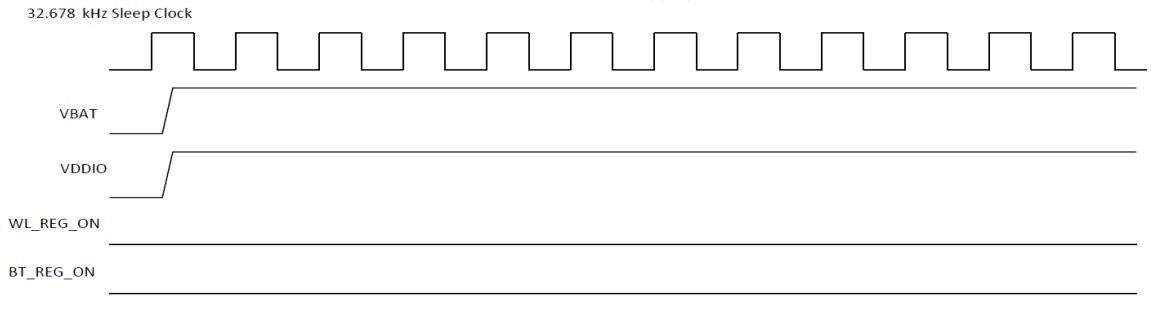
Control Signal Timing Diagrams

WLAN = ON, Bluetooth = ON



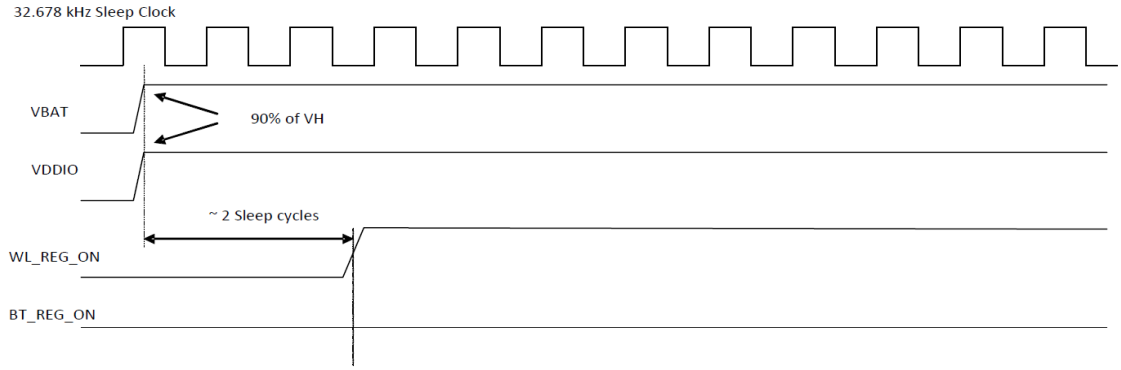
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF



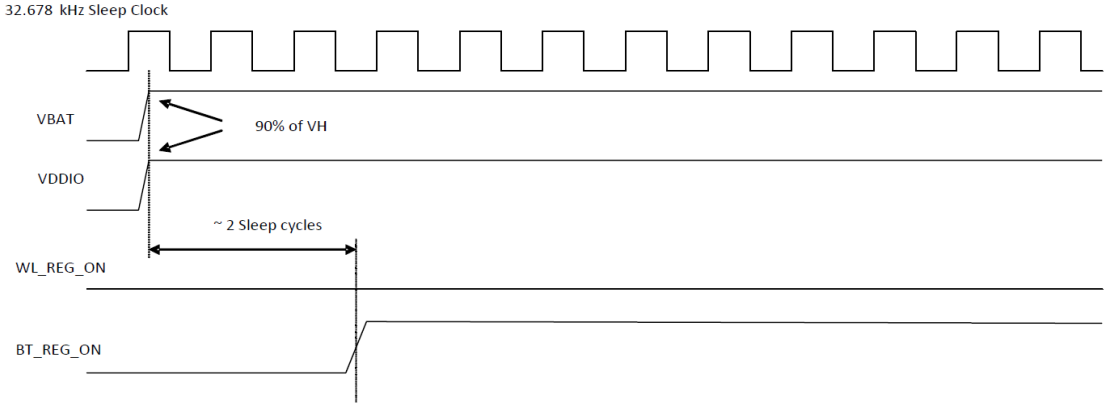
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

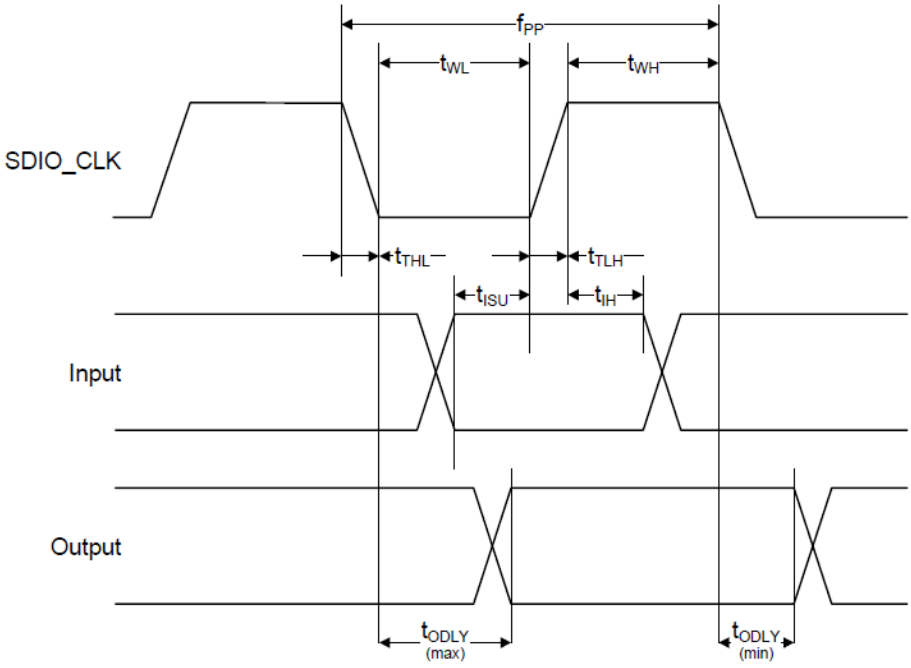
WLAN = OFF, Bluetooth = ON



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

3.4.1 SDIO Interface

SDIO Bus Timing (Default Mode)

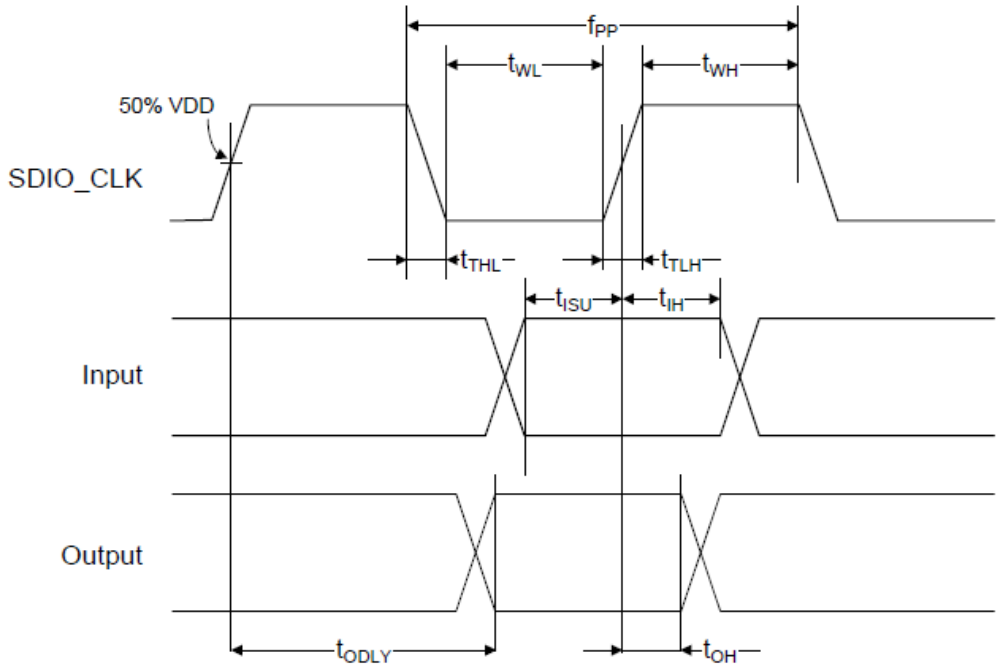


SDIO Bus Timing Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL)					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns

Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

SDIO Bus Timing (High-Speed Mode)



SDIO Bus Timing Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns

Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

3.4.2 UART Interface

The AW-CM572 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“3-wire UART Transport Layer”).Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The CYW54591/CYW54590 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP).It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-CM572 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.UART Interface Signals

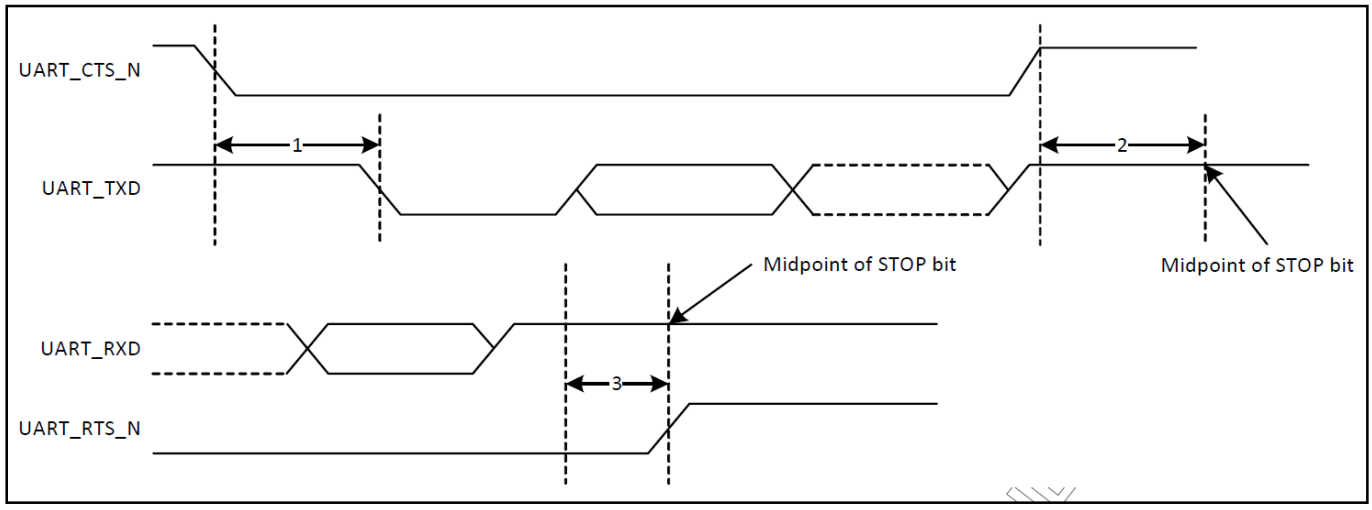
UART Interface Signals

PIN No.	Name	Description	Type
40	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	**O**
41	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	**I**
42	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	**O**
43	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	**I**

Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing



UART Timing Specifications

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

3.4.3 I2S Interface

The AW-CM572 supports I2S digital audio port for Bluetooth audio which shared the pin out with PCM interface.
The I2S signals are:
■ I2S clock: I2S_SCK
■ I2S Word Select: I2S_WS
■ I2S Data Out: I2S_SD_OUT
■ I2S Data In: I2S_SD_IN
I2S_SCK and I2S_WS become outputs in Master mode and inputs in Slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSb of the left-channel data is aligned with the MSb of the I2S bus, in accord with the I2S specification. The MSb of each data word is transmitted one bit clock cycle after the I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when I2S_WS is LOW, and right channel data is transmitted when I2S_WS is HIGH. Data bits sent by the AW-CB511NF-BPF are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SCK.
The clock rate in master mode is either of the following:
48 kHz × 32 bits per frame = 1.536 MHz
48 kHz × 50 bits per frame = 2.400 MHz
The master clock is generated from the input reference clock using a N/M clock divider.
In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

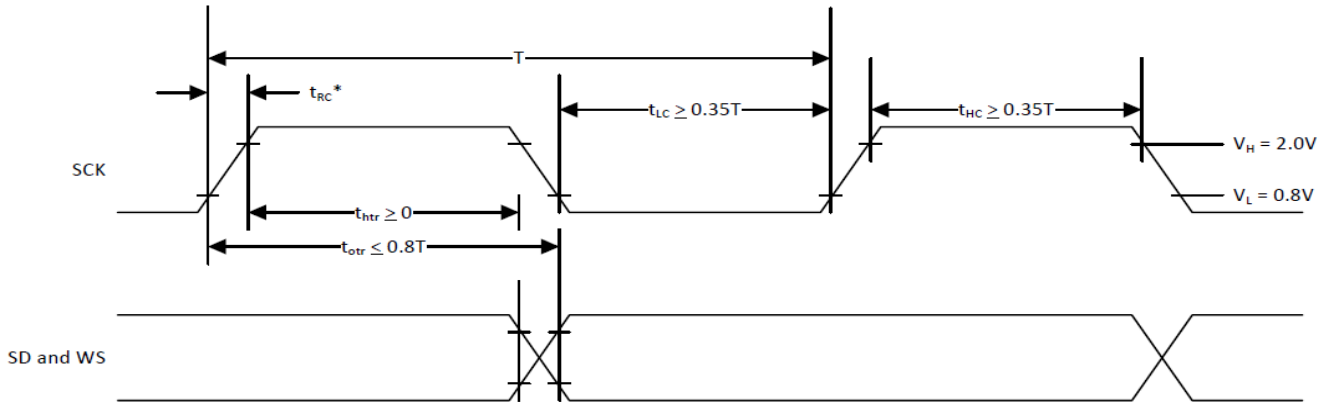
I2S Timing

	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	7
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	8
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	8
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	9
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	9
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	10
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	11
Hold time t_{htr}	0	–	–	–	–	–	–	–	10
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	12
Hold time t_{hr}	–	–	–	–	–	0	–	–	12

Notes

7. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
8. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
9. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
10. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
11. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
12. The data setup and hold time must not be less than the specified receiver setup and hold time.

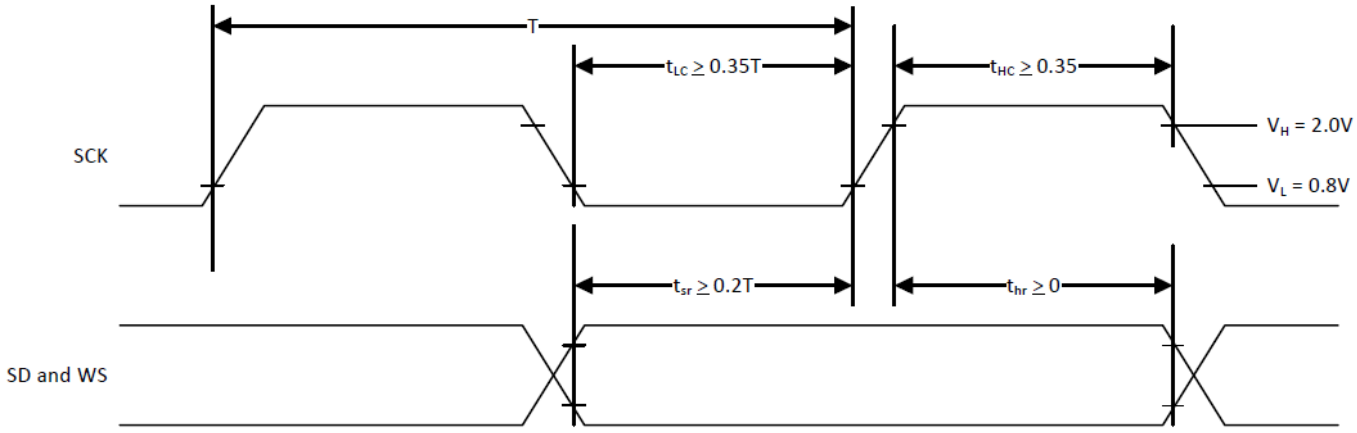
I2S Transmitter Timing[10]



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

[10] The time periods specified in I2C transmitter timing and I2C receiver timing are defined by the transmitter speed. The receiver specifications must match transmitter performance.

I2S Receiver Timing[11]



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

[11] The time periods specified in I2C transmitter timing and I2C receiver timing are defined by the transmitter speed. The receiver specifications must match transmitter performance.

3.5 Power Consumption[12]

3.5.1 WLAN

No.	Item			VBAT=3.3V(mA)		
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit		
				Max.	Avg.	Duty Mean (%)
2.4	11b@1Mbps	20	17.5	345	336	99
	11g@54Mbps	20	16.5	249	248	64
	11n@MCS8	20	15.5	547	545	87
	11n@MCS15	20	15.5	365	363	52
5	11a@6Mbps	20	15.5	406	404	93
	11n@MCS8	40	14.5	652	649	87
	11n@MCS15	40	14.5	437	435	52
	11ac@MSC8 NSS1	20	12.0	275	274	60
	11ac@MSC8 NSS2	20	12.0	399	396	50
	11ac@MSC0 NSS2	40	10.0	576	575	87
	11ac@MSC9 NSS1	40	10.0	271	270	47
	11ac@MSC9 NSS2	40	10.0	383	382	41
	11ac@MSC0 NSS2	80	10.0	600	597	66
	11ac@MSC9 NSS1	80	10.0	318	317	39
	11ac@MSC9 NSS2	80	10.0	448	446	37
Band (GHz)	Mode	BW(MHz)		Receive		
				Max.	Avg.	
2.4	11b@11Mbps	20		83	81	
	11n@MCS7	20		85	84	
5	11a@54Mbps	20		109	107	
	11ac@MCS9 NSS1	80		183	181	

***TX commend: ./wl_fmac_x86_x64 pkteng_start 00:11:22:33:44:55 tx 100 1024 0**

No.	Item			VDDIO=1.8V(uA)	
Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit	
				Max.	Avg.
2.4	11b@1Mbps	20	17.5	38	37
5	11ac@MSC9 NSS2	80	10.0	38	38
Band (GHz)	Mode	BW(MHz)		Receive	
				Max.	Avg.
2.4	11b@11Mbps	20		36	36
5	11ac@MCS9 NSS1	80		37	37

* The power consumption is based on AzureWave test environment, these data for reference only.

[12] For Details, please contact Azurewave FAE

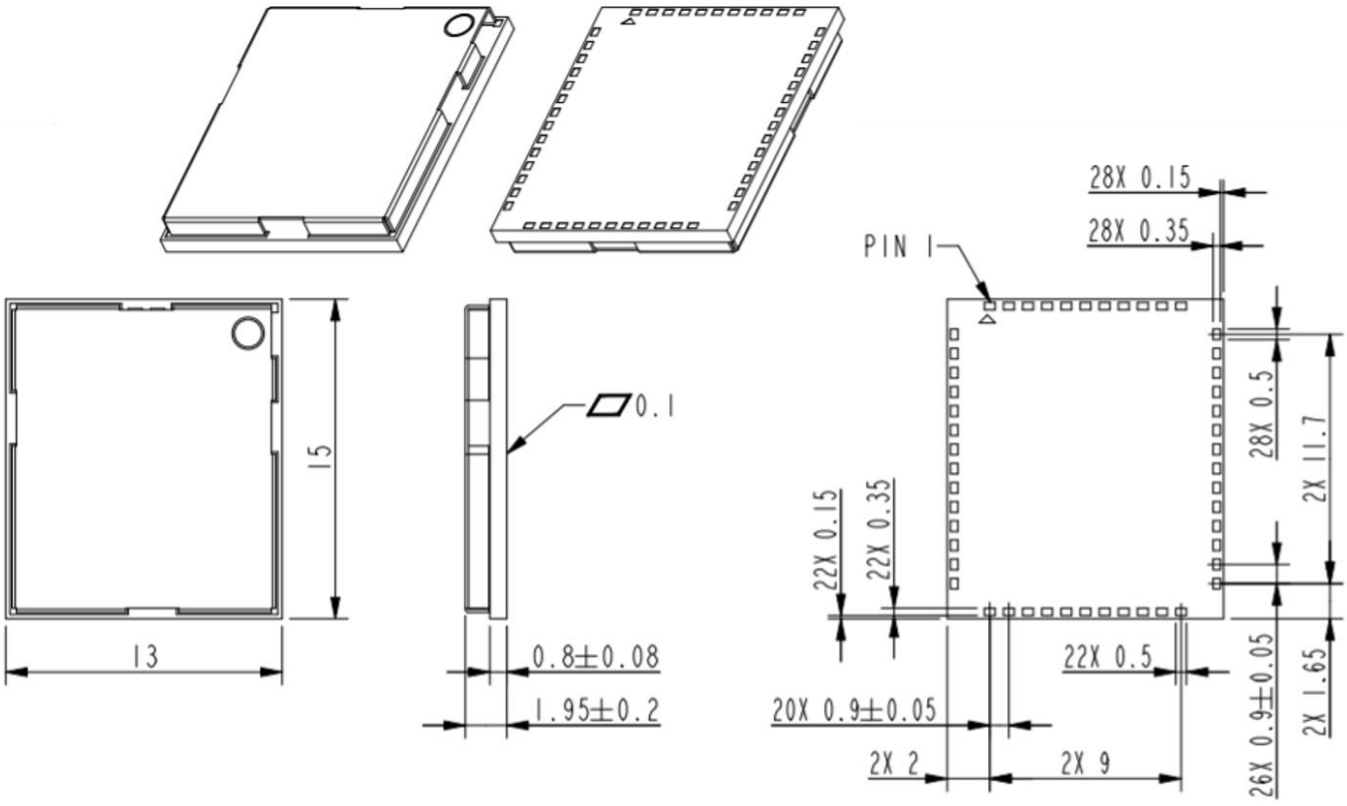
3.5.2 Bluetooth

No.	Mode	Voltage=3.3 V	
		Max.	Avg.
1	Bluetooth RF Off	TBD	TBD
2	No Connection with any BT device	TBD	TBD
3	Connect BT Device	TBD	TBD
4	Transmit by BER 2.1	TBD	TBD
5	Receiver by BER 2.1	TBD	TBD

* The power consumption is based on AzureWave test environment, these data for reference only.

4. Mechanical Information

4.1 Mechanical Drawing



5. Packaging Information

5.1 Label level package

TBD