AW-CM217NF

IEEE 802.11 a/b/g/n/ac Wireless LAN and Bluetooth M.2 Combo Module

Datasheet

Rev. B

0B

(For Standard)

Features

- Integrates Infineon solutions of CYW4356 Wi-Fi /BT Single Chip
- Concurrent Bluetooth and WLAN operation
- ECI—enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- Multiple power saving modes for low power consumption
- Lead-free /Halogen Free Design
- 12 mm(L) x 16mm(W) x 1.5mm(H) 132 pin LGA package

Bluetooth

- Bluetooth Class 1 or Class 2 transmitter operation
- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 5.0 + (Enhanced Data Rate) EDR features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO) — Voice Connections
  - Fast Connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I2S and PCM interface)
- Multiple simultaneous A2DP audio stream

WLAN

- IEEE 802.11ac Draft compliant
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance
- IEEE 802.11a/b/g/n/ac dual-band radio with virtual-simultaneous dual-band operation
- IEEE 802.11ac 2x2 MIMO supports for 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation) provides data rates up to 866.7 Mbps.
- Tx and Rx low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE, GPS, or WiMAX
- Supports IEEE 802.11d, e, h, i, r, k, w
- WLAN host interface options
  - PCIe mode complies with PCI Express base specification revision 3.0 for ×1 lane and power management running at Gen1 speeds
- Security–WEP, WPA/WPA2 (personal), AES

(HW), TKIP (HW), CKIP (SW).

- WMM/WMM-PS/WMM-SA
- Proprietary protocol – CCXv2/CCXv3/CCXv4/CCXv5
- Integrated CPU with on-chip memory for a complete WLAN subsystem minimizing the need to wake up the applications processor

Revision History

Document NO: R2-2217NF-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
0.1	2014/11/26		● Initial release	Stanley Wang	Chihhao Liao
0.2	2014/12/31		● Update Pin definition and Pin Map	Stanley Wang	Chihhao Liao
0.3	2015/2/10		● Update Pin definition and Pin Map	Stanley Wang	Chihhao Liao
0.4	2015/2/16		● Update Specification	Stanley Wang	Chihhao Liao
0.5	2015/3/31		● Update Pin definition, block diagram, and power management	Stanley Wang	Chihhao Liao
0.6	2015/4/15		● Update Electrical Characteristics	Stanley Wang	Chihhao Liao
0.7	2015/6/10		● Modified 1-2 Key features, 1-3 Block Diagram, 1-4 Specifications Table, 2-1 Absolute Maximum Ratings, 3 Pin Definition	Steven Jian	Chihhao Liao
0.8	2015/8/19		● Modified 2-5-1-1 Bluetooth USB Interface	Steven Jian	Chihhao Liao
0.9	2018/07/25		● Updated format ● Modified 2.2 Pin Table ● Modified 3.5 Power Consumption	Steven Jian	Chihhao Liao
1.0	2018/09/20		● Updated title	Steven Jian	Chihhao Liao
1.1	2018/11/15		● Support BT 5.0	Steven Jian	Chihhao Liao
1.2	2019/07/18		● Updated 1.3 Block Diagram ● Updated 1.4.2 ● Updated 2.1	Steven Jian	Chihhao Liao
A	2020/03/14	DCN016870	● Change Document Format ● Updated 1.3.1 General ● Corrected 5G Output Power in 1.3.2 WLAN ● Updated 1.3.3 Bluetooth ● Updated Pin 45 Description ● Updated 3.2 Recommended Operating Conditions ● Updated 3.4 Host Interface	Steven Jian	Chihhao Liao
B	2021/04/15	DCN021169	● Change Document Format ● Updated the chip vendor name	Steven Jian	Chihhao Liao

Table of Contents

1. Introduction

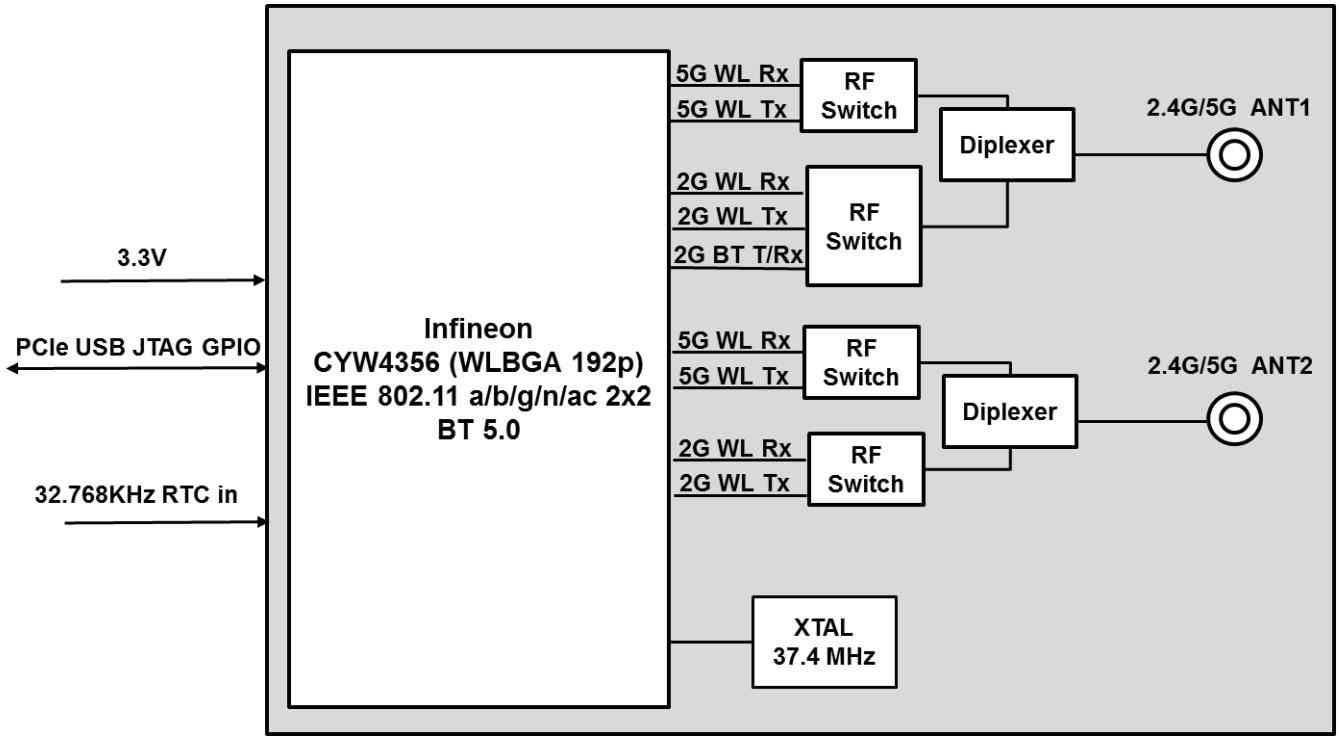
1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced IEEE 802.11 ac/a/b/g/n 2x2 MIMO WLAN and Bluetooth M.2 combo module - AW-CM217NF. The module is targeted to mobile and embedded devices which need small footprint package, low power consumption, and multiple OS support. The module supports 2.4GHz and 5GHz bands IEEE 802.11ac MAC/baseband/radio and Bluetooth 5.0(Core Standard) + EDR. It also features an integrated Power Management Unit (PMU), Power Amplifiers (PAs), and a Low Noise Amplifier (LNA) to address the needs of mobile devices that require minimal power consumption and compact size. By using AW-CM217NF, the customers can easily enable the Wi-Fi and BT embedded applications with the benefits of high design flexibility, short development cycle, and quick time-to-market.

For the WLAN operation, the AW-CM217NF uses DSSS, OFDM, DBPSK, DQPSK, CCK and QAM baseband modulation technologies. In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 867 Mbps. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM217NF. In addition to the support of WPA/WPA2 (personal) and WEP encryption, the AW-CM217NF also supports the IEEE 802.11i security standard through AES and TKIP acceleration hardware for faster data encryption. For the video, voice and multimedia applications the AW-CM217NF support 802.11e Quality of Service (QoS).

For Bluetooth operation, the AW-CM217NF is Bluetooth 5.0. The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability. The AW-CM217NF supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets, and Adaptive Frequency Hopping (AFH) for reducing radio frequency interference. It incorporates all Bluetooth 5.0 features.

1.2 Block Diagram



AW-CM217NF Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac Wireless LAN and Bluetooth M.2 Combo Module
Major Chipset	Infineon CYW4356 (WLBGA 192p)
Host Interface	WLAN: PCIe 3.0 (Gen1 speed) Bluetooth: USB
Dimension	16mm(L) 12xmm(W) x 1.5mm(H)
Form factor	M.2 1216
Antenna	HSC Receptacle(refer to 4.1 Mechanical Drawing) Ant 1: Wi-Fi/BT Main Ant 2: WIFI AUX
Weight	0.6g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant
WLAN VID/PID	14E4/43EC
WLAN SVID/SPID	1A3B/2217
Frequency Rage	WLAN: 2.4 GHz / 5GHz Band
Modulation	DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9)
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 Japan – 1 ~ 13 802.11g:

<table>
<tr><td></td><td>USA and Canada – 1 ~ 11
Most European Countries – 1 ~ 13
802.11n:
USA and Canada – 1 ~ 11
Most European Countries – 1 ~ 13
802.11a:
USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165</td></tr>
<tr><td>Output Power
(Board Level Limit)*</td><td>2.4G
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<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)
@EVM<35%</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)
@EVM≦ -25 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦ -27 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)
@EVM≦ -27 dB</td><td>9</td><td>11</td><td>13</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)
@EVM≦ -25 dB</td><td>11</td><td>13</td><td>15</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)
@EVM≦ -27 dB</td><td>10</td><td>12</td><td>14</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)
@EVM≦ -27 dB</td><td>8</td><td>10</td><td>12</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9)
@EVM≦ -32 dB</td><td>6</td><td>8</td><td>10</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td></td><td>-88</td><td>-82</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td></td><td>-74</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>-71</td><td>-65</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td></td><td>-68</td><td>-62</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td></td><td>-73</td><td>-67</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td></td><td>-70</td><td>-64</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td></td><td>-67</td><td>-61</td><td>dBm</td></tr>
<tr><td>11ac (VHT80 MCS9)</td><td></td><td>-59</td><td>-53</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Data Rate</td><td>802.11b: 1, 2, 5.5, 11Mbps
802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11n: MCS0~7 HT20/HT40</td></tr>
</table>

	802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac: MCS0~8 VHT20 802.11ac: MCS0~9 VHT40/VHT80
Security	◆ WPA™- and WPA2™- (Personal) support for powerful encryption and authentication ◆ AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility ◆ Secure Easy Setup™ for simple Wi-Fi® setup and WPA2/WPA security configuration ◆ Wi-Fi Protected Setup (WPS) ◆ WEP ◆ WMM / WMM-SA ◆ CKIP(Software)

1.3.3 Bluetooth

Features	**Description**
Bluetooth Standard	Bluetooth 2.1+Enhanced Data Rate (EDR) / BT5.0 (Core Standard)
Bluetooth VID/PID	13D3/3485
Frequency Rage	2400~2483.5MHz
Modulation	GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)
Output Power	Class 2
Receiver Sensitivity	

	Min	Typ	Max	Unit
DH5		-92	-82	dBm
2DH5		-94	-84	dBm
3DH5		-88	-78	dBm

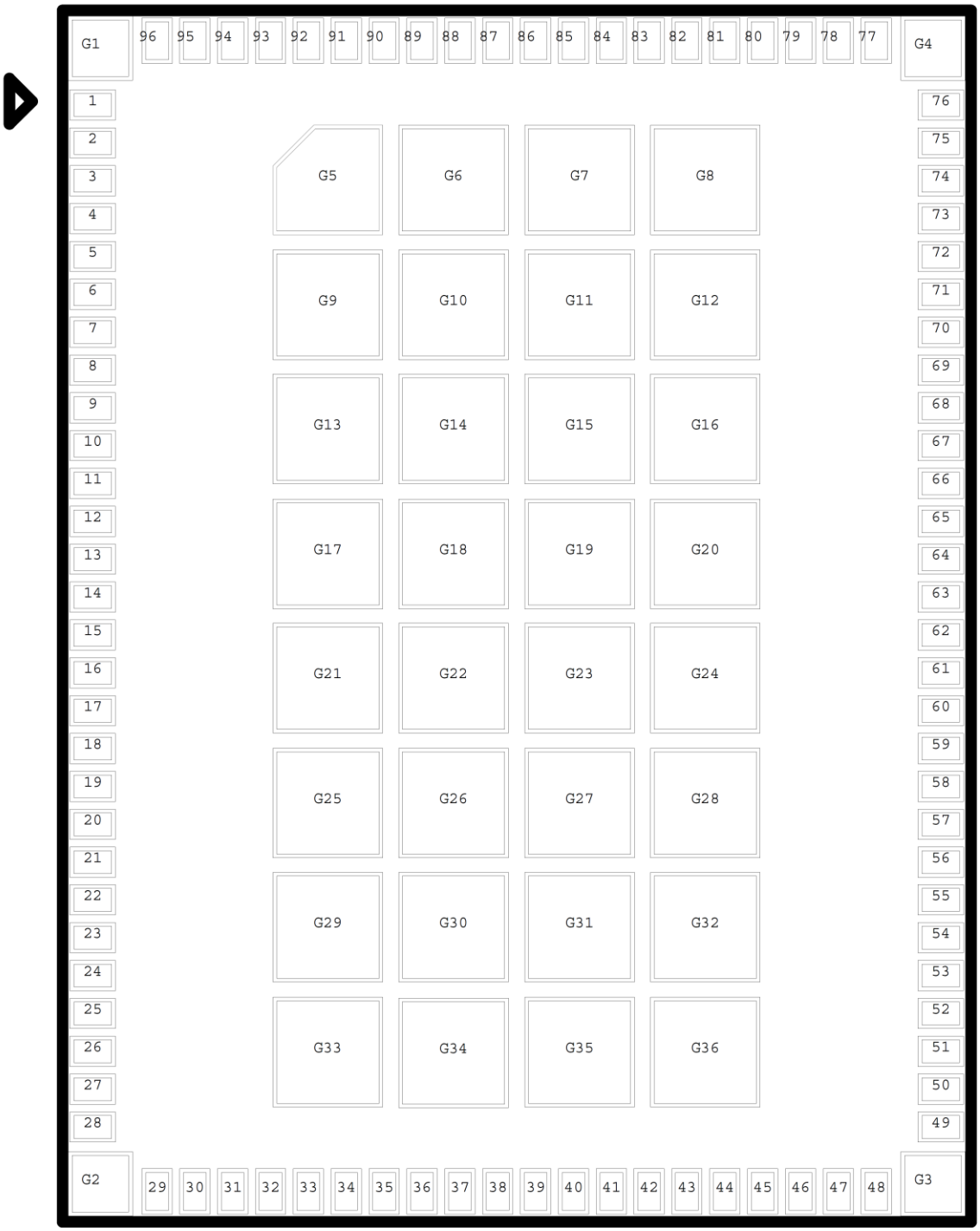
1.3.4 Operating Conditions

Features	**Description**
Operating Conditions	
Voltage	3.3V:3.3V+-5%
Operating Temperature	-30°C to 85°C (Functionality is guaranteed. Optimal RF operating is 0°C to 55°C)
Operating Humidity	less than 85% R.H.

Storage Temperature	-40°C to 85°C
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	±1KV per MIL-STD-883H Method 3015.8
Charged Device Model	±300V per JEDEC EIA/JESD22-C101E

2. Pin Definition

2.1 Pin Map



AW-CM217NF Pin Map (Top View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	NC	No Connect		
2	JTAG_SEL	JTAG test on/off(pull high to enable JTAG)	VIO	I
3	NC	No Connect		
4	3.3V	3.3V Power Supply	3.3V	I
5	3.3V	3.3V Power supply input	3.3V	I
6	GND	System Ground Pin		
7	JTAG_TDO_GPIO_5	GPIO_5 (input/output)	VIO	O
8	GPIO_8	Strapping option(please pull up with 10k resistor)	VIO	I
9	GPIO_9	Strapping option(please pull up with 10k resistor)	VIO	I
10	JTAG_TDI_GPIO_4	0: SPROM is absent (default). *Please reserve pull-down resistor	VIO	I
11	JTAG_TMS_COEX2_GPIO_3	GPIO_3 (input/output)	VIO	I/O
12	JTAG_TCK_COEX1_GPIO_2	GPIO_2 (input/output)	VIO	I/O
13	JTAG_TRST_N_COEX0_GPIO_6	GPIO_6 (input/output)	VIO	I/O
14	NC	No Connect		
15	NC	No Connect		
16	NC	No Connect		
17	GND	System Ground Pin		
18	NC	No Connect		
19	NC	No Connect		
20	GND	System Ground Pin		
21	NC	No Connect		
22	NC	No Connect		
23	GND	System Ground Pin		

24	BT_DEV_WAKE	No Connect		
25	NC	No Connect		
26	GND	System Ground Pin		
27	SLPCLK	External sleep clock input (32.768 kHz LPO).	0.2~3.3 Vp-p	I
28	WL_RFDISABLE_L_GPIO1	WL_DEV_WAKE/GPIO1	VIO	I
29	PCIE_WAKEn	PCIe wake signal (output)	VIO	O
30	PCIE_CLKREQn	PCIe clock request (input/output)	VIO	I/O
31	PCIE_PERSTn	PCIe host indication to reset the device (input)	VIO	I
32	GND	System Ground Pin		
33	PCIE_RCLK_N	PCI Express Differential Clock Input—Negative		I
34	PCIE_RCLK_P	PCI Express Differential Clock Input—Positive		I
35	GND	System Ground Pin		
36	PCIE_TX_N	PCI Express Transmit Data—Negative		O
37	PCIE_TX_P	PCI Express Transmit Data—Positive		O
38	GND	System Ground Pin		
39	PCIE_RX_N	PCI Express Receive Data—Negative		I
40	PCIE_RX_P	PCI Express Receive Data—Positive		I
41	GND	System Ground Pin		
42	NC	No Connect		
43	NC	No Connect		
44	VIO_SD	Logic level for PCIe out-of-band signals.	VIO	I
45	WL_REG_ON	Used by PMU to power up or power down the internal module regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. Pulled up with a 4.7K ohms resistor internally.	VIO	I
46	SDIO_WAKE_L_GPIO_0	Reserve		

47	SDIO DAT3	Reserve		
48	SDIO DAT2	Reserve		
49	SDIO DAT1	Reserve		
50	SDIO DAT0	Reserve		
51	SDIO CMD	Reserve		
52	SDIO CLK	Reserve		
53	BT_HOST_WAKE	Bluetooth HOST_WAKE.	VIO	O
54	UART CTSn	Reserve		
55	UART SOUT	Reserve		
56	UART SIN	Reserve		
57	UART RTSn	Reserve		
58	PCM_SYNC	PCM sync; can be master (output) or slave (input).	VIO	I/O
59	PCM_IN	PCM data input	VIO	I
60	PCM_OUT	PCM data output	VIO	O
61	PCM_CLK	PCM bus clock; can be master (output) or slave (input)	VIO	I/O
62	GND	System Ground Pin		
63	BT_REG_ON	Bluetooth device wake-up: Signal from the host to the AW-CM217NF indicating that the host requires attention. • Asserted: The Bluetooth device must wake-up or remain awake. • Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. *This pin is BT_DEV_WAKE. The original BT_REG_ON is pulled high inside the module and can't be controlled by the host for BT USB mode	VIO	I

64	WL_LED_GPIO_7	It can be used as WL_LED.	VIO	O
65	BT_I2S_DO_BT_LED_L	It can be used as BT_LED.	VIO	O
66	NC	No Connect		
67	NC	No Connect		
68	GND	System Ground Pin		
69	USB_D-	USB Serial Differential Data Negative	3.3V	I/O
70	USB_D+	USB Serial Differential Data Positive	3.3V	I/O
71	GND	System Ground Pin		
72	3.3V	3.3V Power Supply	3.3V	I
73	VIO	Digital I/O Power Supply	VIO	I
74	GND	System Ground Pin		
75	GND	System Ground Pin		
76	GND	System Ground Pin		
77	GND	System Ground Pin		
78	GND	System Ground Pin		
79	GND	System Ground Pin		
80	GND	System Ground Pin		
81	GND	System Ground Pin		
82	GND	System Ground Pin		
83	GND	System Ground Pin		
84	GND	System Ground Pin		
85	GND	System Ground Pin		
86	GND	System Ground Pin		
87	GND	System Ground Pin		
88	GND	System Ground Pin		

89	GND	System Ground Pin		
90	GND	System Ground Pin		
91	GND	System Ground Pin		
92	GND	System Ground Pin		
93	GND	System Ground Pin		
94	GND	System Ground Pin		
95	GND	System Ground Pin		
96	GND	System Ground Pin		
G1	GND	System Ground Pin		
G2	GND	System Ground Pin		
G3	GND	System Ground Pin		
G4	GND	System Ground Pin		
G5	GND	System Ground Pin		
G6	GND	System Ground Pin		
G7	GND	System Ground Pin		
G8	GND	System Ground Pin		
G9	GND	System Ground Pin		
G10	GND	System Ground Pin		
G11	GND	System Ground Pin		
G12	GND	System Ground Pin		
G13	GND	System Ground Pin		
G14	GND	System Ground Pin		
G15	GND	System Ground Pin		
G16	GND	System Ground Pin		
G17	GND	System Ground Pin		
G18	GND	System Ground Pin		

G19	GND	System Ground Pin		
G20	GND	System Ground Pin		
G21	GND	System Ground Pin		
G22	GND	System Ground Pin		
G23	GND	System Ground Pin		
G24	GND	System Ground Pin		
G25	GND	System Ground Pin		
G26	GND	System Ground Pin		
G27	GND	System Ground Pin		
G28	GND	System Ground Pin		
G29	GND	System Ground Pin		
G30	GND	System Ground Pin		
G31	GND	System Ground Pin		
G32	GND	System Ground Pin		
G33	GND	System Ground Pin		
G34	GND	System Ground Pin		
G35	GND	System Ground Pin		
G36	GND	System Ground Pin		

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	Power supply for Internal Regulators	-0.3		5.5	V
VIO	DC supply voltage for digital I/O	-0.5		3.9	V

3.2 Recommended Operating Conditions

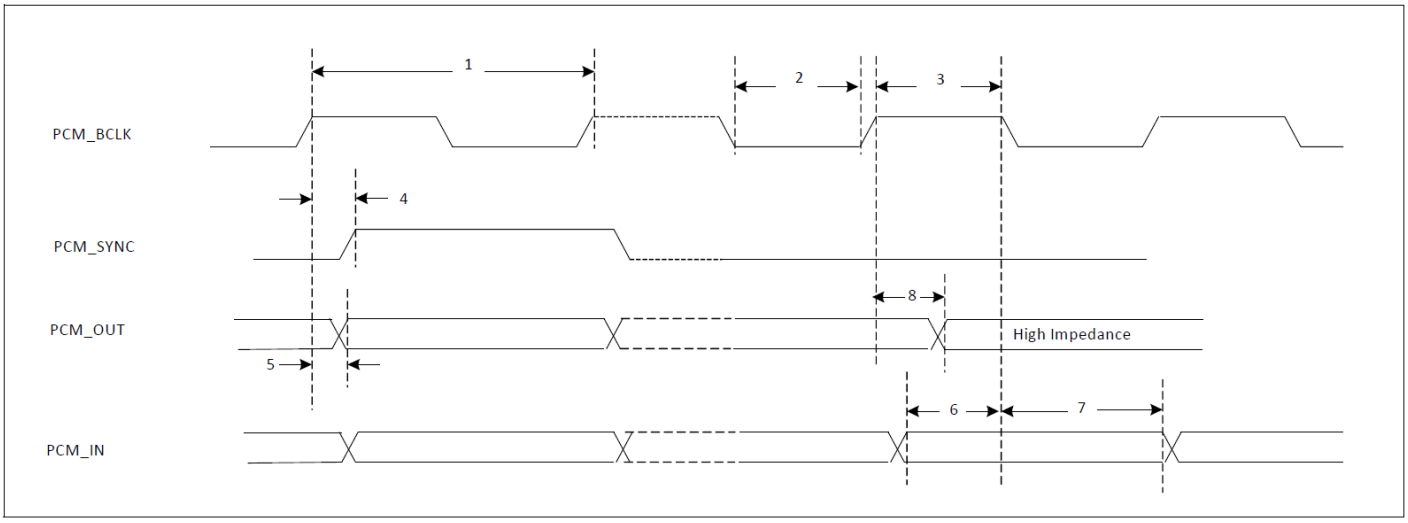
Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	Power supply for Internal Regulators	3.13	3.3	3.46	V

3.3 GPIO DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
PCIe out-of-band signals VIO_SD =1.8V					
VIH	Input high voltage	1.27	-	-	V
VIL	Input low voltage	-	-	0.58	V
VOH	Output High Voltage @ 2mA	1.4	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V
PCIe out-of-band signals VIO_SD =3.3V					
VIH	Input high voltage	2.06	-	-	V
VIL	Input low voltage	-	-	0.82	V
VOH	Output High Voltage @ 2mA	2.47	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.41	V
Other Digital Interface VIO=1.8V					
VIH	Input high voltage	1.17	-	-	V
VIL	Input low voltage	-	-	0.63	V
VOH	Output High Voltage @ 2mA	1.35	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V
Other Digital Interface VIO=3.3V					
VIH	Input high voltage	2	-	-	V
VIL	Input low voltage	-	-	0.8	V
VOH	Output High Voltage @ 2mA	2.9	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.4	V

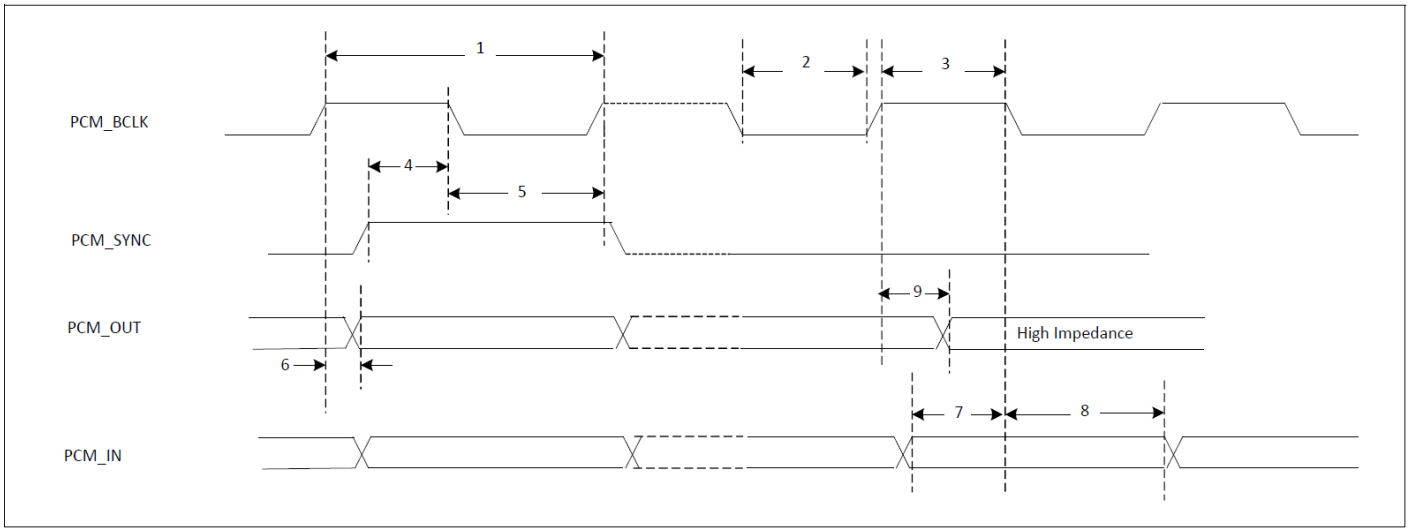
3.4 Host Interface

3.4.1 PCM Interface Timing



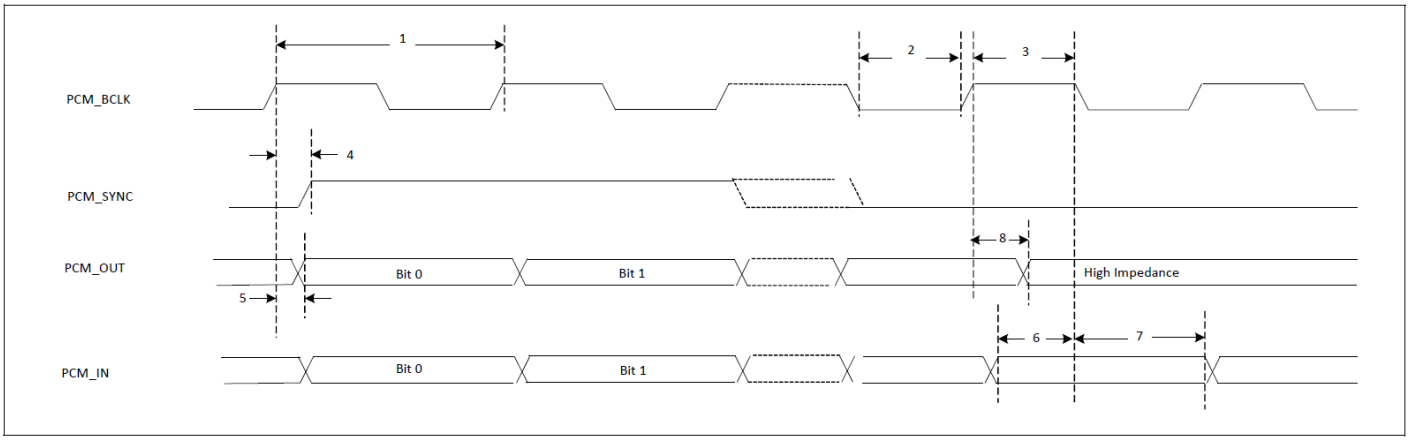
PCM Timing Diagram (Short Frame Sync, Master Mode)

Parameter	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC delay	0		25	ns
5	PCM_OUT delay	0		25	ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns



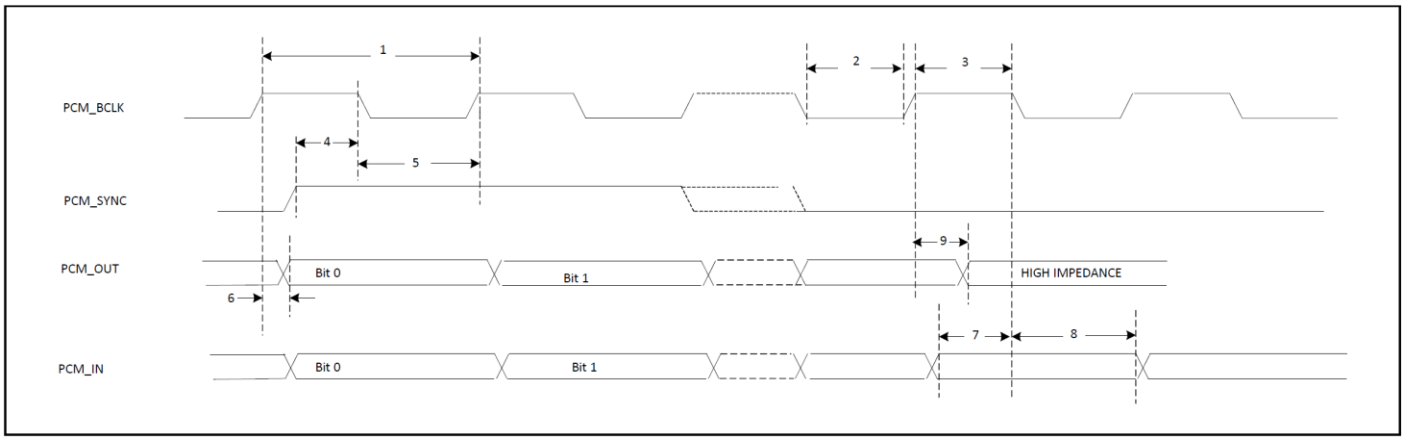
PCM Timing Diagram (Short Frame Sync, Slave Mode)

Parameter	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC setup	8			ns
5	PCM_SYNC hold	8			ns
6	PCM_OUT delay	0		25	ns
7	PCM_IN setup	8			ns
8	PCM_IN hold	8			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns



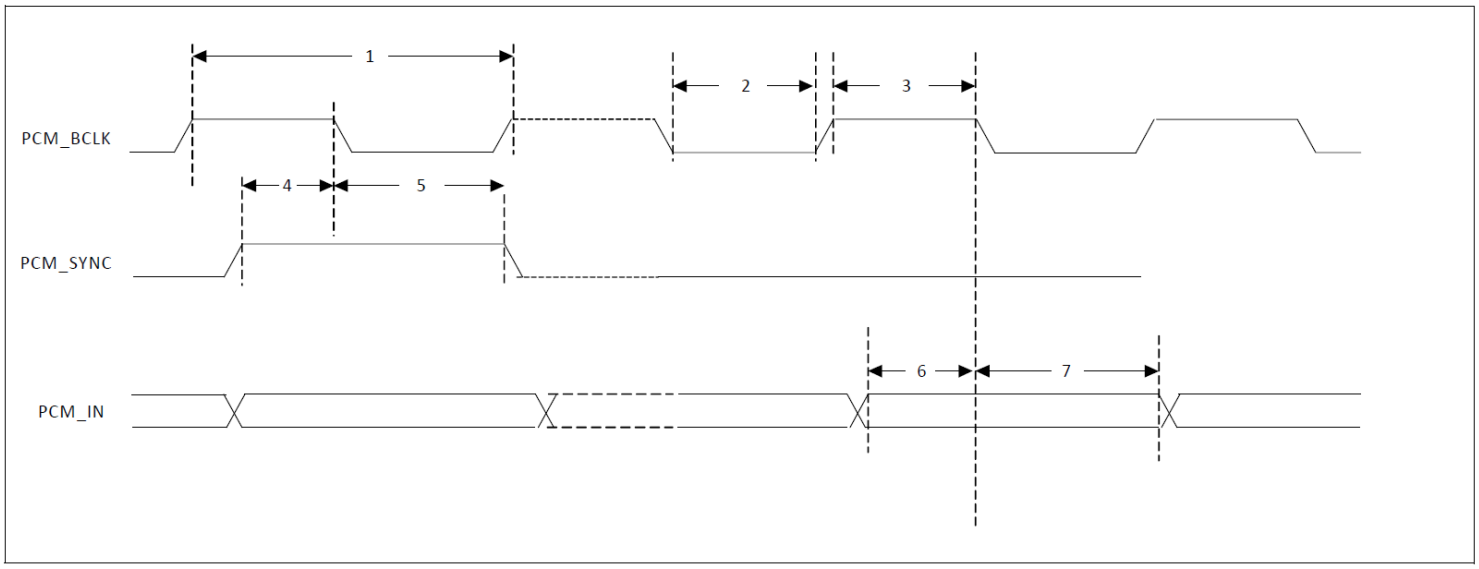
PCM Timing Diagram (Long Frame Sync, Master Mode)

Parameter	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC delay	0		25	ns
5	PCM_OUT delay	0		25	ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns



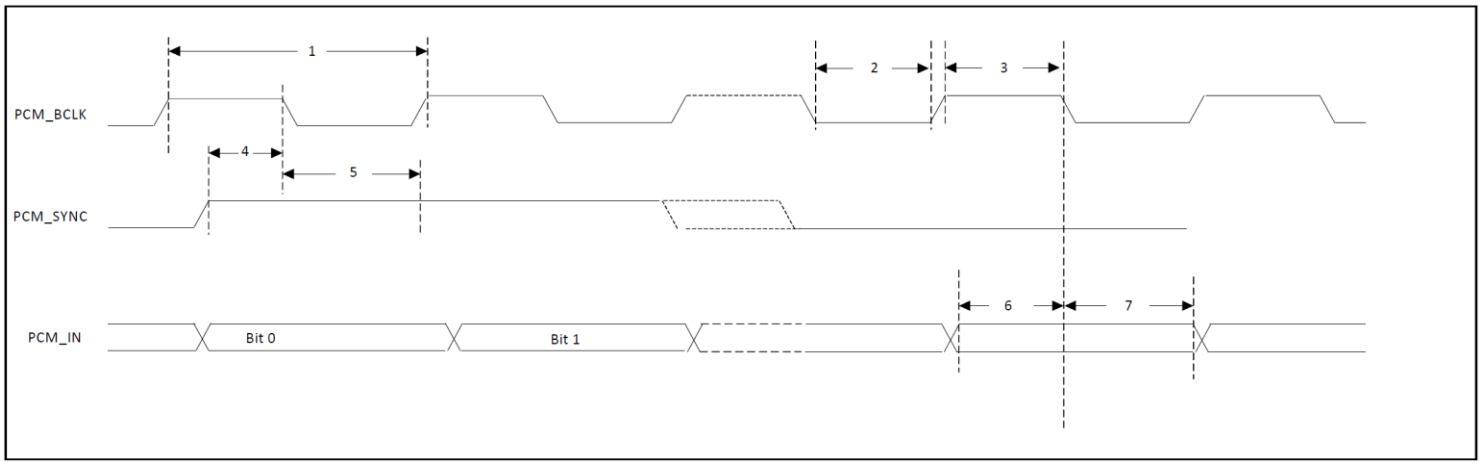
PCM Timing Diagram (Long Frame Sync, Slave Mode)

Parameter	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC setup	8			ns
5	PCM_SYNC hold	8			ns
6	PCM_OUT delay	0		25	ns
7	PCM_IN setup	8			ns
8	PCM_IN hold	8			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns



PCM Burst Mode Timing (Receive Only, Short Frame Sync)

Parameter	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			24	MHz
2	PCM bit clock low	20.8			ns
3	PCM bit clock high	20.8			ns
4	PCM_SYNC setup	8			ns
5	PCM_SYNC hold	8			ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns



PCM Burst Mode Timing (Receive Only, Long Frame Sync)

Parameter	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			24	MHz
2	PCM bit clock low	20.8			ns
3	PCM bit clock high	20.8			ns
4	PCM_SYNC setup	8			ns
5	PCM_SYNC hold	8			ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns

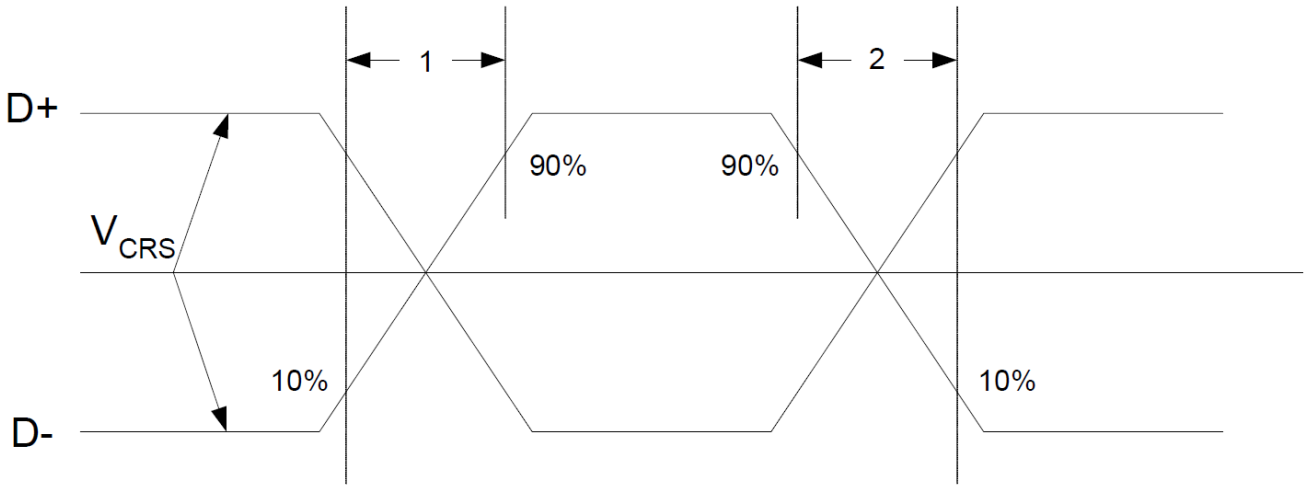
3.4.2 PCIe

The PCI Express (PCIe) core on the AW-CM217NF is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen1 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and AW-CM217NF device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

3.4.3 USB Interface



USB Full-Speed Timing

Parameter	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	Transition rise time	4	-	1.5	Bit periods
2	Transition fall time	4	-	0.5	Bit periods
3	Rise/fall timing matching	90	-	0.5	Bit periods
4	Full-speed data rate	12-0.25%		12+0.25%	Mbps

USB Full-Speed Timing Specifications

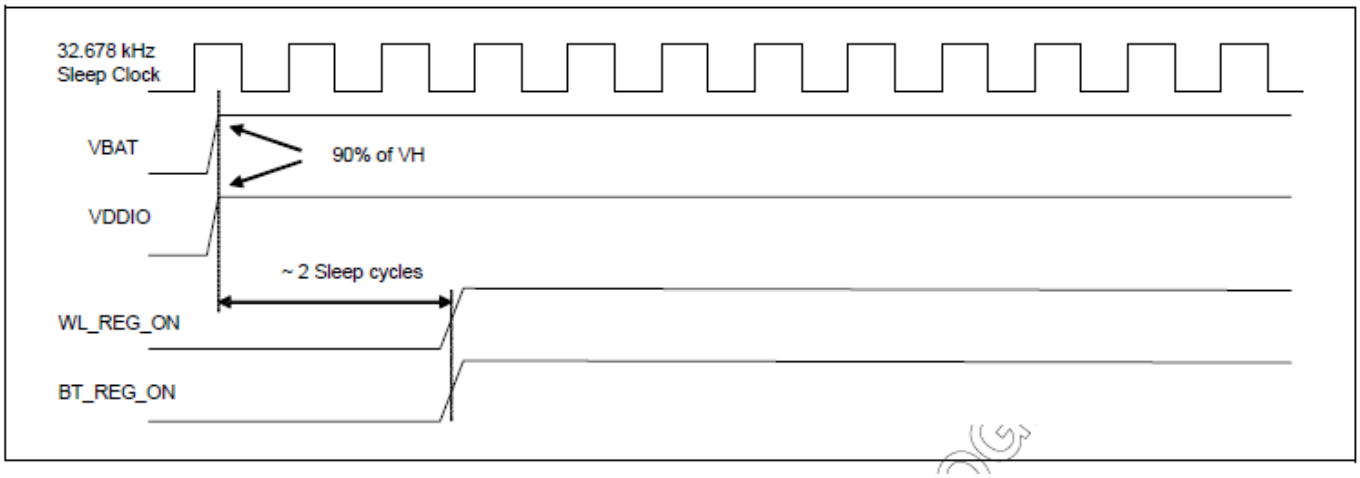
3.5 Power up Timing Sequence

The AW-CM217NF has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

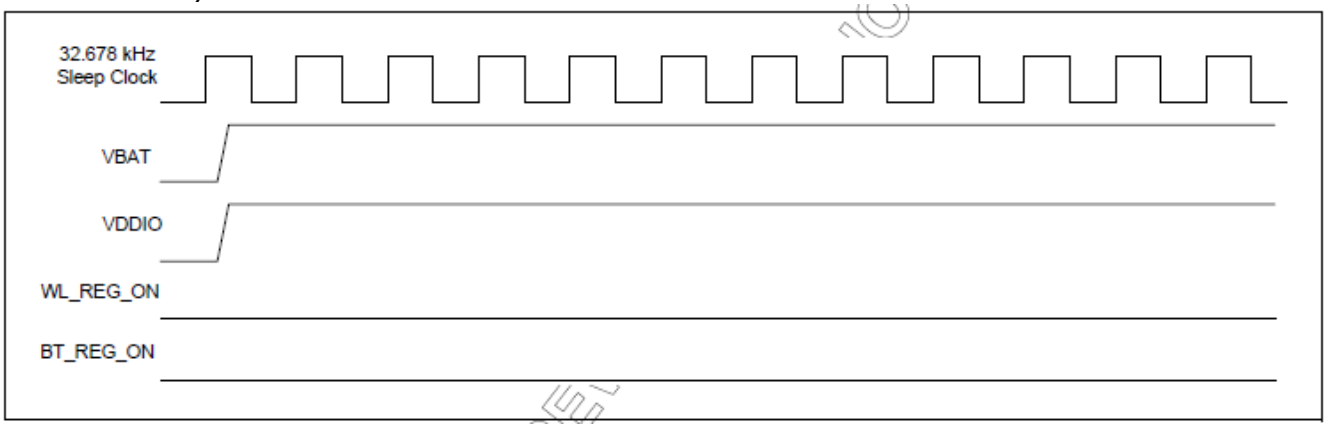
Note:

- **For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.**
- **VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high**.

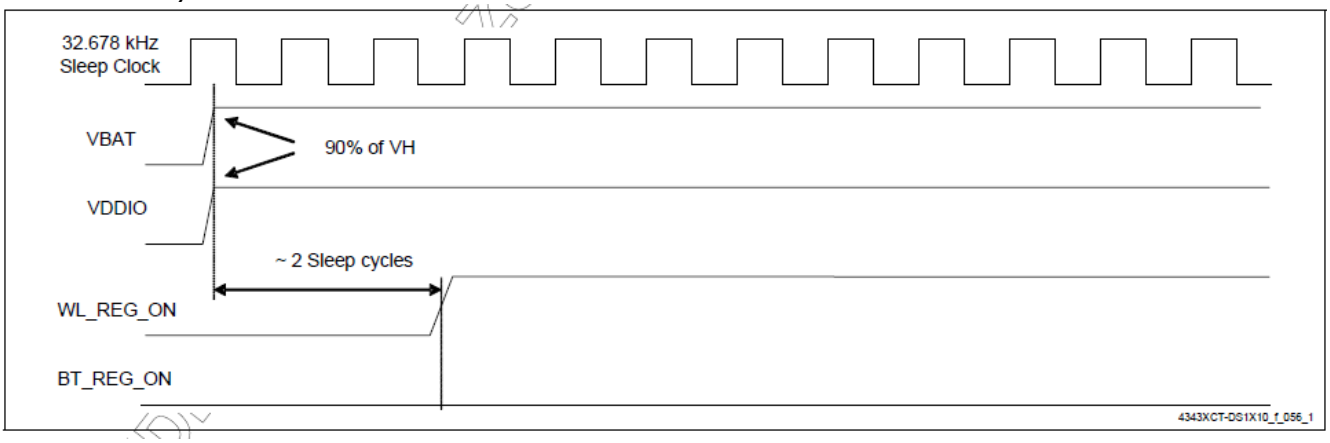
WLAN = ON, Bluetooth = ON



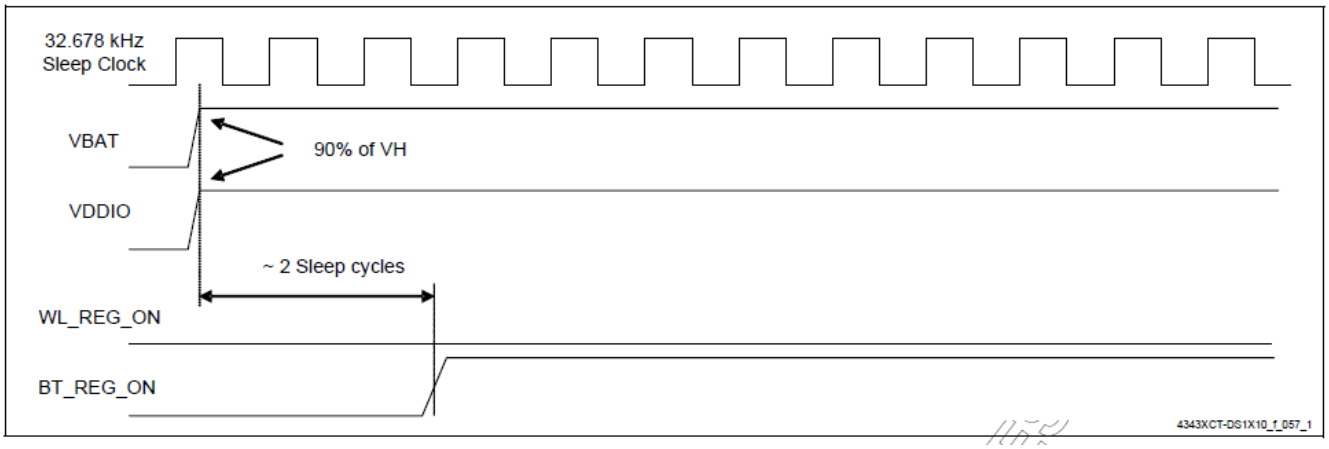
WLAN = OFF, Bluetooth = OFF



WLAN = ON, Bluetooth = OFF



WLAN = OFF, Bluetooth = ON



3.6 Power Consumption*

3.6.1 WLAN

Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit		Receive	
				Max.	Avg.	Max.	Avg.
2.4	11b@1Mbps	20	16	328.6	322.5	62.2	61.2
	11g@54Mbps	20	14	285.9	284.1	61.7	60.6
	11n@MCS7	20	13	274.3	272.4	61.8	59.8
	11n@MCS7	40	11	268.6	267.9	80.8	78.6
	11n@MCS15 MIMO	40	11	465.6	464.5	122.2	120.7
5	11a@54Mbps	20	13	279.8	279.4	77.4	77.1
	11n@MCS7	20	12	267.7	266.9	77.1	76.8
	11n@MCS7	40	10	280.0	279.2	95.8	95.5
	11ac@MCS9 SISO	80	8	311.4	310.4	128.3	128.0
	11ac@MCS9 MIMO	80	8	519.8	518.1	213.3	212.5

Current Unit: mA

3.6.2 Bluetooth

No.	Mode	Packet Type	VBAT_IN=3.3 V	
			Max.	Avg.
1	Sleep	n/a	3.0	
2	Transmit	DH5	25.0	24.5
3	Receive	3-DH5	16.9	16.7
4	AirPlane *(3)	n/a	1.5	1.5

Current Unit: mA

* The power consumption is based on Azurewave test environment, these data for reference only.

3.7 Frequency References

The AW-CM217NF uses an internal 37.4MHz xtal for normal operation and an external secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, a trade-off caused by this wide LPO tolerance is a small current consumption increase during WLAN power save mode that is incurred by the need to wake up earlier to avoid missing beacons.
The preferred approach for WLAN is to connect a precision external 32.768 kHz clock that meets the requirements listed in Table below.

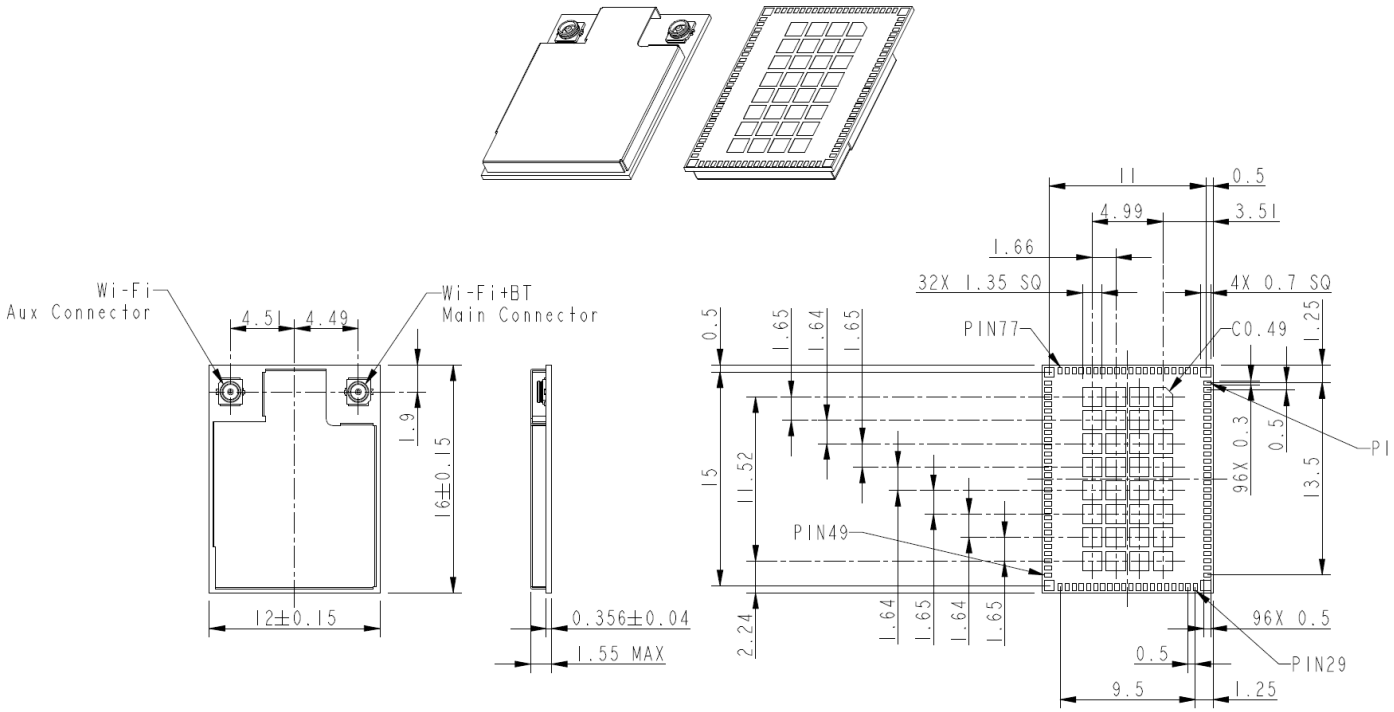
Parameter	LPO	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+-200	ppm
Duty cycle	30 - 70	%
Input signal amplitude	200 – 3300 [a]	mV , p-p
Input impedance [b]	>100	kΩ
	<5	pF
Signal type	Square-wave or sine-wave	-
Clock jitter (during initial start-up)	<10000	ppm

a. The input DC offset must be ≥ 0V to avoid conduction by the ESD protection diode.

b. When power is applied or switched off.

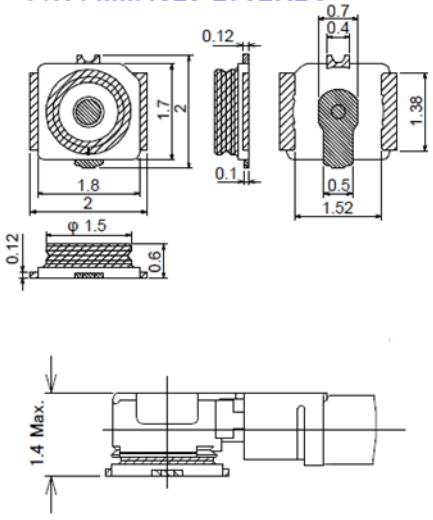
4. Mechanical Information

4.1 Mechanical Drawing

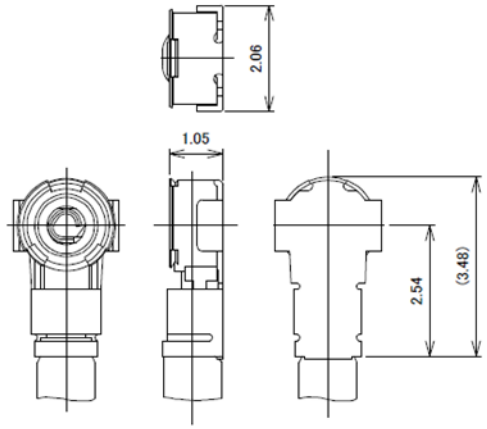


TOLERANCES UNLESS OTHERWISE SPECIFIED : ±0.15mm

HSC Receptacle
P/N : MM4829-2702RB0



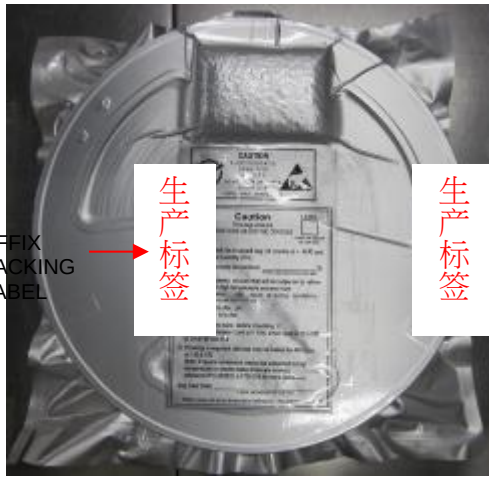
HSC Cable
P/N : MXHG_ _ _ _ _ _ _ _ _



5. Packaging Information

5.1

5.2



5.3

5.4

5.5

1 Carton= 5 Boxes

5.6