AzureWave Technologies, Inc.

AW-CB511NF

IEEE 802.11 a/b/g/n/ac WLAN 2T2R with Bluetooth 5.1 Combo Module (M.2 2230)

Datasheet

Rev. E

DF

(For Standard)

Features

WLAN

- IEEE 802.11ac Wave-2 compliant.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE 802.11ac/n beamforming.
- Supports RSDB.
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE and GPS.
- PCIe mode complies with PCI Express base specification
- Revision 3.0 for ×1 lane and power management running at Gen1 speed.
- Worldwide regulatory support: Global products supported with worldwide homologated design.
- Integrated Arm® Cortex® -R4 processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features.

Bluetooth

- Supports Bluetooth 5.1 optional features:
  - Angel or Arrival (AoA)
  - Angel of Departure (AoD)
  - GATT Cache
  - LE power control
- Supports all BT 5.0 optional features including LE-2Mbps, LE-Long Range, LE-Advertising extensions.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high speed UART interface and PCM for audio data.

Bluetooth (continued)

- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.

Revision History

Document NO: R2-2511NF-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/12/28	DCN019638	● Initial version	Licheng Wang	Chihhao Liao
B	2021/04/29	DCN021612	● Update AzureWave Format. ● Change pin 40 to CLK_REQ.	Licheng Wang	Chihhao Liao
C	2022/06/30	DCN026658	● Update to BT 5.1 ● Modify 4.1 Mechanical Drawing. ● Add Mark for ANT0 and ANT1. ● Update 1.3 Specifications Table for WLAN and BT. ● Modify 1.2.1 Block Diagram.	Licheng Wang	Chihhao Liao
D	2023/05/16	DCN029194	● Modify 3.4.2 UART description. ● Update 5. Packaging Information.	Licheng Wang	Chihhao Liao
E	2023/9/22	DCN030132	● Modify 1.3.3 Bluetooth output power.	Licheng Wang	Renton Tao

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced IEEE 802.11 ac/a/b/g/n 2x2 MIMO WLAN and Bluetooth M.2 combo module - AW-CB511NF. The Module is a complete dual-band (2.4 GHz and 5 GHz) Wi-Fi 2×2 MIMO MAC/PHY/Radio system-on-module. This 5G Wi-Fi single-chip device provides a high level of integration with a dual-stream IEEE 802.11ac MAC/baseband/radio and Bluetooth 5.1. In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 867 Mbps. In addition, all the rates specified in IEEE 802.11a/b/g/n are supported. Included on-chip are the 2.4 GHz and 5 GHz transmit power amplifiers and receive low-noise amplifiers. The WLAN operation supports two fully simultaneous SISO channels and real simultaneous dual-band (RSDB).

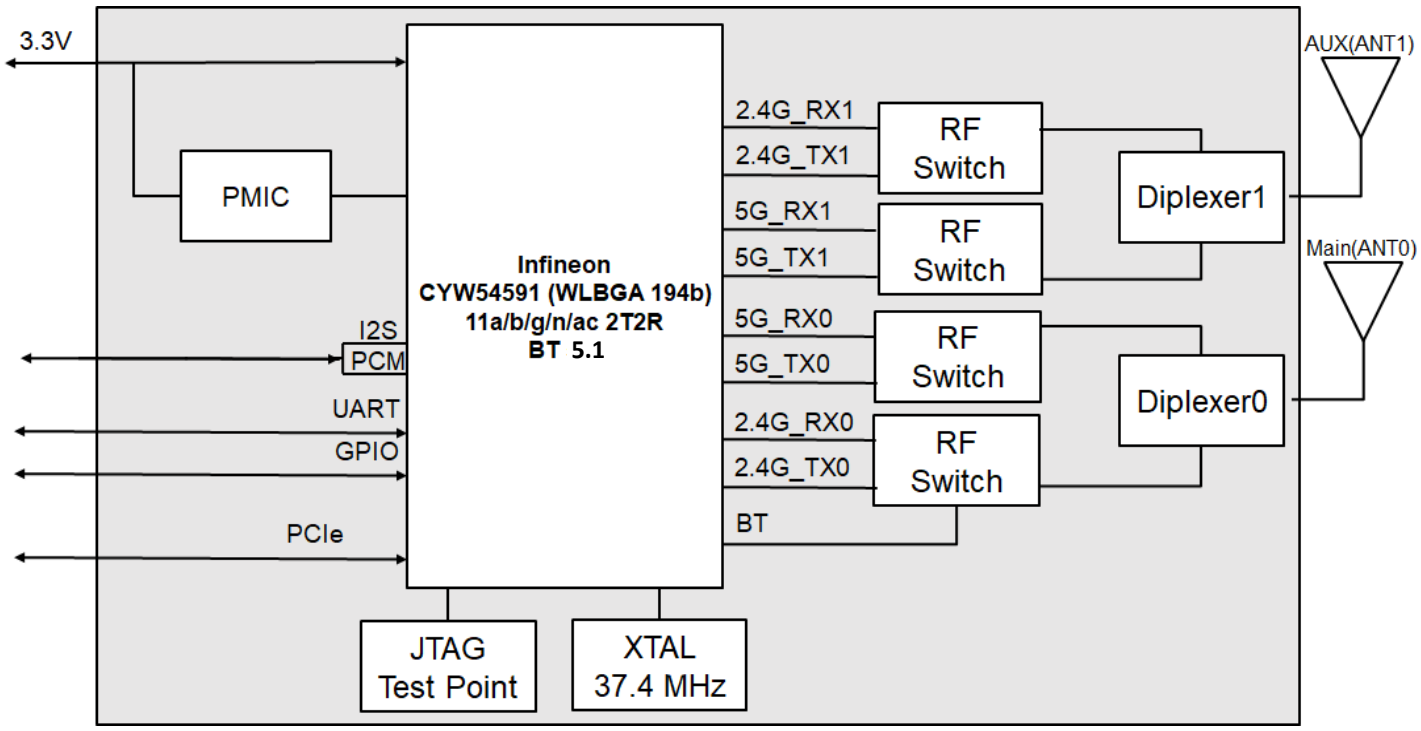
For the WLAN section, the device interfaces to a host SoM processor through a PCIe v3.0-compliant interface running at Gen1 speed.

For the Bluetooth section, Host interface is through a high-speed 4-wire UART interface and PCM interface for audio.

In addition, the AW-CB511NF implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms that ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. Coexistence support for external radios (such as LTE cellular and GPS) is provided via an external interface. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a Commercial/Consumer systems is achieved.

1.2 Block Diagram

1.2.1 Block Diagram



AW-CB511NF Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac WLAN 2T2R with Bluetooth 5.1 Combo Module (M.2 2230)
Major Chipset	Infineon CYW54591 (wlbga 194b)
Host Interface	Wi-Fi: PCIe , BT: UART/PCM
Dimension	22mm(L) 30xmm(W) x 2.25mm(H) (Typical)
Form factor	M.2 2230 E Key
Antenna	I-PEX MHF4 Connector Receptacle (20449) Ant 0(Main): Wi-Fi / BT → TX/RX Ant 1(Aux): Wi-Fi → TX/RX
Weight	2.45g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant
WLAN VID/PID	NA
WLAN SVID/SPID	NA
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	802.11a/g/n/ac: OFDM 802.11b: CCK(11, 5.5Mbps), DQPSK(2Mbps), BPSK(1Mbps)
Number of Channels	**2.4GHz** ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13 **5GHz** USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

Output Power[1] (Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<35%	16.5	18.5	20.5	dBm
11g (54Mbps) @EVM≦-27 dB	16.5	18.5	20.5	dBm
11n (HT20 MCS7) @EVM≦-28 dB	16	18	20	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM≦-27 dB	13	15	17	dBm
11n (HT20 MCS7) @EVM≦-28 dB	13	15	17	dBm
11n (HT40 MCS7) @EVM≦-28 dB	12	14	16	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	12	14	16	dBm
11ac (VHT40 MCS9) @EVM≦-32 dB	12	14	16	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	10.5	12.5	14.5	dBm

Receiver Sensitivity

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-90	-87	dBm
11g (54Mbps)		-77	-74	dBm
11n (HT20 MCS7)		-76	-73	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		-75.5	-72.5	dBm
11n (HT20 MCS7)		-74	-71	dBm
11n (HT40 MCS7)		-71	-68	dBm
11ac (VHT20 MCS8)[2]		-69	-66	dBm
11ac (VHT40 MCS9)[3]		-63	-60	dBm
11ac (VHT80 MCS9)[4]		-61	-58	dBm

[1] EVM Spec are under typical test conditions.
[2] Tested by BCC instead of LDPC.
[3] Tested by BCC instead of LDPC.
[4] Tested by BCC instead of LDPC.

Data Rate	WLAN: 802.11b : 1, 2, 5.5, 11Mbps 802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac/n : Maximum data rates up to 192.6 Mbps(20MHz channel),400 Mbps (40 MHz channel), 866.7 Mbps (80 MHz channel)
Security	● WPA, WAPI STA, and WPA2 (Personal) support for powerful encryption and authentication. ● AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility. ● Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS).

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	**Description**
Bluetooth Standard	BT5.1+Enhanced Data Rate (EDR)
Bluetooth VID/PID	N/A
Frequency Rage	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: 4-DQPSK Payload 3M: 8DPSK
Output Power	

	Min	Typ	Max	Unit
BR	8	11	14	dBm
BLE(1M)	8	11	14	dBm
BLE(2M)	7	10.5	13.5	dBm

Receiver Sensitivity[5]

	Min	Typ	Max	Unit
BR		-91	-88	dBm
EDR(π/4-DQPSK)		-94	-91	dBm
EDR(8DPSK)		-89	-86	dBm
BLE(1M)		-99	-96	dBm
BLE(2M)		-96	-93	dBm

[5] Tested by sLNA.

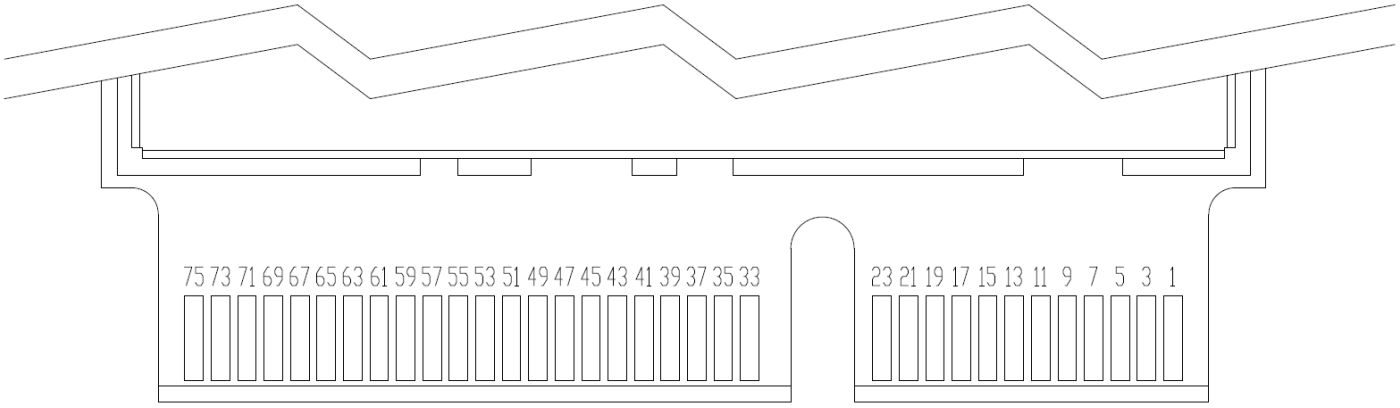
1.3.4 Operating Conditions

Operating Conditions	
Voltage	Power supply for host:3.3V
Operating Temperature	-40℃ to +85℃[6]
Operating Humidity	less than 85% R.H.
Storage Temperature	-40℃ to +85℃
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	2KV per JEDEC EID/JESD22-A114
Changed Device Model	300V per JEDEC EIA/JESD22-C101

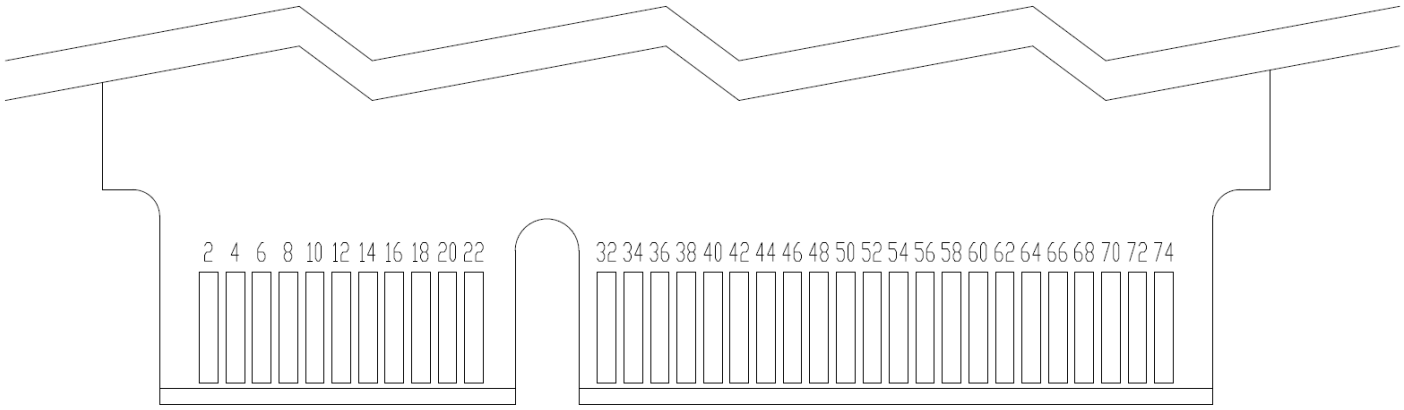
[6] -40℃~85℃ is Functional operation, for detail please check with AzureWave FAE.

2. Pin Definition

2.1 Pin Map



AW-CB511NF Pin Map (Top View)



AW-CB511NF Pin Map (Bottom View)

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GND	System Ground Pin		
2	3.3V	3.3V Power Supply	3.3V	I
3	NC	NC		
4	3.3V	3.3V Power supply input	3.3V	I
5	NC	NC		
6	NC	NC		
7	GND	System Ground Pin		
8	PCM_CLK/I2S_SCK	PCM clock; can be master (output) or slave (input). I2S clock, can be master (output) or slave (input).	1.8V	I/O
9	NC	NC		
10	PCM_SYNC/I2S_WS	PCM sync; can be master (output) or slave (input). I2S WS; can be master (output) or slave (input).	1.8V	I/O
11	NC	NC		
12	PCM_OUT/I2S_SD_OUT	PCM data output. I2S data output.	1.8V	O
13	NC	NC		
14	PCM_IN/I2S_SD_IN	PCM data input. I2S data input.	1.8V	I
15	NC	NC		
16	NC	NC		
17	NC	NC		
18	GND	System Ground Pin		
19	NC	NC		
20	BT_HOST_WAKE	Bluetooth HOST_WAKE	3.3V	I/O
21	NC	NC		
22	BT_UART_TXD	UART serial output. Serial data output for the HCI UART interface.	1.8V	O
23	NC	NC		

24	NC	NC		
25	NC	NC		
26	NC	NC		
27	NC	NC		
28	NC	NC		
29	NC	NC		
30	NC	NC		
31	NC	NC		
32	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	1.8V	I
33	GND	System Ground Pin		
34	BT_UART_RTS	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	1.8V	O
35	PERp0	PCIe receiver differential pair (×1 lane).	3.3V	I
36	BT_UART_CTS	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	1.8V	I
37	PERn0	PCIe receiver differential pair (×1 lane).	3.3V	I
38	NC	NC		
39	GND	System Ground Pin		
40	CLK_REQ	Reference clock request (shared by BT and WLAN). If not used, this can be no-connect.	1.8V	O
41	PETp0	PCIe transmitter differential pair (×1 lane).	3.3V	O
42	BT_DEV_WAKE	Bluetooth DEV_WAKE.	1.8V	I/O
43	PETn0	PCIe transmitter differential pair (×1 lane).	3.3V	O
44	NC	NC		
45	GND	System Ground Pin		
46	GPIO9_WL_UART_TX_1V8	GPIO.	1.8V	I/O
47	REFCLKp0	PCIe differential Clock inputs (negative and positive). 100 MHz differential	3.3V	I
48	GPIO8_WL_UART_RX_1V8	GPIO.	1.8V	I/O
49	REFCLKn0	PCIe differential Clock inputs (negative and positive). 100 MHz differential	3.3V	I

50	EXT_LPO	External sleep clock input (32.768 kHz).	3.3V	I
51	GND	System Ground Pin		
52	PERST0	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1. PERST0 pad excludes internal pull-up.	3.3V	I
53	CLKREQ0	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.	3.3V	OD
54	W_DISABLE2	BT_REG_ON; Used by PMU to power up or power down the internal AW-CB511NF regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.	3.3V	I
55	PEWAKE0	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.	3.3V	OD
56	W_DISABLE1	WL_REG_ON; Used by PMU to power up or power down the internal AW-CB511NF regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.	3.3V	I
57	GND	System Ground Pin		
58	NC	NC		
59	NC	NC		
60	NC	NC		
61	NC	NC		
62	NC	NC		
63	GND	System Ground Pin		
64	NC	NC		
65	NC	NC		
66	NC	NC		

67	NC	NC		
68	NC	NC		
69	GND	System Ground Pin		
70	NC	NC		
71	NC	NC		
72	3.3V	3.3V Power Supply	3.3V	I
73	NC	NC		
74	3.3V	3.3V Power Supply	3.3V	I
75	GND	System Ground Pin		

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	DC supply voltage for VBAT and VDDIO.	-0.5	-	+3.9	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply voltage for VBAT and VDDIO.	3[7]	3.3	3.6	V

3.3 Digital IO Pin DC Characteristics

3.3.1 PCIe Out-of-Band Signals (PERST0, PEWAKE0, and CLKREQ0)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO=1.8V					
V_{IH}	Input high voltage (V_{DDIO})	1.27	-	3.63	V
V_{IL}	Input low voltage (V_{DDIO})	-	-	0.58	V
V_{OL}	Output Low Voltage @ 2mA	-	-	0.45	V
VDDIO=3.3V					
V_{IH}	Input high voltage (V_{DDIO})	0.625 × VDDIO	-	3.63	V
V_{IL}	Input low voltage (V_{DDIO})	-	-	0.25 × VDDIO	V
V_{OL}	Output Low Voltage @ 2mA	-	-	0.125 × VDDIO	V

[7] AW-CB511NF is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 3.6V.

3.3.2 Other Digital I/O Pins

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO=1.8V					
V_{IH}	Input high voltage (V_{DDIO})	0.65 × VDDIO	-	3.63	V
V_{IL}	Input low voltage (V_{DDIO})	-	-	0.35 × VDDIO	V
V_{OH}	Output High Voltage @ 2mA	VDDIO – 0.45	-	-	V
V_{OL}	Output Low Voltage @ 2mA	-	-	0.45	V
VDDIO=3.3V					
V_{IH}	Input high voltage (V_{DDIO})	2.0	-	3.63	V
V_{IL}	Input low voltage (V_{DDIO})	-	-	0.8	V
V_{OH}	Output High Voltage @ 2mA	VDDIO – 0.4	-	-	V
V_{OL}	Output Low Voltage @ 2mA	-	-	0.4	V

3.4 Power Up Timing Sequence

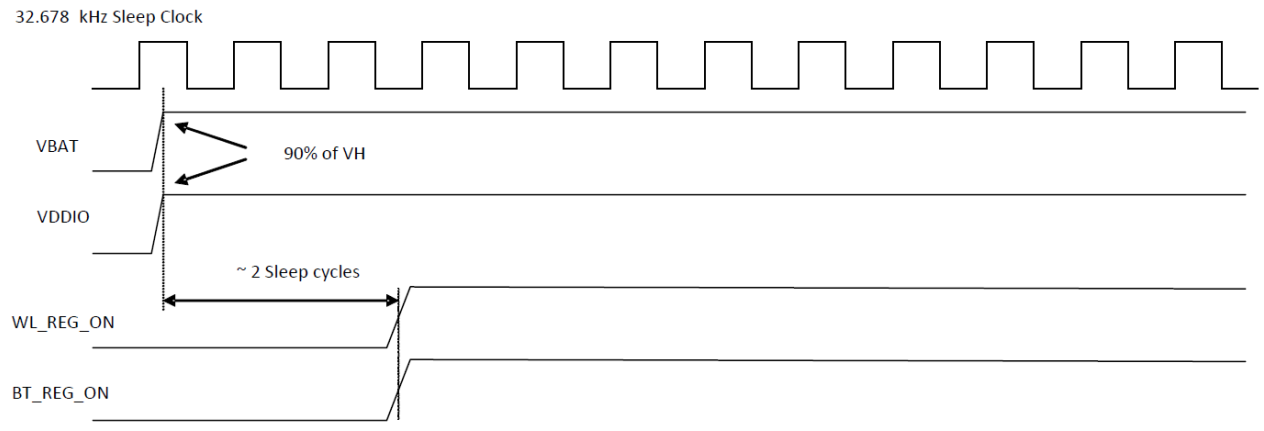
The AW-CB511NF has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals (Power-Up/Power-Down/Reset Control Signals)

Signal	***Description***
W_DISABLE1 (WL_REG_ON)	Used by the PMU to power up the WLAN section. It is also OR-gated with the W_DISABLE2(BT_REG_ON) input to control the internal AW-CB511NF regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the W_DISABLE2(BT_REG_ON) and W_DISABLE1(WL_REG_ON) pins are low, the regulators are disabled.
W_DISABLE2 (BT_REG_ON)	Used by the PMU (OR-gated with W_DISABLE1) to power up the internal AW-CB511NF regulators. If both the W_DISABLE2(BT_REG_ON) and W_DISABLE1(WL_REG_ON) pins are low, the regulators are disabled. When this pin is low and W_DISABLE1(WL_REG_ON), the BT section is in reset.

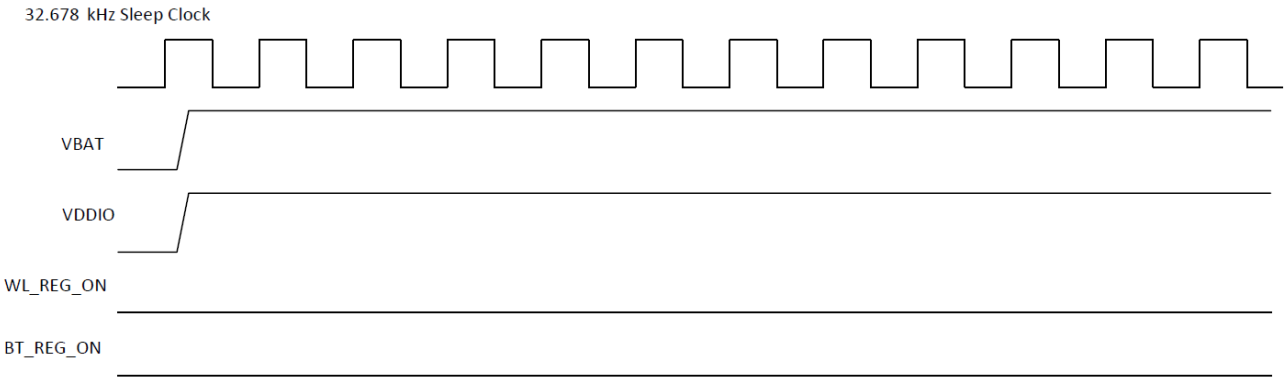
Control Signal Timing Diagrams

WLAN = ON, Bluetooth = ON



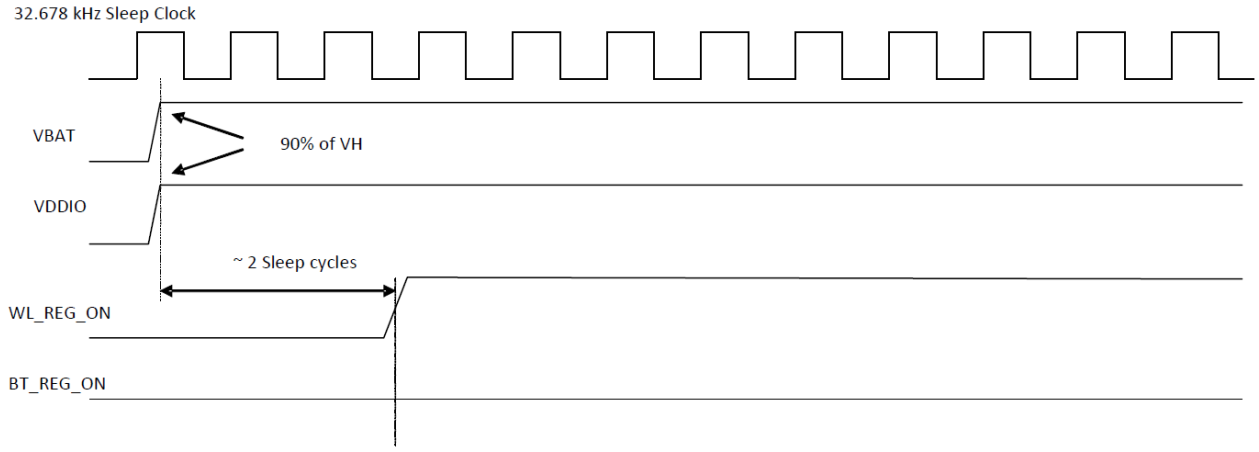
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF



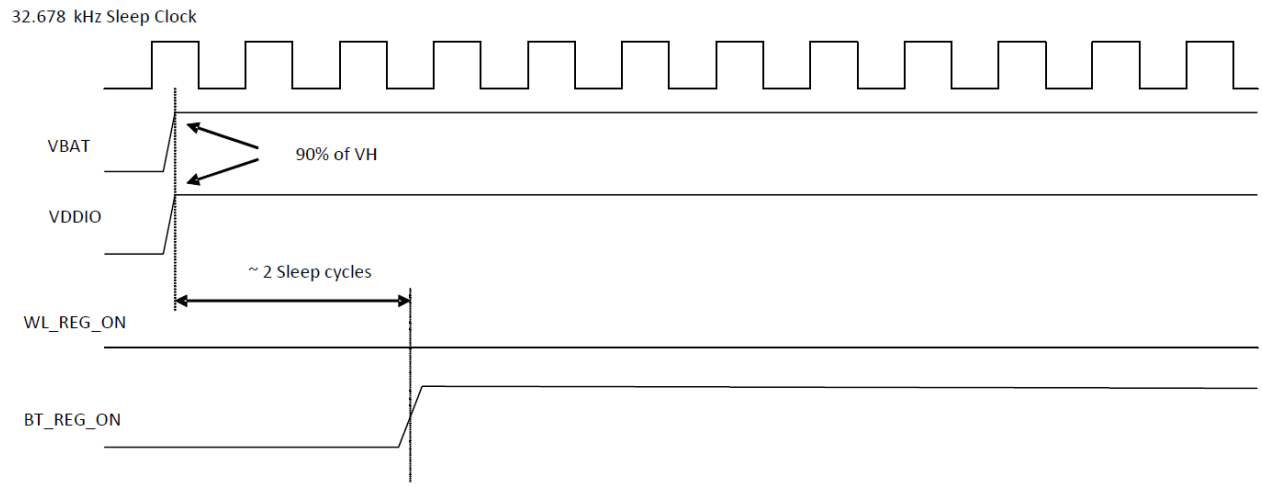
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF



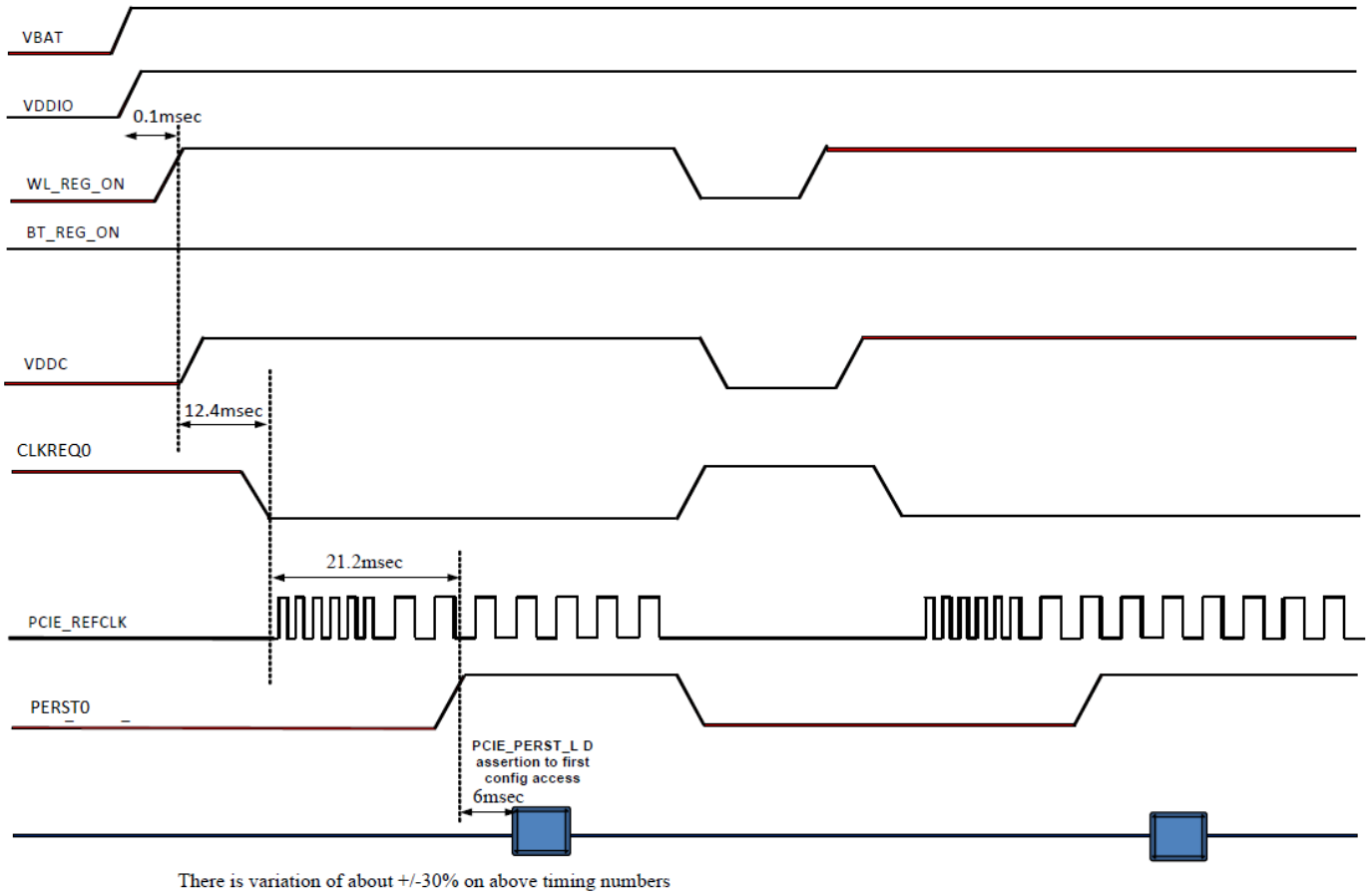
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = ON



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN Power-Up Sequence for PCIe Host



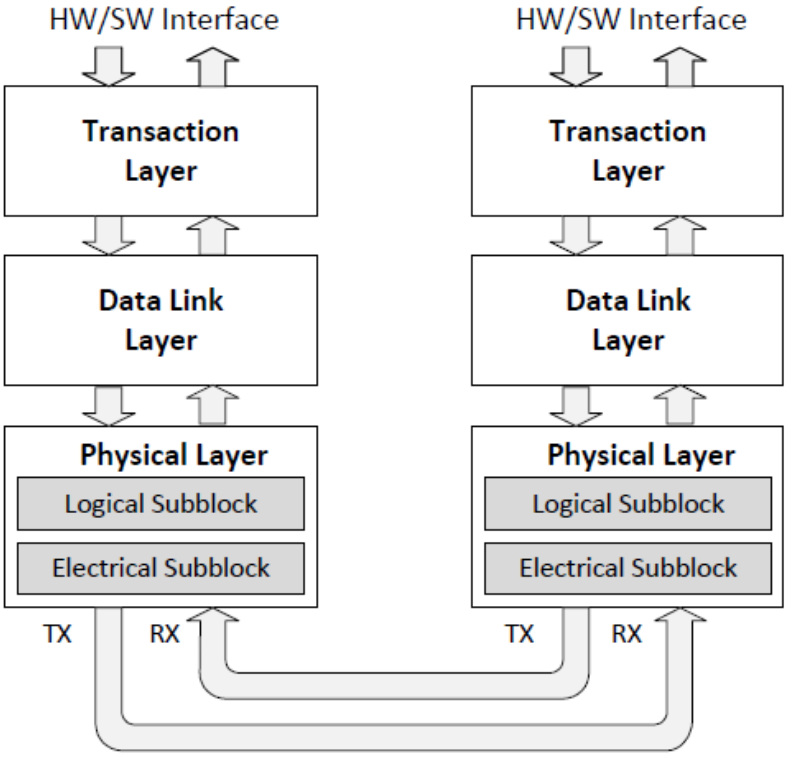
There is variation of about +/-30% on above timing numbers

3.4.1 PCI Express (PCIe) Interface Specification

The PCI Express core on the AW-CB511NF is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen1 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in below figure. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and AW-CB511device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.



3.4.2 UART Interface

The AW-CB511NF UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.1 UART HCI specification: H4, and H5. The default baud rate is 115.2 Kbaud.

The CYW54591 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP).It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

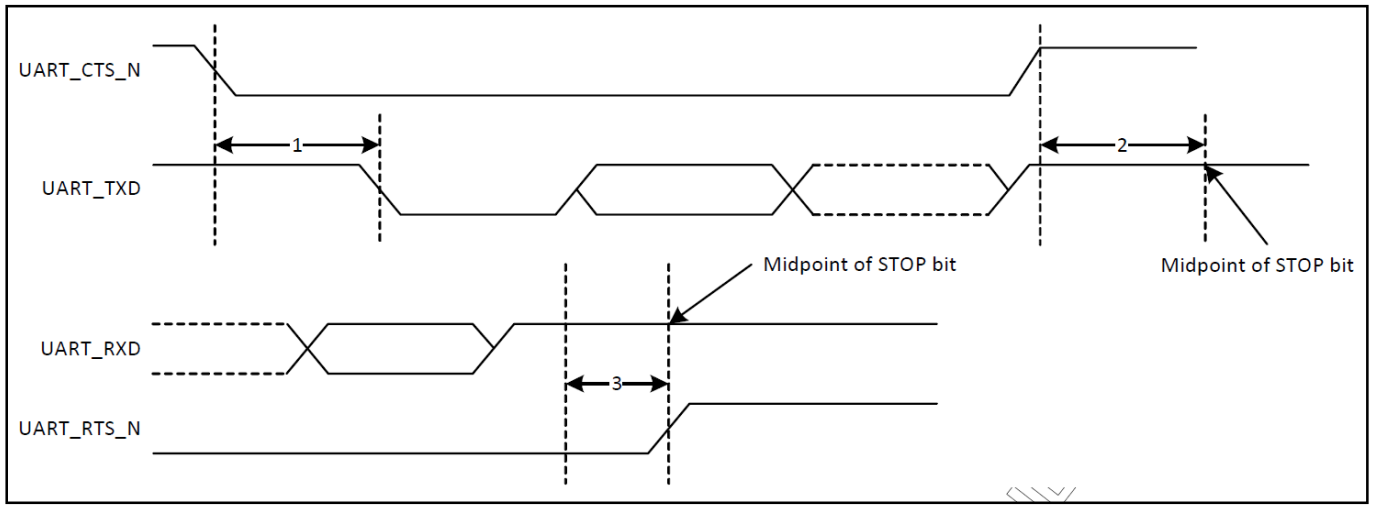
Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-CB511NF UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.UART Interface Signals

PIN No.	Name	Description	Type
22	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	O
32	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	I
34	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	O
36	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	I

Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing



UART Timing Specifications

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

3.4.3 I2S Interface

The AW-CB511NF supports I2S digital audio port for Bluetooth audio which shared the pin out with PCM interface.

The I2S signals are:

■ I2S clock: I2S_SCK

■ I2S Word Select: I2S_WS

■ I2S Data Out: I2S_SD_OUT

■ I2S Data In: I2S_SD_IN

I2S_SCK and I2S_WS become outputs in Master mode and inputs in Slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSb of the left-channel data is aligned with the MSb of the I2S bus, in accord with the I2S specification. The MSb of each data word is transmitted one bit clock cycle after the I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when I2S_WS is LOW, and right channel data is transmitted when I2S_WS is HIGH. Data bits sent by the AW-CB511NF are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SCK.

The clock rate in master mode is either of the following:

48 kHz × 32 bits per frame = 1.536 MHz

48 kHz × 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

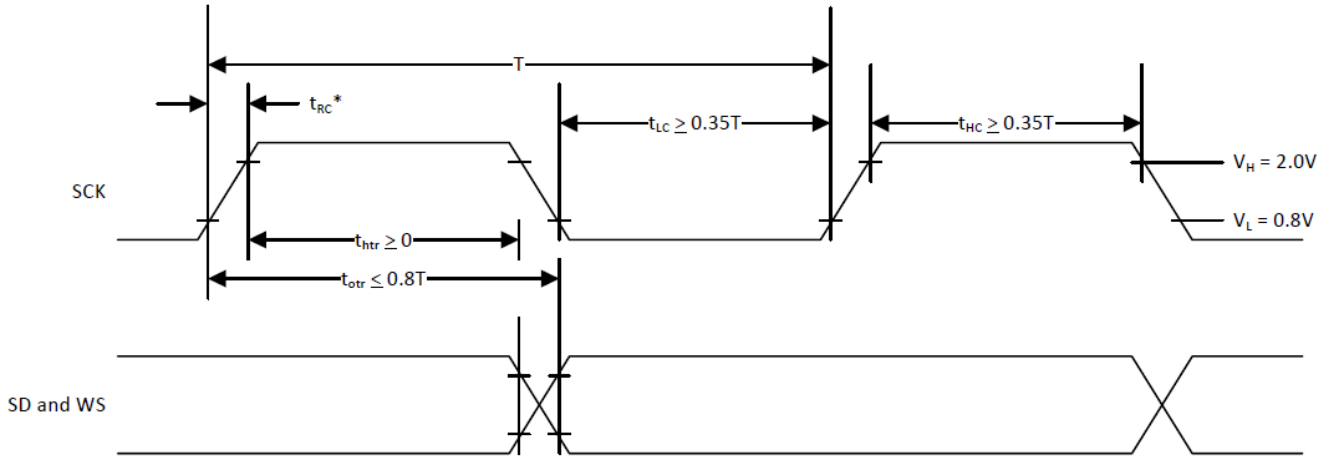
I2S Timing

	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	7
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	8
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	8
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	9
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	9
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	10
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	11
Hold time t_{htr}	0	–	–	–	–	–	–	–	10
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	12
Hold time t_{hr}	–	–	–	–	–	0	–	–	12

Notes

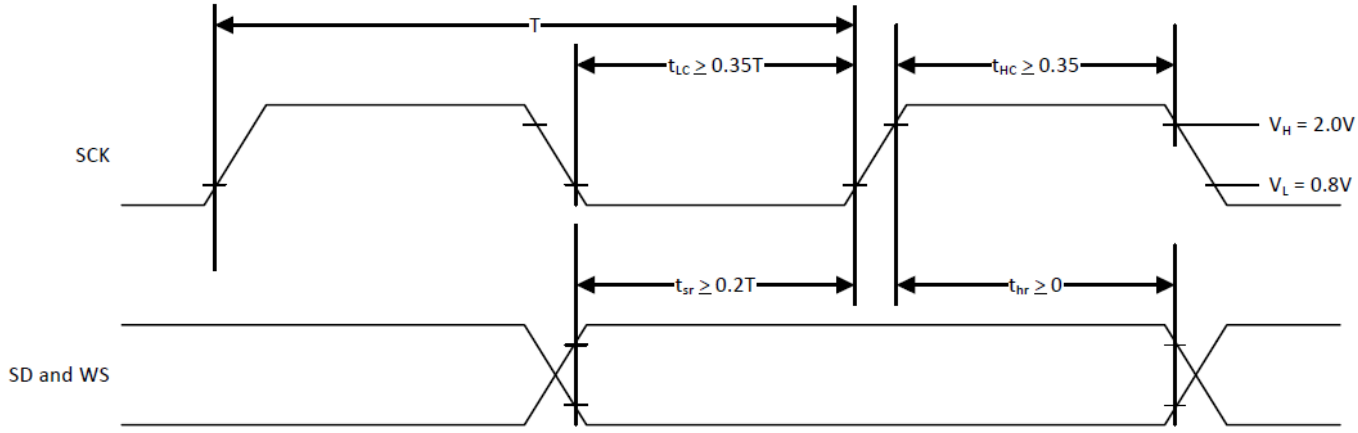
7. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
8. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
9. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
10. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
11. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
12. The data setup and hold time must not be less than the specified receiver setup and hold time.

I2S Transmitter Timing[8]



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

I2S Receiver Timing[9]



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

[8] The time periods specified in I2C transmitter timing and I2C receiver timing are defined by the transmitter speed. The receiver specifications must match transmitter performance.

[9] The time periods specified in I2C transmitter timing and I2C receiver timing are defined by the transmitter speed. The receiver specifications must match transmitter performance.

3.4.4 PCM Interface

The AW-CB511 supports independent PCM interfaces that share the pins with the I2S interfaces. The PCM Interface on the AW-CB511NF can connect to linear PCM codec devices in Master/Slave mode. In Master mode, the AW-CB511NF generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in Slave mode, these signals are provided by another master on the PCM interface and are inputs to the AW-CB511NF.
The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

3.4.4.1 Slot Mapping

The AW-CB511NF supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from a SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

3.4.4.2 Frame Synchronization

The AW-CB511NF supports both short and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

3.4.4.3 Data Formatting

The AW-CB511NF may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the AW-CB511NF uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked Most Significant Bit (MSb) first.

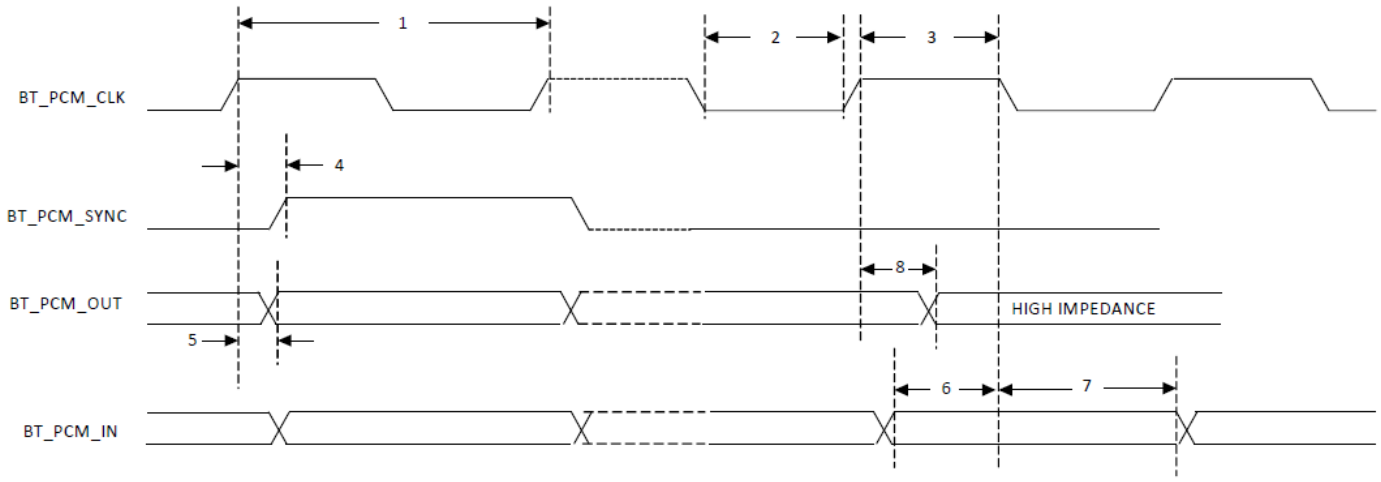
3.4.4.4 Wideband Speech Support

When the host encodes WBS packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The AW-CB511NF also supports slave transparent mode using a proprietary rate-matching scheme. In SBCcode mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

3.4.4.5 PCM Interface Timing

Short Frame Sync, Master Mode

PCM Timing Diagram (Short Frame Sync, Master Mode)

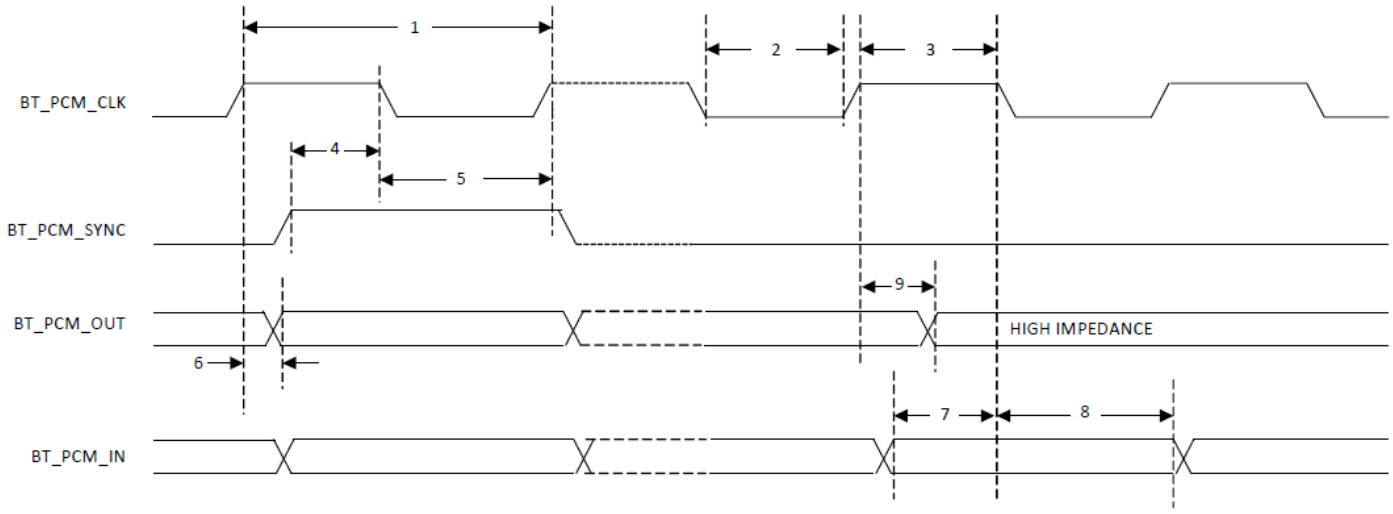


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC delay	0	–	25.0	ns
5	BT_PCM_OUT delay	0	–	25.0	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

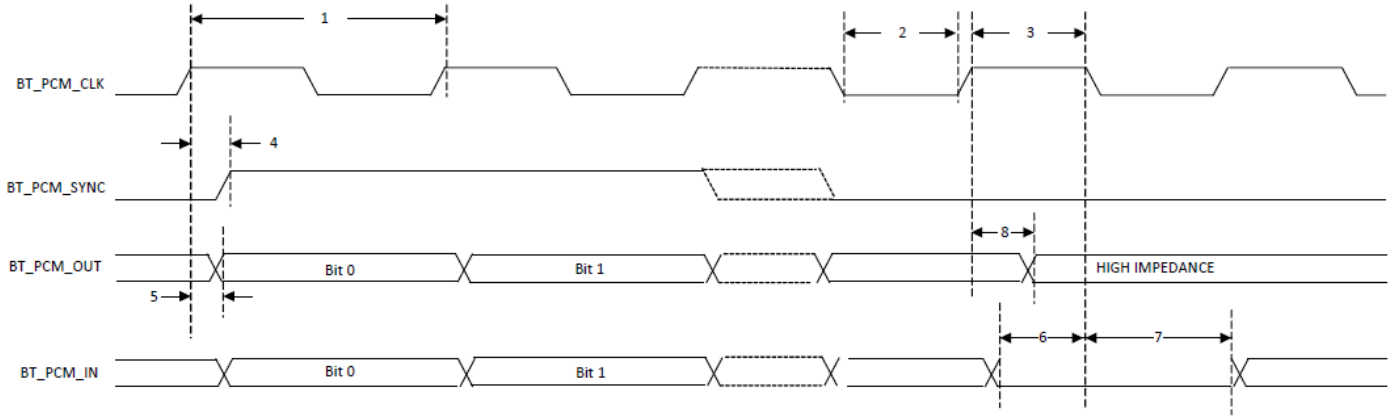


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_OUT delay	0	–	25.0	ns
7	BT_PCM_IN setup	8.0	–	–	ns
8	BT_PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

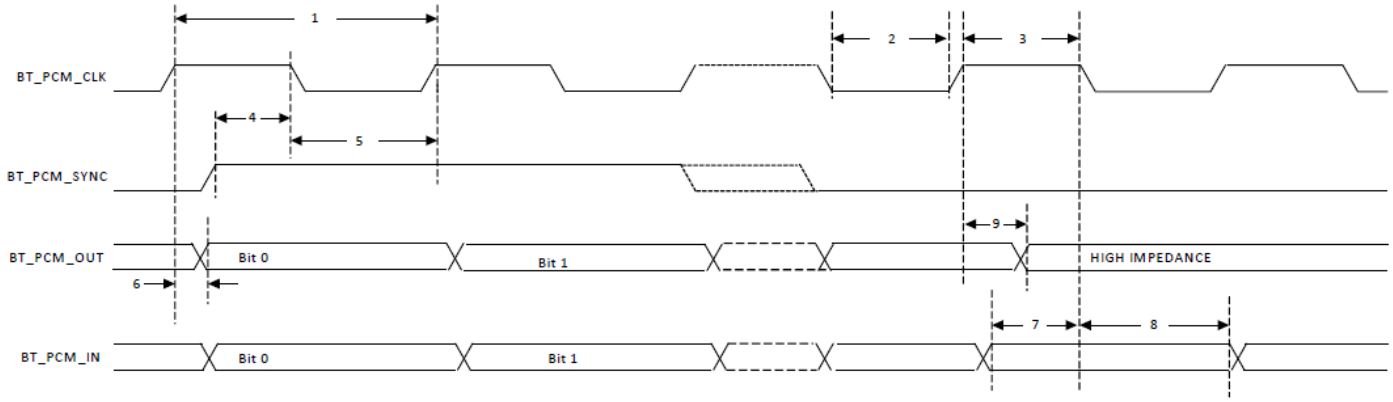


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC delay	0	–	25.0	ns
5	BT_PCM_OUT delay	0	–	25.0	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_OUT delay	0	–	25.0.	ns
7	BT_PCM_IN setup	8.0	–	–	ns
8	BT_PCM_IN hold	8.0.	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

3.5 Power Consumption*

3.5.1 WLAN

No.	Item	Total(VDDIO+VBAT)_IN=3.3V	
		Max.	Avg.
1	power off*(1)(2)(4)	TBD	TBD
2	Deepsleep (VBAT) (2)(3)(4)(5)	TBD	TBD
3	Deepsleep (VDDIO) (2)(3)(4)(5)	TBD	TBD
4	Deepsleep (total) (2)(3)(4)(5)	TBD	TBD
5	Power Save (2.4G) (2) (3)(4)(6)(7)	TBD	TBD
6	Power Save (5G) (2) (3)(4)(6)(7)	TBD	TBD

Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit			Receive	
				Max.	Avg.	Duty %	Max.	Avg.
2.4	11b@1M	20	17	TBD	TBD	TBD	TBD	TBD
	11b@11M	20	17	TBD	TBD	TBD	TBD	TBD
	11g@6M	20	14	TBD	TBD	TBD	TBD	TBD
	11g@54M	20	14	TBD	TBD	TBD	TBD	TBD
	11n@MCS0	20	13	TBD	TBD	TBD	TBD	TBD
	11n@MCS7	20	13	TBD	TBD	TBD	TBD	TBD
5	11a@6M	20	15	TBD	TBD	TBD	TBD	TBD
	11n@MCS0	20	15	TBD	TBD	TBD	TBD	TBD
	11n@MCS7	20	15	TBD	TBD	TBD	TBD	TBD
	11n@MCS0	40	15	TBD	TBD	TBD	TBD	TBD
	11ac@MCS0 NSS1	80	12	TBD	TBD	TBD	TBD	TBD
	11ac@MCS9 NSS1	80	12	TBD	TBD	TBD	TBD	TBD

3.5.2 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	Total(VDDIO+VBAT)_IN=3.3V	
				Max.	Avg.
1	power off*(1)	N/A	N/A	TBD	TBD
2	Transmit	DH5	9.16	TBD	TBD
2	Receive	3DH5	N/A	TBD	TBD

* Current Unit: mA

* The power consumption is based on Azurewave test environment, these data for reference only.

3.6 Frequency Reference

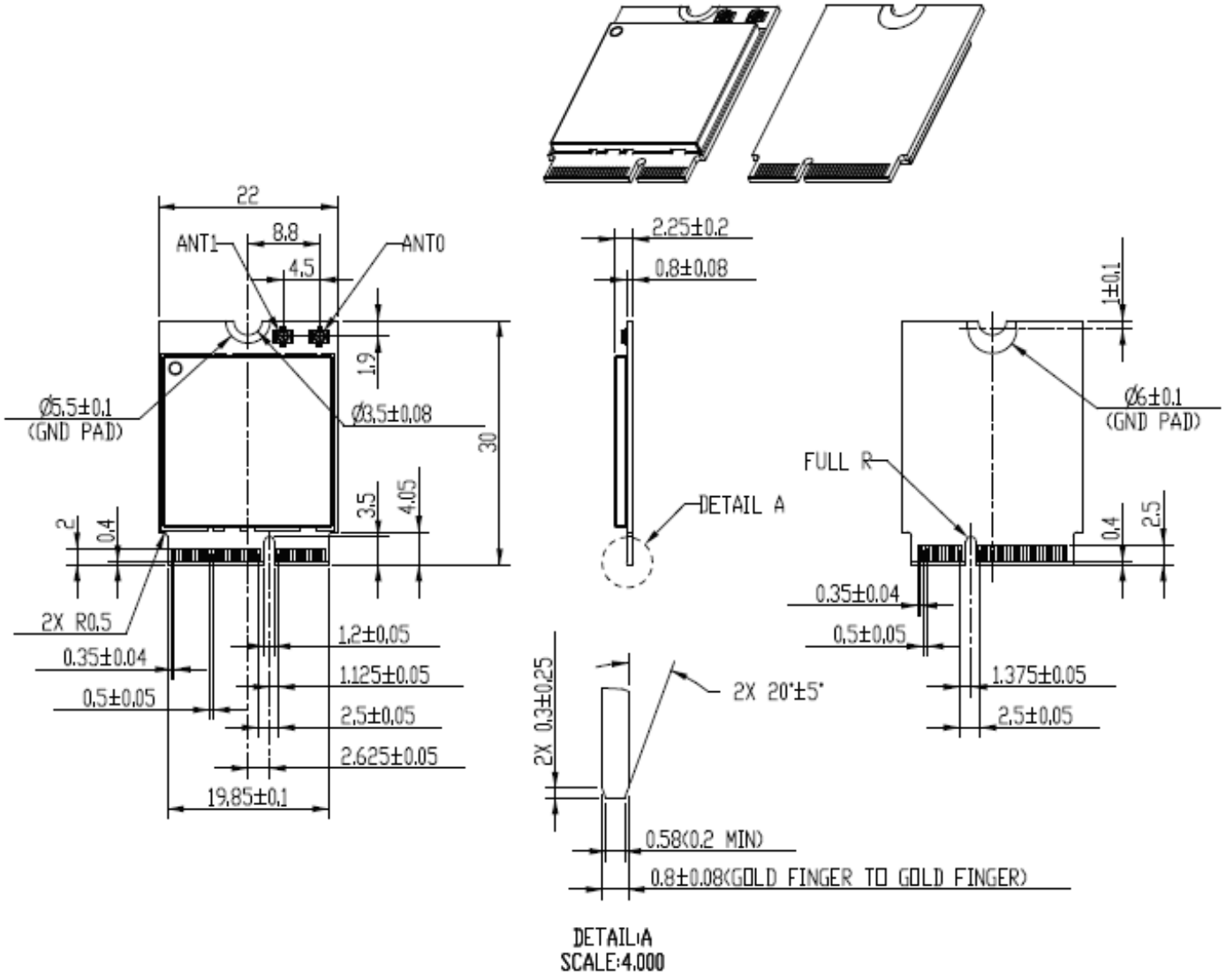
The AW-CB511NF requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed in below table must be used.

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance [5]	> 100k	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10,000	ppm

Note
5. When power is applied or switched off.

4. Mechanical Information

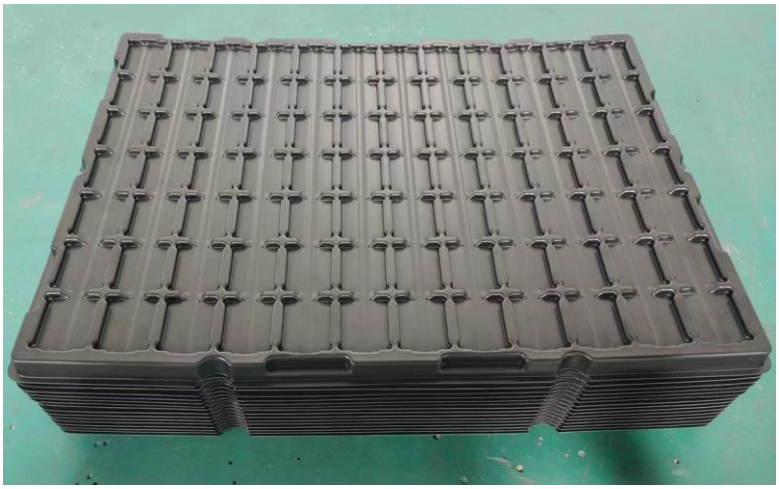
4.1 Mechanical Drawing



5. Packaging Information

1. 84pcs M.2 2230 modules put in one tray

2. The trays are stacked with each other, and add more one tray on the top, so the total number of trays is 14pcs, i.e. 13pcs tray (full) and 1pcs tray (empty)



3. Use P.P Strap to pack 14pcs trays and add one packing label on the top

Example:

4. Put the two packed tray into the box

5. Seal the carton by AzureWave tape

6. One carton label and one box label pasted on the carton. If the carton is not full, add one balance label pasted on the carton

One carton label

One box label

Label Information on the carton

<table>
<tr><td>Example of carton label</td><td>
<table>
<tr><td colspan="2">AzureWave Technologies Inc.</td></tr>
<tr><td>AzureWave P/N</td><td>AW-XXXXX</td></tr>
<tr><td>Customer</td><td>Provided by Sales</td></tr>
<tr><td>Customer P/N</td><td>Provided by Sales</td></tr>
<tr><td>Customer P/O</td><td>Provided by Sales</td></tr>
<tr><td>Description</td><td>AW-XXXXX</td></tr>
<tr><td>Q'ty</td><td>依照实际出货数量</td></tr>
<tr><td>C/N</td><td>依实际情况填写</td></tr>
<tr><td>N.W.</td><td>G.W.</td></tr>
<tr><td colspan="2">RoHS HF Made in China</td></tr>
</table>
</td></tr>
<tr><td>Example of box label</td><td> 
</td></tr>
<tr><td>Example of balance label</td><td> 
</td></tr>
</table>