

# **AW-AM617**

# IEEE 802.11ac MAC/Baseband/Radio with Bluetooth® 5.3 Combo LGA Module

# **Datasheet**

Rev. C

DF

(For Standard)

 1

 FORM NO.: FR2-015\_A
 Responsible Department : WBU
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# Features

#### WLAN

- Full IEEE 802.11ac compatibility with enhanced performance
- Supports MCS8 (256-QAM) for 20 MHz channels
- 20 MHz channels with optional SGI support for MCS0-MCS7
- IEEE 802.11ac explicit beamformer support TX and RX low-density parity check (LDPC) support for improved range and power efficiency
- Receive space-time block coding (STBC)
- On-chip power amplifier/low-noise amplifier for both bands
- Support for front-end modules (FEMS)
- Supports RF front-end architecture with a single dual-band antenna shared between Bluetooth® and WLAN
- Shared Bluetooth<sup>®</sup> and WLAN receive signal path
- Integrated Arm® processor with on-chip RAM and ROM minimizes the need to wake-up the applications processor for standard WLAN functions.

#### Bluetooth

- Complies with Bluetooth® core specification v5.3 with provisions for supporting future specifications
- Bluetooth® 5.3-compliant with 2 Mbps GFSK data rate for Bluetooth® Low Energy
- All optional Bluetooth® 4.2 features supported
- Bluetooth® class 1 or class 2 transmitter operation
- Supports BDR (1Mbps), EDR (2/3Mbps), Bluetooth® LE (1/2Mbps)
- Host controller interface (HCI) using a highspeed UART interface
- PCM for audio data
- Ultra low TX O/P power mode to enable use cases like proximity pairing etc
- Embedded Bluetooth® host stack in ROM
- Low power consumption improves battery life of handheld devices
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Supports multiple simultaneous advanced audio distribution profiles (A2DP) for stereo sound
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.



# **Revision History**

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Α	2023/05/03	DCN029125	First Release	QM.TAN	N.C Chen
В	2023/06/16	DCN029311	<ul> <li>Modify Title</li> <li>Update BT Power Spec.</li> </ul>	QM.TAN	N.C Chen
с	2024/11/13	DCN032749	<ul> <li>Features update</li> <li>Block Diagram update</li> <li>Specifications Table update</li> <li>Pin Table update</li> <li>Power Consumption update</li> </ul>	Barry Tsai	N.C Chen



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#### 1. Introduction

#### 1.1 Product Overview

The AW-AM617 LGA Module integrates a IEEE 802.11ac MAC/baseband/radio and Bluetooth® 5.3 + EDR (enhanced data rate). It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows hand-held device flexibility in size, form, and function. Comprehensive power management circuitry and software ensures, the system can meet the need of high mobile devices that require minimal power consumption and reliable operation.

#### 1.2 Block Diagram



AW-AM617 Block Diagram



# **1.3 Specifications Table**

#### 1.3.1 General

Features	Description		
Product Description	IEEE 802.11 a/b/g/n/ac Wi-Fi + Bluetooth 5.3 Combo LGA Module		
Major Chipset         CYW43022 (106-ball WLBGA)			
Host Interface	WiFi + BT ● SDIO + UART		
Dimension	12.0mm(L) x 12.0mm(W) x 1.75 mm(H)		
Form Factor	LGA module, 47 pins		
Antenna	For LGA, "1T1R, external" ANT1(Main) : WiFi/Bluetooth → TX/RX		
Weight	0.5g		

#### 1.3.2 WLAN

Features	Description
WLAN Standard	IEEE802.11 a/b/g/n/ac 1T1R
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Modulation	802.11a/g/n/ac: OFDM 802.11b: CCK(11, 5.5Mbps), DQPSK(2Mbps), BPSK(1Mbps)
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 802.11g: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13

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	802.11n:						
	USA and Canada – 1 ~ 11						
	Most European Countries – 1 ~ 13						
	802.11a:						
	USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120,						
	124, 128, 132, 136, 140, 149, 153, 157, 161, 165						
	2.4G						
		Min	Тур	Max	Unit		
	11b (11Mbps) @EVM<35%	16	18	20	dBm		
	11g (54Mbps)	13	15	17	dBm		
	@EVIM≦-25 dB						
	11n (HT20 MCS7)	12	15	17	dBm		
	@EVM≦-27 dB	15	15	17	ubili		
(Board Level Limit)*	5G						
		Min	Тур	Max	Unit		
	11a (54Mbps)	11	13	15	dDm		
	@EVM≦-25 dB				UDIII		
	11n (HT20 MCS7)	11	13	15	dDm		
	@EVM≦-27 dB				UDIII		
	11ac (VHT20 MCS8)	0	10	12	alDura		
	@EVM≦-30 dB	8	10		abm		
	2.4G						
		Min	Тур	Max	Unit		
	11b (11Mbps)	-	-89	-86	dBm		
	11g (54Mbps)	-	-77	-74	dBm		
	11n (HT20 MCS7)	-	-77	-74	dBm		
Receiver Sensitivity							
	5G		· _				
		Min	Тур	Max	Unit		
	11a (54Mbps)	-	-75	-72	dBm		
	11n (HT20 MCS7)	-	-75	-72	dBm		
	11ac (VHT20 MCS8)	-	-72	-69	dBm		
	802.11b: 1, 2, 5.5, 11Mb	ops					
Data Rate	802.11a/g: 6, 9, 12, 18,	24, 36, 48,	54Mbps				
	802.11n:MCS0~7						
	802.11ac:MCS0~8						

<sup>&</sup>lt;sup>1</sup> Power setting at typical value, EVM specification will pass with IEEE specification.

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<sup>&</sup>lt;sup>2</sup> Unless otherwise stated, limit values apply for an ambient temperature of +25 °C.



Security	* * *	WEP WPA Personal, WPA2 Personal, WPA3 Personal WMM, WMM-PS (U-APSD), WMM-SA, AES (hardware accelerator) TKIP (hardware accelerator) CKIP (software support)
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\* If you have any certification questions about output power please contact FAE directly.

#### 1.3.3 Bluetooth

Features	Description				
Bluetooth Standard	Bluetooth 5.3 (C	ore Specific	cation)		
Bluetooth VID/PID	N/A				
Frequency Rage	2402MHz~2480	MHz			
Modulation	Header GFSK Payload 2M: 4-DQPSK Payload 3M: 8DPSK				
Output Power	Basic Rate Low Energy	Min 3 3	Тур 6.5 6.5	Max 10 10	Unit dBm dBm
Receiver Sensitivity <sup>3</sup>	BT Sensitivity (B BDR EDR (2DH5) EDR (3DH5)	ER<0.1%) Min	Typ -92 -92 -87	Max -87 -87 -82 -90	Unit dBm dBm dBm dBm

<sup>&</sup>lt;sup>3</sup> Tested by sLNA.



# **1.3.4 Operating Conditions**

Features	Description			
	Operating Conditions			
Voltage	VBAT: 3.2~4.4V VIO : 1.8V			
Operating Temperature	-20°C to +70°C			
Operating Humidity	less than 85% R.H.			
Storage Temperature	-40°C to +125°C			
Storage Humidity	less than 60% R.H.			
ESD Protection				
Human Body Model 1.5KV per MIL-STD-883H Method 3015.8				
Changed Device Model	500V per JEDEC EIA/JESD22-C101E			



# 2. Pin Definition

# 2.1 Pin Map



# AW-AM617 Pin Map (Top View)

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# 2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Туре
1	GND1	Ground.		GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
3	GND2	Ground.		GND
4	NC1	Floating		I/O
5	NC2	Floating		I/O
6	BT_WAKE	BT Device Wake		I
7	BT_HOST_WAKE	BT Host Wake		0
8	CLK REQ	Reference clock request		I/O
9	VBAT	3.3V power pin	3.3V	VCC
10	NC3	Floating		
11	NC4	Floating		0
12	WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW43022 regulators. When this pin is HIGH, the regulators are enabled and the WLAN section is out of reset. When this pin is LOW, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both LOW, the regulators are disabled. This pin has an internal 50 k $\Omega$ pull-down resistor that is auto enabled and disabled when the input is LOW and HIGH, respectively		I
13	WL HOST WAKE	WL Host Wake		0
14	SDIO DATA 2	SDIO Data Line 2		I/O
15	SDIO DATA 3	SDIO Data Line 3		I/O
16	SDIO CMD	SDIO Command Input		I/O
17		SDIO Clock		
18	SDIO DATA 0	SDIO Data Line 0		I/O
19	SDIO_DATA_1	SDIO Data Line 1		I/O
20	GND3	Ground.		GND
21	VIN_LDO_OUT	Internal Buck voltage generation pin		VCC
22	VDDIO	1.8V VDDIO supply for WLAN and BT	1.8V	VCC
23	VIN_LDO	Internal Buck voltage generation pin		VCC
24	LPO	External 32K or RTG clock		
25	PCM_OUT	PCM data out		0
26	PCM_CLK	PCM clock		I/O
27	PCM_IN	PCM data input		I
28	PCM_SYNC	PCM Synchronization control		0
29	NC5	Floating		I/O

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30	GPIO2	GPIO configuration pin	I/O
31	GND4	Ground.	GND
32	NC7	Floating	I/O
33	GND5	Ground.	GND
34	BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW43022 regulators. If BT_REG_ON and WL_REG_ON are LOW, the regulators will be disabled. This pin has an internal 50 k $\Omega$ pull-down resistor that is auto enabled and disabled when the input is LOW and HIGH, respectively.	I
35	NC8	Floating	I/O
36	GND	Ground	GND
37	GPIO6	GPIO configuration pin	I/O
38	GPIO4	SECI_IN	I/O
39	RF_SW_CTRL_5	Programmable RF switch-control lines	I/O
40	GPIO5	SECI_OUT	I/O
41	UART_RTS_N	High-Speed UART RTS	0
42	UART_TXD	High-Speed UART Data Out	0
43	UART_RXD	High-Speed UART Data In	I
44	UART_CTS_N	High-Speed UART CTS	I
45	TP1	Floating	I/O
46	TP2	Floating	I/O
47	GPIO1_P7	GPIO configuration pin	I/O



# 3. Electrical Characteristics

# 3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	-0.5	-	+5.0	V
VIO	DC supply voltage for digital I/O	-0.5	-	2.20	V
VDDIO RF	DC supply voltage for RF switch I/Os	-0.5	-	4.10	V
Tj	Maximum junction temperature	-	-	125	°C
-	Maximum input power for RX input ports <sup>4</sup>	-	-	0	dBm

#### **3.2 Recommended Operating Conditions**

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulator and FEM	3.2	3.6	4.4	V
VDDIO	DC supply voltage for digital I/O	1.62	1.8	1.98	V

#### **3.3 Digital IO Pin DC Characteristics**

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIH	Input high voltage (VDDIO)	0.65 x VDDIO	-	-	V
VIL	Input low voltage (VDDIO)	-	-	0.35 × VDDIO	V
VOH	Output High Voltage @ 2mA	VDDIO – 0.45	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V

<sup>&</sup>lt;sup>4</sup> .Devices incur a maximum of 3 dB reduction in LNA gain with a maximum input level of 0 dBm at a 1.5% duty-cycle derated from a seven year lifetime.

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#### 3.4 Power up Timing Sequence

# 3.4.1 SDIO Host Interface Specification



SDIO Bus Timing (Default Mode)					
Parameter	Symbol	Minimum	Typical	Maximu m	Unit
SDIO CLK (All values are refe	erred to mi	nimum VIH	and maxi	mum VIL)	
Frequency – Data Transfer mode	f <sub>PP</sub>	0	_	25	MHz
Frequency – Identification mode	fod	0	_	400	kHz
Clock low time	t <sub>WL</sub>	10	_	-	ns
Clock high time	twн	10	_	-	ns
Clock rise time	tт∟н	-	_	10	ns
Clock low time	t⊤н∟	-	_	10	ns
Inputs: CMD,	DAT (refe	renced to C	LK)		
Input setup time	tisu	5	_	-	ns
Input hold time	tıн	5	_	-	ns
Outputs: CMD	, DAT (refe	erenced to (	CLK)		
Output delay time – Data Transfer mode	todly	0	_	14	ns
Output delay time – Identification mode	todly	0	_	50	ns
SDIO Bus Timing Parameters (Default Mode)	•	•	•	•	•

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#### SDIO Bus Timing (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit		
SDIO CLK (all values are referred to minimum VIH and maximum VIL							
Frequency – Data Transfer Mode	fрр	0	_	50	MHz		
Frequency – Identification Mode	fod	0	-	400	kHz		
Clock low time	tw∟	7			ns		
Clock high time	twн	7	-	—	ns		
Clock rise time	t⊤∟н	-	-	3	ns		
Clock low time	t⊤н∟	_		3	ns		
Inputs: CMI	D, DAT (rei	fer- enced t	o CLK)				
Input setup Time	tisu	6	_	_	ns		
Input hold Time	tıн	2	-	—	ns		
Outputs: CM	ID, DAT (re	efer- enced	to CLK)				
Output delay time – Data Transfer Mode	todly	_	_	14	ns		
Output hold time	toн	2.5	_	_	ns		
Total system capacitance (each line)	CL	_	_	40	pF		

SDIO Bus Timing a Parameters (High-Speed Mode)



#### 3.4.2 UART Interface

The BT HCI UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 4.0 Mbps.

The interface features an automatic baud rate detection capability that returns a baud rate selection. The baud rate may be changed using a vendor-specific UART HCI command.

The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth UART HCI H4 specification. The default baud rate is 115.2 Kbaud.

The AW-AM617 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP).

It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The AW-AM617 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 2\%$ .

Pin Number	Signal Name	Description	Туре
42	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	0
43	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	Ι
41	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	I
44	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to- send signal for the HCI UART interface.	0

**UART** Interface Signals

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#### **UART** Timing

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	-	_	0.5	Bit periods

**UART Timing Specifications** 



#### 3.4.3 Sequencing of Reset and Regulator Control Signals

The AW-AM617 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

#### **Description of Control Signals**

**WL\_REG\_ON**: Used by the PMU to power-up the WLAN section. It is also OR-gated with the BT\_REG\_ON input to control the internal AW-AM617 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT\_REG\_ON and WL\_REG\_ON pins are low, the regulators are disabled.

**BT\_REG\_ON**: Used by the PMU (OR-gated with WL REG ON) to power-up the internal AW-AM617 regulators. If both the BT\_REG\_ON and WL\_REG\_ON pins are low, the regulators are disabled. When this pin is low and WL\_REG\_ON is high, the BT section is in reset.

Note: The AW-AM617 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating Host SDIO, UART or SPI accesses.

Note: VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

#### Power-Up/Power-Down/Reset Circuits

The AW-AM617 has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption.



Signal	Description				
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power-up the WLAN section. It is also OR-gated with the BT EG ON input to control the internal AW-AM617 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 50 k $\Omega$ pull-down resistor that is auto enabled and disabled when the input is low and high, respectively				
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal AW-AM617 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 50 kΩ pull-down resistor that is auto enabled and disabled when the input is low and high, respectively.				

#### Power-Up/Power-Down/Reset Control Signals



WLAN = ON, Bluetooth = ON



32.678 kHz Sleep Clock	
VBAT⁺	<u>د</u>
VDDIC	
WL_REG_ON	
BT_REG_ON	
	*Notes: 1. VBAT should not rise 10%–90% faster than 40 microseconds. 2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high .

#### WLAN = OFF, Bluetooth = OFF



WLAN = ON, Bluetooth = OFF





WLAN = OFF, Bluetooth = ON



#### 3.5 Power Consumption\*

#### 3.5.1 WLAN

No	Itom			VBAT=3.6 V (mA)			
NO.		em		Max.	Avg.		
1	OFF *			0.010	0.002		
2	Deepsleep*			0.010	0.003		
3	Power Save 2.4GHz (D	)TIM-1)*		22	0.23		
4	Power Save 2.4GHz (D	)TIM-3)*		24	0.12		
5	Power Save 5GHz (DT	IM-1)*		24	0.15		
6	Power Save 5GHz (DT	IM-3)*		24	0.10		
Band	Mada	BW	<b>RF Power</b>	Transm	nit		
(GHz)	wode	(MHz)	(dBm)	Max.	Avg.		
	11b@1Mbps	20	18	183	139		
2.4	11g@54Mbps	20	15	236	205		
	11n@MCS7	20	15	186	167		
	11a@54Mbps	20	13	269	235		
5	11n@MCS7	20	13	278	235		
	11ac@MCS8 NSS1	20	10	251	219		
Band	Mada					Receiv	/e
(GHz)	Mode	DVV	(11172)	Max.	Avg.		
2.4	11b@1Mbps		20	20	18		
2.4	11n@MCS7		20	19	18		
Б	11a@54Mbps		20	21	20		
Э	11ac@MCS8 NSS1		20	21	20		

\* The power consumption is based on Azurewave test environment, these data for reference only.

No	Item		VDDIO=1.8 V(uA)			
NO.	nem			Max.	Avg.	
1	WLAN OFF *			0.269	)	
2	Sleep *			212	125	
3	Power Save DTIM1 (2.4GHz) *			5873	118	
Band	Mada	BW RF Power		Transmit		
(GHz)	wode	(MHz)	(MHz) (dBm)	Max.	Avg.	
2.4	11b@1Mbps	20	18	2411	2406	
Band	Modo	BW(MHz)		Receiv	/e	
(GHz)	wode			Max.	Avg.	
2.4	11b@1Mbps		20	449	439	

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#### 3.5.2 Bluetooth

No.	Mode	Packet Type	RF Power	VBAT=3.6V (mA)		
		i denot i jpo	(dBm)	Max.	Avg.	
1	Sleep	Ν	I/A	0.021	0.003	
2	Transmit *	DH5/3DH5	6.5	27	25	
3	Receive *	DH5/3DH5	N/A	11	9	
No	Mode	Packet Type	RF Power	VDDIO=1.8V (uA)		
110.	mode	I denet Type	(dBm)	Max.	Avg.	
1	Sleep	N	J/A	46	27	
2	Transmit *	DH5/3DH5	6.5	200	186	
3	Receive *	DH5/3DH5	N/A	179	164	

\* The power consumption is based on Azurewave test environment, these data for reference only.



#### 3.6 Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

#### External 32.768KHz Low-Power Oscillator

The AW-AM617 uses a secondary low frequency clock for low-power-mode timing. Either the internal low- precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz  $\pm$  30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake-up earlier to avoid missing beacons. Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in below.

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30–70	%
Input signal amplitude	500–1800	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance <sup>a</sup>	>100k	Ω

External 32.768 kHz Sleep Clock Specifications



# 4. Mechanical Information

4.1 Mechanical Drawing



#### TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.1mm

Unit:mm



# 5. Packaging Information

- 1. One reel = 1,500pcs 12\*12 LGA module. (一卷數量為 1500pcs.)
- One production label is pasted on the reel.
   One desiccant & one humidity indicator card are put on the reel.

(卷軸貼上一張生產標籤,同時放上一包防潮包及濕度指示卡.)



3.One reel is put into the anti-static moisture barrier bag with one production label on the bag. (卷軸放進入防靜電鋁袋,再貼上生產標籤.)



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4. The anti-static reel is put into the pink bubble wrap.

(防靜電鋁箔袋放進氣泡袋.)

Then put into the inner box with one production label pasted on the box.

(氣泡袋放進內箱中,再貼上一張生產標籤.)



5. One outer box contained <u>5 inner boxes</u>.

(一個外箱可放五個內箱盒.)



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6. Sealing the carton with Azurewave logo tape. (使用海華 Logo 膠帶將外箱進行工字型封箱)



7. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label will be pasted on the carton (外箱上貼附出貨標籤和箱號標籤;如不滿箱‧需貼附尾數標籤)

