AzureWave Technologies, Inc.

AW-CU362

Bluetooth 5.0 LE Stamp Module
BLE + Cortex M0 + Flash + Antenna

Datasheet

Rev. B

DF

For Standard

Features

DA14585(DialogDA14585 is a Bluetooth Low Energy 5.0 SoC)

Processor

- ARM Cortex-M0, 32bit, 16MHz
- Dedicated Link Layer Processor
- AES-128 bit encryption Processor

Memory

- 64 KB OTP Memory
- 28 KB ROM
- 96 KB Retention SRAM

Flash

- 1M Bit SPI Flash (up to 256M Bit)

Wireless

- Bluetooth V5.0

Antenna

- Embedded Antenna

IO Interfaces

- UART x 2
- SWD x 1
- GPIO x 15
- SPI x 1
- I2C x 1
- ADC x 2
- Quadrature Decoder

Power input

- Single 3.3V Power Input

Package

- Stamp Module 19.6 mm x 15 mm x 2.45 mm

Application

- Support up to 8 Bluetooth LE connections
- Voice-controlled remote controls
- Beacons
- (Multi-sensor) Wearable devices
- Fitness trackers
- Consumer health
- Smartwatches
- Human interface devices
- Keyboard
- Mouse
- Toys
- Consumer appliances

Certifications

- FCC/CE

Revision History

Document NO: R2-2362-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2019/09/27	DCN016564	● Update Receiver Sensitivity	Morris Huang	N.C. Chen
B	2020/05/27	DCN021522	● Update New format	Morris Huang	N.C. Chen

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1. Introduction

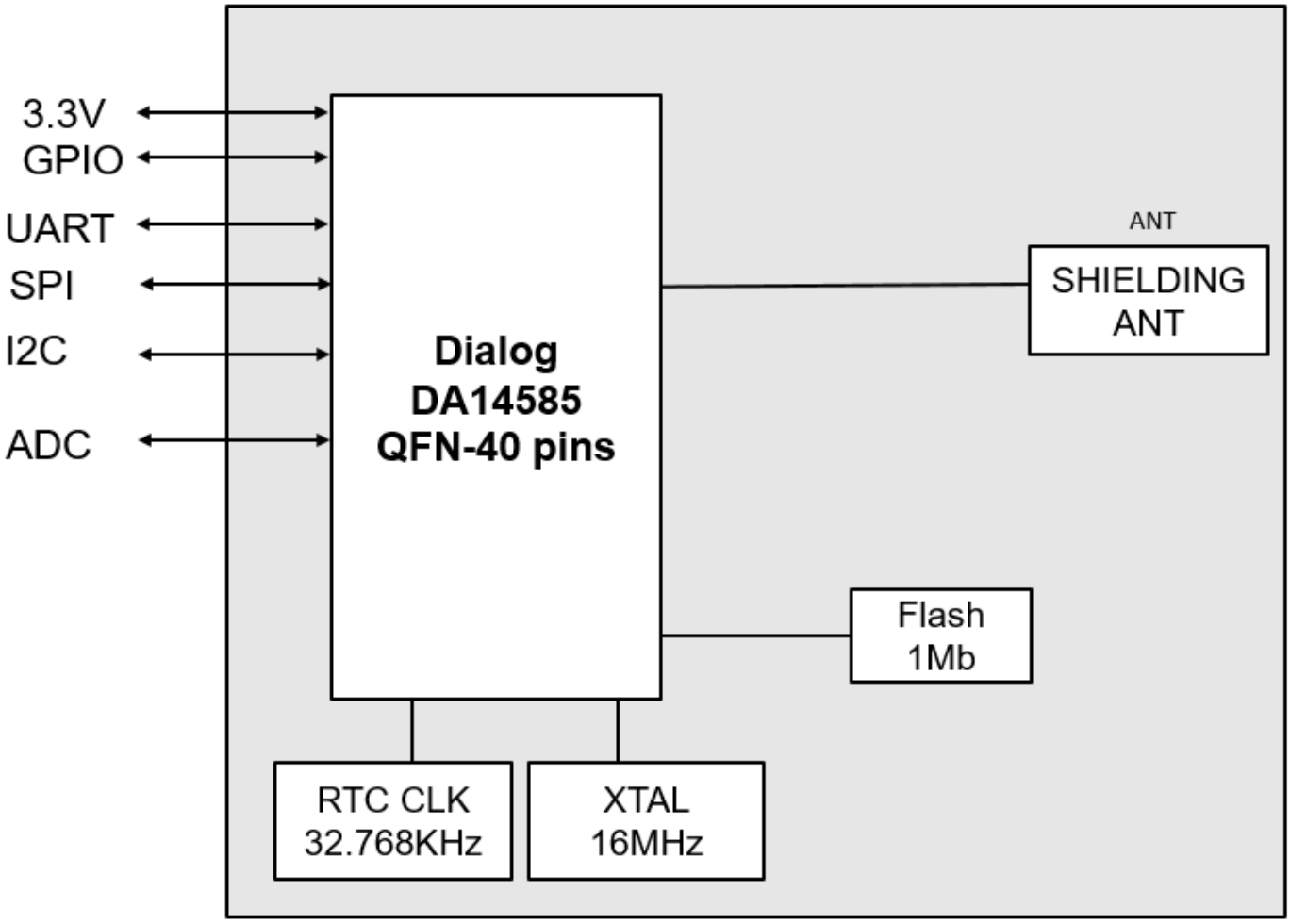
1.1 Product Overview

AzureWave presents **AW-CU362** the advanced Stamp *Bluetooth® Low Energy 5.0* **module** provides a highly cost-effective, flexible and easy to-use hardware/software device to build a new generation of connected, smart devices. These smart-connected devices enable device to deliver a broad-range of services to consumers including energy-management, demand-response, home automation and remote access. This allows a user to manage comfort and convenience, also run diagnostics and receive alerts and notifications, in addition to managing and controlling the device. Developers can leverage the rich connectivity features of these new smart devices to create a new generation of innovative new applications and services

The device builds upon the success of Dialog's Bluetooth microcontroller device using the Dialog DA14585 and software. Adding new enhancements and capabilities.

The **AW-CU362** is powered by production quality, field-tested Dialog software that includes a rich set of software components that work together to support the development of Smart devices, and enable these devices to connect to mobile clients such as smart-phones, Internet-based Cloud and Smart-Grid services. The feature-rich software stack enables OEMs to focus on application-specific software functionality, thus enabling rapid development and reduced software development costs and risks.

1.2 Block Diagram



Block Diagram of AW-CU362

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	AW-CU362 Bluetooth® Low Energy 5.0 Stamp Module
Major Chipset	Dialog DA14585 (QFN 40p)
Host Interface	UART / SPI / I2C / GPIO / ADC /QD_channel
Dimension	19.6 mm x 15 mm x 2.45 mm
Form factor	Stamp LGA module, 30-pin
Antenna	Shielding Antenna ANT : Bluetooth → Tx/Rx
Weight	1g

1.3.2 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth V5.0 complaint
Frequency Rage	2402~2480MHz
Modulation	LE GFSK
Output Power (Board Level Limit)*	

	Min	Typ	Max	Unit
BLE	-5	-	1	dBm

Receiver Sensitivity	1 Mbps,PER = 30.8 %;Dirty Transmitter: off TA= 25 °C			
	Min	Typ	Max	Unit
BLE		-93	-90	dBm
Data Rate	Bluetooth® Low Energy 5.0 1 Mbit/s			
Range	TBD			

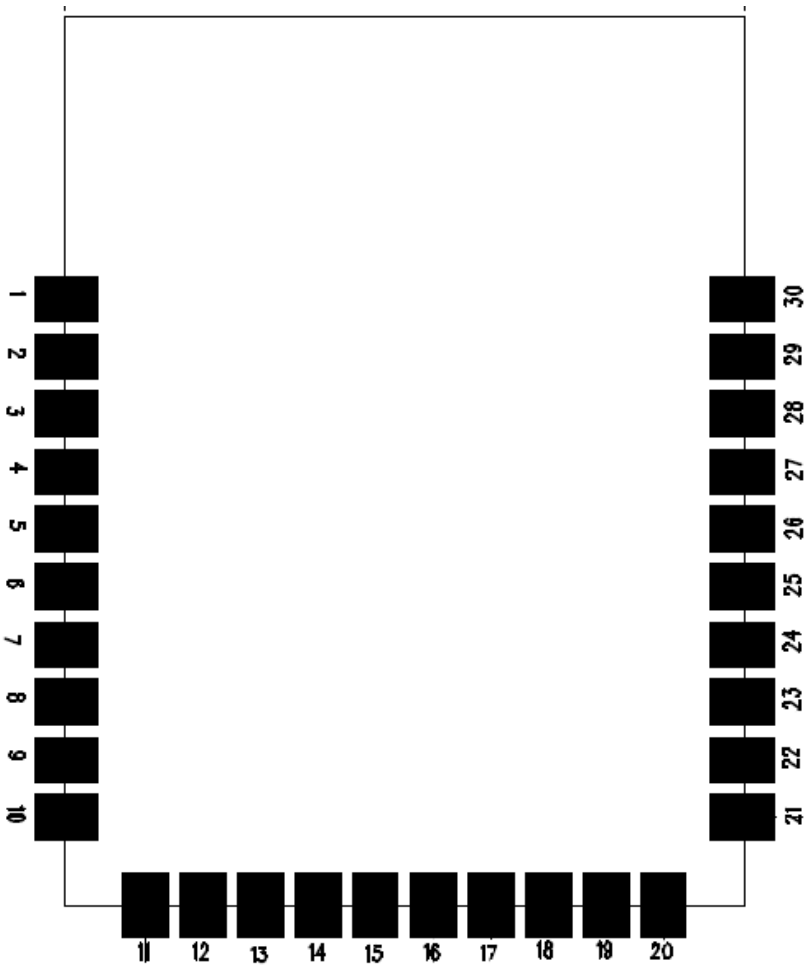
* If you have any certification questions about output power please contact FAE directly.

1.3.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V +/- 8%
Operating Temperature	-30℃ ~ 85℃
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40℃ ~ 85℃
Storage Humidity	Less than 60% R.H.
ESD Protection	
Human Body Model	2KV per JEDEC EID/JESD22-A114
Changed Device Model	500V per JEDEC EIA/JESD22-C101

2. Pin Definition

2.1 Pin Map



AW-CU632 Pin Map (Top View)

2.2 Pin Table

2.2.1 Power

Pin No	Definition	Basic Description	Type	Level
15	VBAT_3V	3.3V Power input	PWR	3.3V
4	VPP	Leave VPP floating		

2.2.2 Reset and SWD

Pin No	Definition	Basic Description	Type	Level
24	SWDIO	JTAG Data input/output.	I/O	3.3V
25	SWCLK	JTAG clock signal input.	I/O	3.3V
17	RST	Reset signal (active high). Must be connected to GND if not used.	I	3.3V (internal pull low 2.2k ohm)

2.2.3 GPIO

Pin No	Definition	Flash writing	Function 1	Type	Level
3	P2_8		GPIO/UART/I2C/SPI*/QD_channel	I/O	3.3V
5	P2_9			I/O	3.3V
6	P2_0			I/O	3.3V
7	P0_1		GPIO/UART/I2C/SPI*/QD_channel /ADC[1]	I/O	3.3V
8	P0_2		GPIO/UART/I2C/SPI*/QD_channel /ADC[2]	I/O	3.3V
9	P0_4	UART(TX)	GPIO/UART/I2C/ SPI*/QD_channel	I/O	3.3V
10	P0_5	UART(RX)	N/A	I/O	3.3V
11	P2_1		GPIO/UART/I2C/SPI*/QD_channel	I/O	3.3V
12	P0_7			I/O	3.3V
14	P2_2			I/O	3.3V
18	P2_3			I/O	3.3V
19	P2_4			I/O	3.3V
22	P1_0			I/O	3.3V
23	P1_1			I/O	3.3V
28	P2_5			I/O	3.3V
29	P2_6			I/O	3.3V

2.2.4 GND

Pin No	Definition	Basic Description	Type	Level
1	GND			
2				
13				
16				
20				
21				
26				
27				
30				

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT_3V	3.3V power supply		3.3	3.6	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT_3V	3.3V power supply	3.0	3.3	3.6	V

3.3 Reset Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIH	Input High Voltage	0.84			V
VIL	Input Low Voltage			0.36	V

3.4 General Purpose ADC Characteristics

3.4.1 General Purpose ADC - Recommended Operating Condition

Symbol	Parameter		Minimum	Typical	Maximum	Unit
NBIT(ADC)	number of bits (resolution)			10		bit

3.4.2 General Purpose ADC - DC Characteristics

Symbol	Parameter		Minimum	Typical	Maximum	Unit
VI(ZS)	zero-scale input voltage	single-ended, calibrated at zero input	-2.5	0	2.5	mV
VI(FS)	full-scale input voltage	single-ended, calibrated at zero input	1150	1180	1250	mV
VI(FSN)	negative full-scale input voltage	differential, calibrated at zero input		-1180		mV
VI(FSP)	positive full-scale input voltage	differential, calibrated at zero input		1180		mV
INL	integral non-linearity		-2		2	LSB
DNL	differential non-linearity		-2		2	LSB

3.4.3 General Purpose ADC - Timing Characteristics

Symbol	Parameter		Minimum	Typical	Maximum	Unit
NBIT(ADC)	number of bits (resolution)			10		bit

3.5. I2C Protocols

The I2C Controller has the following protocols:

- START and STOP Conditions
- Addressing Slave Protocol
- Transmitting and Receiving Protocol
- START BYTE Transfer Protocol

3.5.1 START and STOP Conditions

When the bus is idle, both the SCL and SDA signals are pulled high through external pull-up resistors on the bus. When the master wants to start a transmission on the bus, the master issues a START condition. This is defined to be a high-to-low transition of the SDA signal while SCL is 1. When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the SDA line while SCL is 1. Below figure shows the timing of the START and STOP conditions. When data is being transmitted on the bus, the SDA line must be stable when SCL is 1.

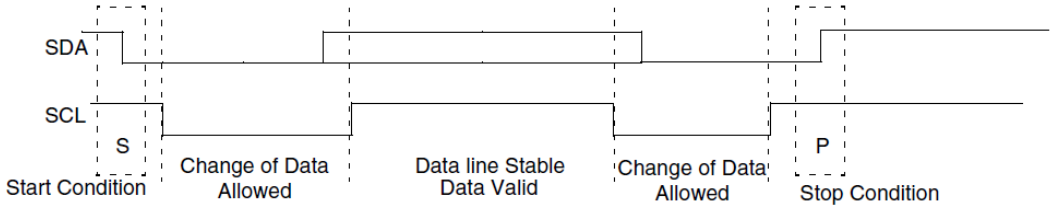


Figure. Start and Stop conditions

Note: The signal transitions for the START/STOP conditions, as depicted in above figure, reflect those observed at the output signals of the Master driving the I2C bus. Care should be taken when observing the SDA/SCL signals at the input signals of the Slave(s), because unequal line delays may result in an incorrect SDA/SCL timing relationship.

3.6. UART interface

The AW-CU362(DA14585) contains two identical instances of this block, i.e. UART and UART2.

The UART is compliant to the industry-standard 16550 and is used for serial communication with a peripheral. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

There is also DMA support on the UART block thus the internal FIFOs can be used. Both UARTs support hardware flow control signals (RTS, CTS).

Features

- 16 bytes Transmit and receive FIFOs

● Hardware flow control support (CTS/RTS)

● Shadow registers to reduce software overhead and also include a software programmable reset

● Transmitter Holding Register Empty (THRE) interrupt mode

● IrDA 1.0 SIR mode supporting low power mode.

● Functionality based on the 16550 industry standard:

● Programmable character properties, such as number of data bits per character (5-8), optional

● parity bit (with odd or even select) and number of stop bits (1, 1.5 or 2)

● Line break generation and detection

● Prioritized interrupt identification

● Programmable serial data baud rate as calculated by the following: baud rate = (serial clock frequency)/(16 * divisor).

3.7. SPI+ interface

This interface supports a subset of the Serial Peripheral Interface (SPI™). The serial interface can transmit and receive 8, 16 or 32 bits in master/slave mode and transmit 9 bits in master mode. The SPI+ interface has enhanced functionality with bidirectional 2x16-bit word FIFOs.

SPI is a trademark of Motorola, Inc.

Features

● Slave and Master mode

● 8 bit, 9 bit, 16 bit or 32 bit operation

● Clock speeds up to 16 MHz for the SPI controller. Programmable output frequencies of SPI source clock divided by 1, 2, 4, 8

● SPI clock line speed up to 8 MHz

● SPI mode 0, 1, 2, 3 support (clock edge and phase)

● Programmable SPI_DO idle level

● Maskable Interrupt generation

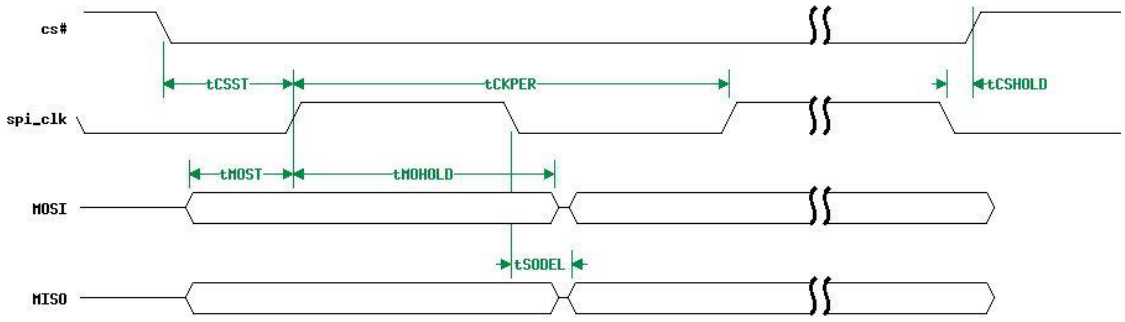
● Bus load reduction by unidirectional writes-only and reads-only modes.

● Built-in RX/TX FIFOs for continuous SPI bursts.

● DMA support

3.7.1 SPI Timing

The timing of the SPI interface when the SPI controller is in Slave mode is presented in below figure.



Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{CKPER}	spi_clk clock period			0.25 * T_{SPI_CLK}	ns
t_{CSST}	CS active time before rising edge of spi_clk	10.6 +T_{INT}	5.2 + T_{INT}	3.1 + T_{INT}	ns
t_{CSHOLD}	CS active time after falling edge of spi_clk	0	0	0	ns
t_{MOST}	Input data latching setup time	2.7	1.5	0.9	ns
t_{MOHOLD}	Input data hold time	0	0	0	ns
t_{SODEL}	Output data hold time	17.2	8.6	5.5	ns

Note TINT represents the internal SPI clock period and is equal to 1.5 * spi_clk period.

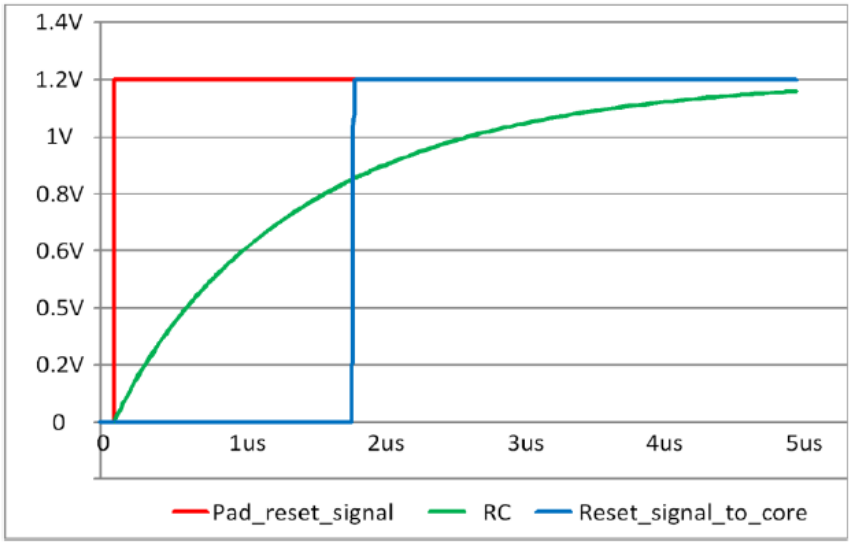
3.8 Power up Sequence/Rest Timing

3.8.1 Power up sequence

3.8.2 Reset timing

The AW-CU362 comprises an RST pad which is active high. It contains an RC filter for spikes suppression with 400 kΩ and 2.8 pF for the resistor and the capacitor respectively. It also contains a 25 kΩ pull-down resistor.

The response is illustrated in the below figure which displays the voltage (V) on the vertical axis and the time (μs) on the horizontal axis: The typical latency of the RST pad is in the range of 2 μs.



3.9 Power Consumption*

3.9.1 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	Voltage=3.3V	
				Max.	Avg.
1.	TX	LE	-0.72dBm	3.67mA	3.66mA
2.	RX	LE	n/a	5.13mA	5.13mA

Current Unit: mA

* The power consumption is based on Azurewave test environment, these data for reference only.

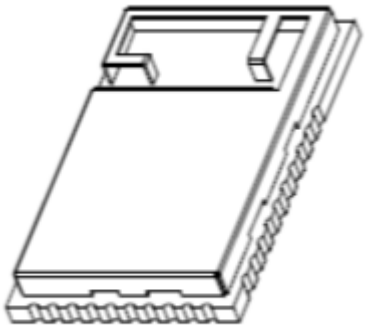
3.10 Certifications FCC Bluetooth 2.4GHz Power Table

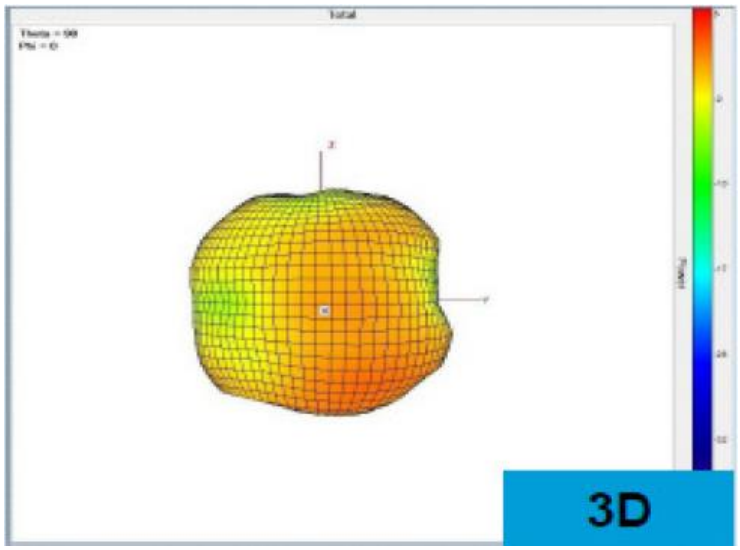
FCC Bluetooth 2.4GHz Power Table:

Embedded Antenna (3.78dBi)

Modulation	Channel	Meter Power	Meter Power
		(Average,dBm)	(Average,dBm)
802.15.1 (BT5.0)	0(2402MHz)	0.600	0.670
	19(2440MHz)	0.405	0.510
	39(2480MHz)	0.230	0.280

Shielding Antenna Spec

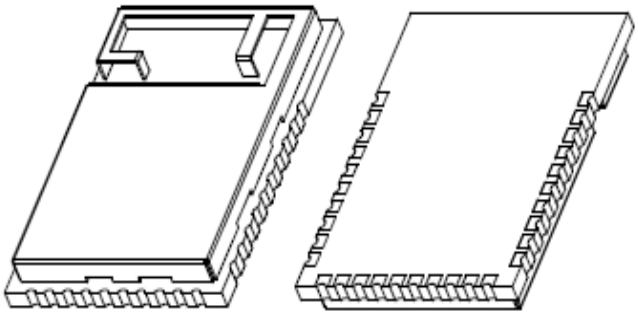


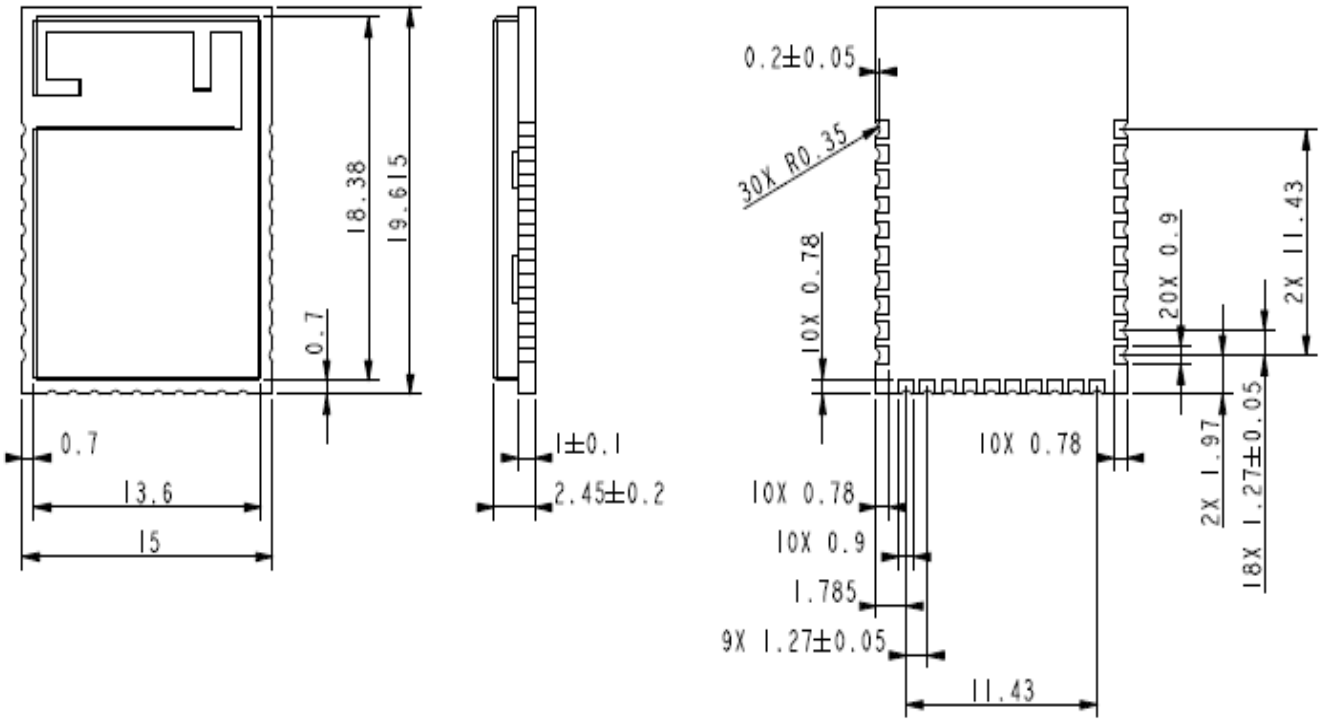


Ant			
Frequency(MHz)	2400	2450	2500
Efficiency (dB)	-1.43	-1.36	-1.44
Peak Gain (dBi)	2.13	2.3	2.11
Efficiency (%)	71.96	73.1	71.82

4. Mechanical Information

4.1 Mechanical Drawing



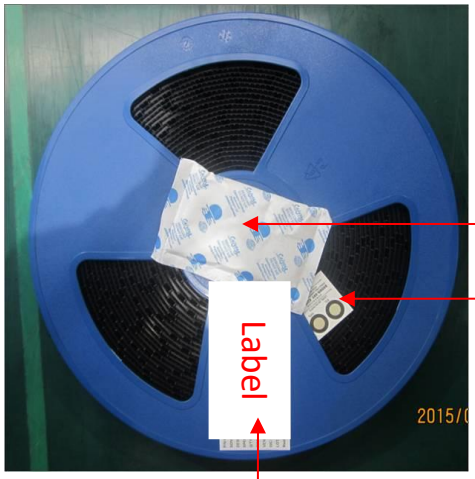


5. Packaging Information

Tape reel = 1 Box = 700 pcs

Carton = 3 Boxes = 2,100 pcs

5.1 Tape & Reel Picture

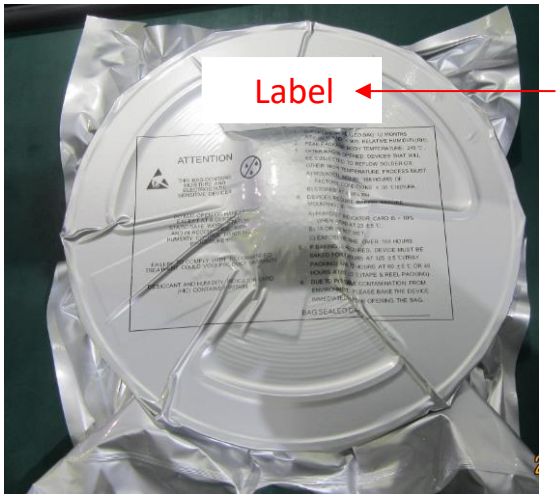


DESICCANT

HUMIDITY INDICATOR CARD

AFFIX PACKING LABEL

5.2 Packing Picture



AFFIX PACKING LABEL

5.3 Inside of Inner Box Picture

5.4 Inner Box Picture

5.5 Inside of Carton Picture

1 Carton = 3 Boxes

5.6 Carton and Label Picture

AFFIX SHIPPING LABEL

AFFIX PACKING LABEL

AFFIX BOX LABEL