# AW-NM432SM

## IEEE 802.11 b/g/n Wireless LAN Stamp Module

## Datasheet

**Rev. A**

**DF**

**(For Standard)**

# Features

## WLAN

- Integrates Cypress solutions of CYW43364 WiFi SoC
- SDIO v2.0 interfaces support for WLAN
- Lead-free Design
- 12.0mm(L) x 12.0mm(W) x 1.5 mm(H) 47 pin LGA package
- With Crystal(XTAL)
- Single band 2.4 GHz 802.11 b/g/n
- WLAN host interface options
- SDIO v2.0, including DS and HS modes
- Security–WEP, WPA/WPA2 (personal), AES (HW), TKIP (HW), CKIP (SW), WMM/WMM-PS/WMM-SA

# Revision History

Document NO: R2-2432SM-DST-01

| Version | Revision Date | DCN NO. | Description | Initials | Approved |
|---|---|---|---|---|---|
| Version 0.1 | 2019/02/15 | | ● Initial Version | Sonia Yang | Chihhao Liao |
| Version 0.2 | 2019/05/06 | | ● Specifications Table update | JM.Pang | Chihhao Liao |
| A | 2019/11/21 | DCN016358 | ● Format Update | JM.Pang | Chihhao Liao |
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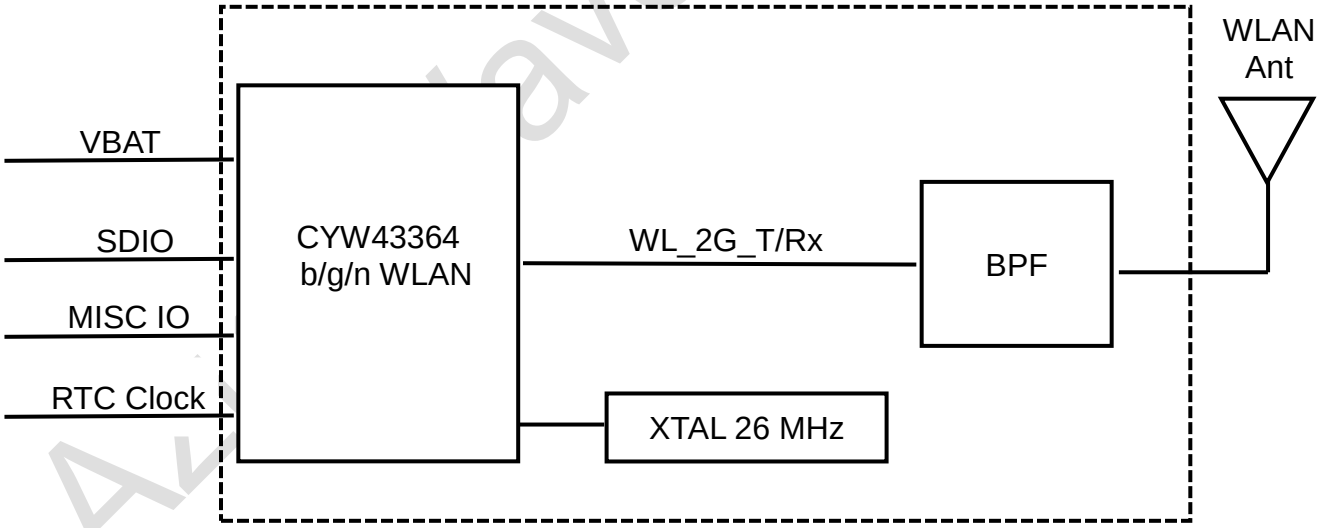
# 1. Introduction

## 1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced IEEE 802.11 b/g/n WLAN module - AW-NM432SM. The module is targeted to mobile and embedded devices which need small footprint package, low power consumption, and multiple OS support. The module supports 2.4GHz IEEE 802.11b/g/n MAC/baseband/radio functionality. In addition, it also features an integrated Power Management Unit (PMU), Power Amplifiers (PAs), and a Low Noise Amplifier (LNA) to address the needs of mobile devices that require minimal power consumption and compact size. By using AW-NM432SM, the customers can easily enable the Wi-Fi embedded applications with the benefits of high design flexibility, short development cycle, and quick time-to-market. Specified in the IEEE 802.11 standard minimize the system power requirements by using AW-NM43SM. In addition to the support of WPA/WPA2 (personal) and WEP encryption, the AW-NM432SM also supports the IEEE 802.11i security standard through AES and TKIP acceleration hardware for faster data encryption. For the video, voice and multimedia applications the AW-NM432SM support 802.11e Quality of Service (QoS). The host interface is SDIO v2.0 interface.

## 1.2 Block Diagram

A simplified block diagram of the AW-NM432SM module is depicted in the figure below.



## 1.3 Specifications Table

### 1.3.1 General

| Features | Description |
|---|---|
| Product Description | IEEE 802.11 b/g/n Wireless LAN Stamp Module |
| Major Chipset | Cypress CYW43364 |
| Host Interface | WLAN: SDIO v2.0 |
| Dimension | 12.0mm(L) x 12.0mm(W) x 1.5 mm(H) |
| Package | 47 pin Stamp Module |
| Antenna | 2.4G Ant: WiFi |
| Weight | TBD |

### 1.3.2 WLAN

| Features | Description |
|---|---|
| WLAN Standard | IEEE 802.11 b/g/n, Wi-Fi compliant |
| WLAN VID/PID | N/A |
| WLAN SVID/SPID | N/A |
| Frequency Rage | WLAN: 2.4 GHz |
| Modulation | DSSS, OFDM, BPSK(9/6Mbps), QPSK(18/12Mbps), DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps), 16-QAM(36/24Mbps), 64-QAM (72.2/54/48Mbps) |
| Number of Channels | 802.11b:<br>USA, Canada and Taiwan – 1 ~ 11<br>Most European Countries – 1 ~ 13<br>Japan – 1 ~ 14<br>802.11g:<br>USA and Canada – 1 ~ 11<br>Most European Countries – 1 ~ 13<br>802.11n:<br>USA and Canada – 1 ~ 11<br>Most European Countries – 1 ~ 13 |
| Output Power**<br>(Board Level Limit)* | **2.4G** |

| | | | | | |
|---|---|---|---|---|---|
| | | Min | Typ | Max | Unit |
| | 11b (11Mbps) @EVM<35% | 16 | 18 | 20 | dBm |
| | 11g (54Mbps) @EVM≦-25 dB | 14 | 16 | 18 | dBm |
| | 11n (HT20 MCS7) @EVM≦-28 dB | 13 | 15 | 17 | dBm |

| | | | | | |
|---|---|---|---|---|---|
| Receiver Sensitivity | **2.4G** | | | | |
| | | Min | Typ | Max | Unit |
| | 11b (11Mbps) | | -89 | -86 | dBm |
| | 11g (54Mbps) | | -75 | -71 | dBm |
| | 11n (HT20 MCS7) | | -73 | -69 | dBm |

| | |
|---|---|
| Data Rate | 802.11b: 1, 2, 5.5, 11Mbps<br>802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps<br>802.11n:MCS 0~7 HT20 |
| Security | ◆ WPA™- and WPA2™- (Personal) support for powerful encryption and authentication<br>◆ AES in WLAN hardware for faster data encryption and IEEE802.11i compatibility<br>◆ Cisco Compatible Extensions(CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)<br>◆ Wi-Fi Protected Setup (WPS) |

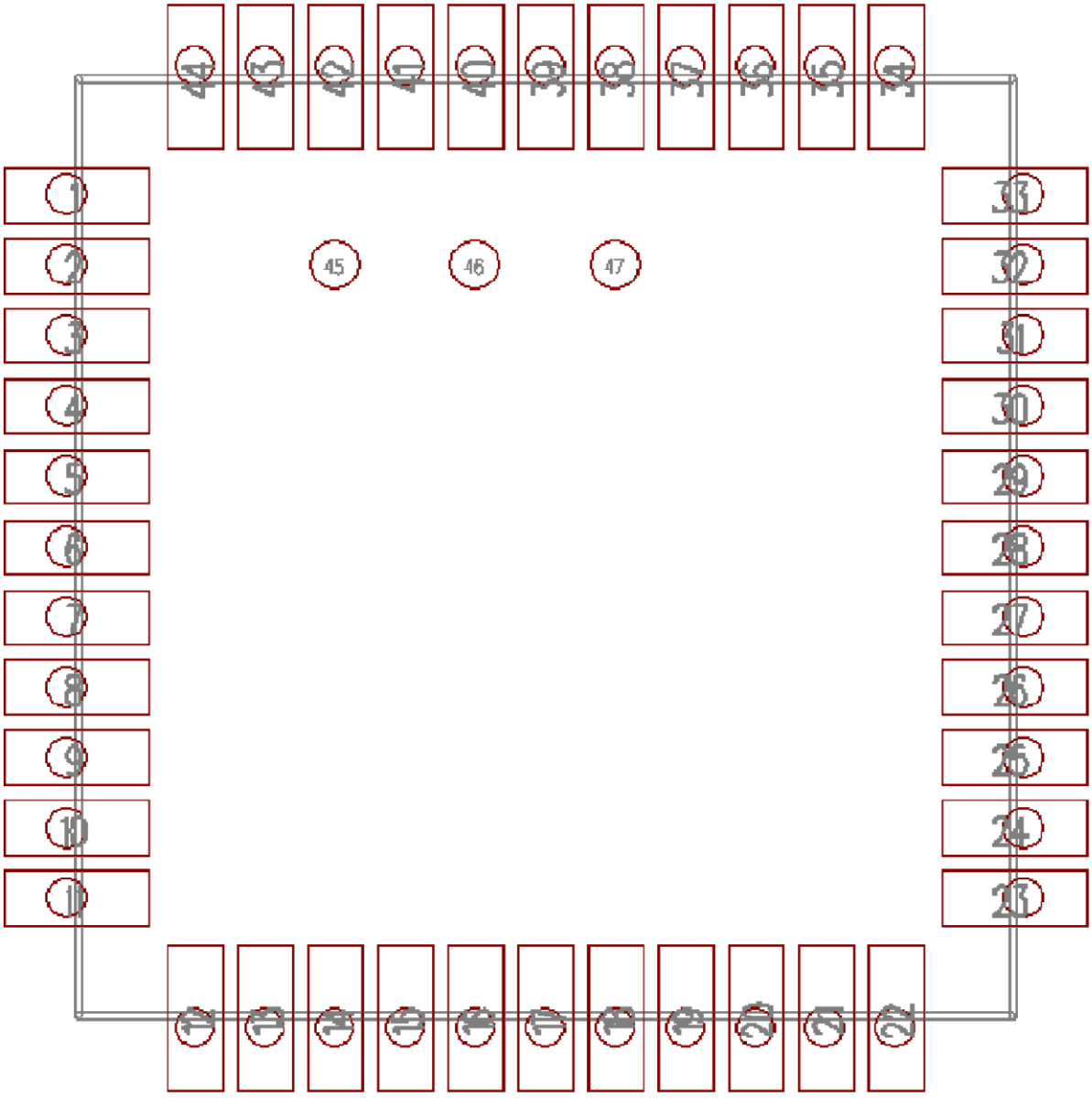
*** If you have any certification questions about output power please contact FAE directly.1.3.3 Operating Conditions**

| Features | Description |
|---|---|
| Operating Conditions | |
| Voltage | Input supply for host I/O : 3.3V |
| Operating Temperature | -30~70 ºC (Optimal RF performance guarantee -10~55 ºC) |
| Operating Humidity | Less than 85%R.H. |
| Storage Temperature | -40~85 ºC |
| Storage Humidity | Less than 60%R.H. |
| ESD Protection | |
| Human Body Model | 1.25KV |
| Changed Device Model | 300V |

# 2. Pin Definition

## 2.1 Pin Map

**AW-NM432SM Top View Pin Map**



## 2.2 Pin Table

| Pin No | Definition | Basic Description | Voltage | Type |
|---|---|---|---|---|
| 1 | GND | Ground. | | GND |
| 2 | WL_BT_ANT | WLAN/BT RF TX/RX path. | | RF |
| 3 | GND | Ground. | | GND |
| 4 | NC | Floating Pin, No connect to anything | | Floating |
| 5 | NC | Floating Pin, No connect to anything | | Floating |
| 6 | NC | Floating Pin, No connect to anything | | Floating |
| 7 | NC | Floating Pin, No connect to anything | | Floating |
| 8 | NC | Floating Pin, No connect to anything | | Floating |
| 9 | VBAT | 3.3V power pin | 3.3V | VCC |
| 10 | NC | Floating Pin, No connect to anything. | | Floating |
| 11 | NC | Floating Pin, No connect to anything. | | Floating |
| 12 | WL_REG_ON | Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming. | VDDIO | I |
| 13 | WL_HOST_WAKE | WL Host Wake | VDDIO | O |
| 14 | SDIO_DATA2 | SDIO Data Line 2 | VDDIO | I/O |
| 15 | SDIO_DATA3 | SDIO Data Line 3 | VDDIO | I/O |
| 16 | SDIO_DATA_CMD | SDIO Command Input | VDDIO | I/O |
| 17 | SDIO_DATA_CLK | SDIO Clock Input | VDDIO | I |
| 18 | SDIO_DATA0 | SDIO Data Line 0 | VDDIO | I/O |
| 19 | SDIO_DATA1 | SDIO Data Line 1 | VDDIO | I/O |
| 20 | GND | Ground. | | GND |
| 21 | VIN_LDO_OUT | Internal Buck 1.2V voltage generation pin | 1.4V | O |
| 22 | VDDIO | 1.8V-3.3V VDDIO supply for WLAN and BT | VDDIO | VCC |
| 23 | VIN_LDO | Internal Buck 1.2V voltage generation pin | 1.4V | I |
| 24 | LPO | External 32K or RTC clock | 0.2~3.3V | I |
| 25 | NC | Floating Pin, No connect to anything. | | Floating |
| 26 | NC | Floating Pin, No connect to anything. | | Floating |
| 27 | NC | Floating Pin, No connect to anything. | | Floating |
| 28 | NC | Floating Pin, No connect to anything. | | Floating |
| 29 | NC | Floating Pin, No connect to anything. | | Floating |
| 30 | NC | Floating Pin, No connect to anything. | | Floating |
| 31 | GND | Ground. | | GND |
| 32 | NC | Floating Pin, No connect to anything. | | Floating |
| 33 | GND | Ground. | | GND |

| | | | | |
|---|---|---|---|---|
| 34 | NC | Floating Pin, No connect to anything. | | Floating |
| 35 | NC | Floating Pin, No connect to anything. | | Floating |
| 36 | GND | Ground. | | GND |
| 37 | NC | Floating Pin, No connect to anything. | | Floating |
| 38 | NC | Floating Pin, No connect to anything. | | Floating |
| 39 | GPIO2 | Wi-Fi Co-existence pin with LTE(WLAN_SECI_RX) | VDDIO | I |
| 40 | GPIO1 | Wi-Fi Co-existence pin with LTE(WLAN_SECI_TX) | VDDIO | O |
| 41 | NC | Floating Pin, No connect to anything. | | Floating |
| 42 | NC | Floating Pin, No connect to anything. | | Floating |
| 43 | NC | Floating Pin, No connect to anything. | | Floating |
| 44 | NC | Floating Pin, No connect to anything. | | Floating |
| 45 | NC | Floating Pin, No connect to anything. | | Floating |
| 46 | NC | Floating Pin, No connect to anything. | | Floating |
| 47 | NC | Floating Pin, No connect to anything. | | Floating |

# 3. Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| VBAT | Power supply for | -0.5 | - | 6 | V |
| VDDIO | DC supply voltage | -0.5 | - | 3.9 | V |
| VDDIO_RF | supply voltage for | -0.5 | - | 3.9 | V |
| - | DC input supply | -0.5 | - | 1.575 | V |
| VDDRF | DC supply voltage | -0.5 | - | 1.32 | V |
| VDDC | DC supply voltage | -0.5 | - | 1.32 | V |
| Vundershoot | Maximum | - | -0.5 | - | V |
| Vovershoot | Maximum overshoot | - | VDDIO+0.5 | - | V |
| Tj | Maximum junction | - | 125 | - | °C |

a. Continuous operation at 6.0V is supported

b. Duration not to exceed 25% of the duty cycle

## 3.2 Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| VBAT | Power supply for Internal Regulators | 3 | - | 4.8 | V |

*The module is functional across this range of voltages. However, optimal RF performance specified in the data sheet is guaranteed only for 3.2V < VBAT <4.8V.

## 3.3 Digital IO Pin DC Characteristics

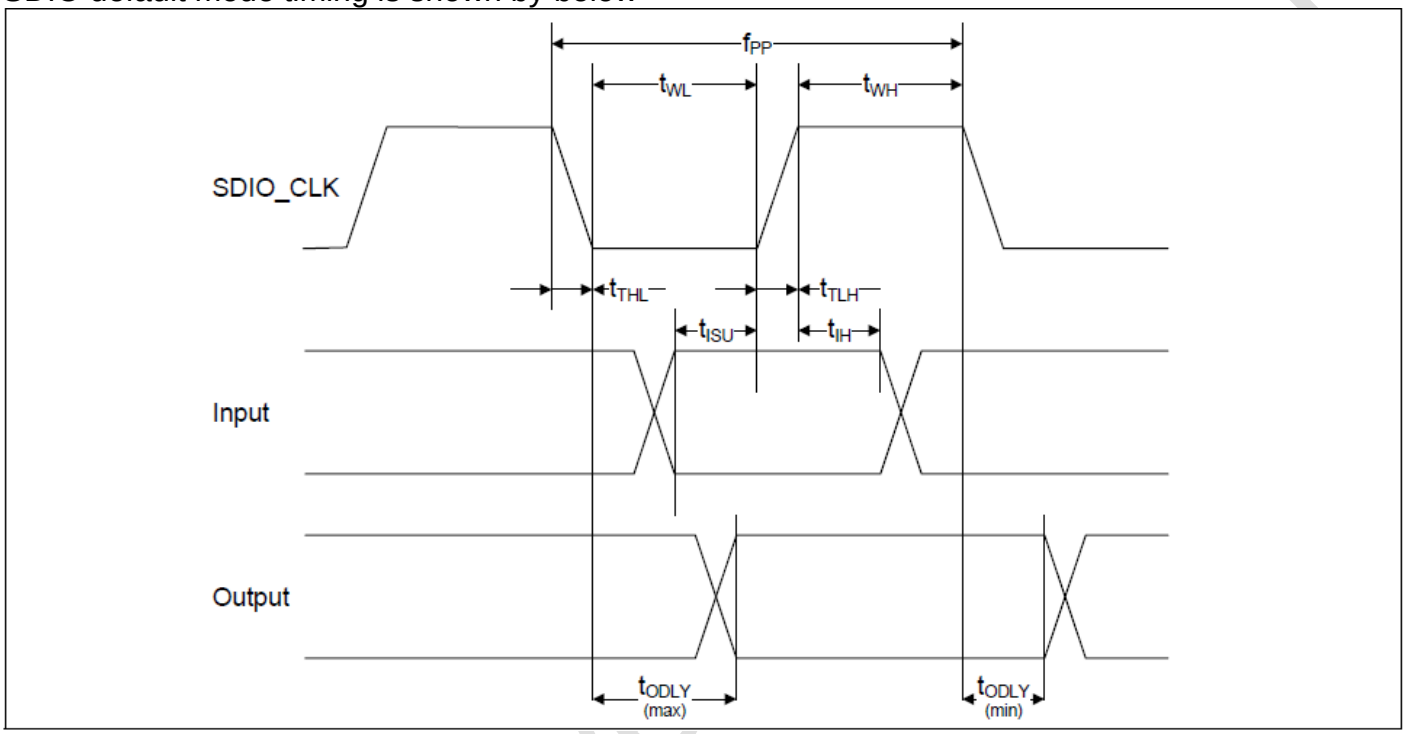
| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| SDIO Interface I/O pins (For VDDIO_SD=1.8V) | | | | | |
| VIH | Input high voltage | 1.27 | - | - | V |
| VIL | Input low voltage | - | - | 0.58 | V |
| VOH | Output high voltage @ 2 mA | 1.40 | - | - | V |
| VOL | Output low voltage @ 2 mA | - | - | 0.45 | V |
| For VDDIO_SD = 3.3V: | | | | | |

| | | | | | |
|---|---|---|---|---|---|
| VIH | Input high voltage | 0.625xVDDIO | - | - | V |
| VIL | Input low voltage | - | - | 0.25XVDDIO | V |
| VOH | Output high voltage @ 2 mA | 0.75xVDDIO | - | - | V |
| VOL | Output low voltage @ 2 mA | - | - | 0.125xVDDIO | V |
| Other Digital I/O Pins (For VDDIO = 1.8V) | | | | | |
| VIH | Input high voltage | 0.65xVDDIO | - | - | V |
| VIL | Input low voltage | - | - | 0.35Xvddio | V |
| VOH | Output high voltage @ 2 mA | VDDIO-0.45 | - | - | V |
| VOL | Output low voltage @ 2 mA | - | - | 0.45 | V |
| For VDDIO = 3.3V: | | | | | |
| VIH | Input high voltage | 2.00 | - | - | V |
| VIL | Input low voltage | - | - | 0.80 | V |
| VOH | Output high voltage @ 2 mA | VDDIO-0.4 | - | - | V |
| VOL | Output low voltage @ 2 mA | - | - | 0.40 | V |
| RF Switch Control Output Pinsc (For VDDIO_RF = 3.3V) | | | | | |
| VOH | Output high voltage @ 2 mA | VDDIO-0.4 | - | - | V |
| VOL | Output low voltage @ 2 mA | - | - | 0.40 | V |
| CIN | Input capacitance | - | - | 5 | pF |

## 3.4 Interface

### 3.4.1 SDIO Host Interface Specification

SDIO default mode timing is shown by below

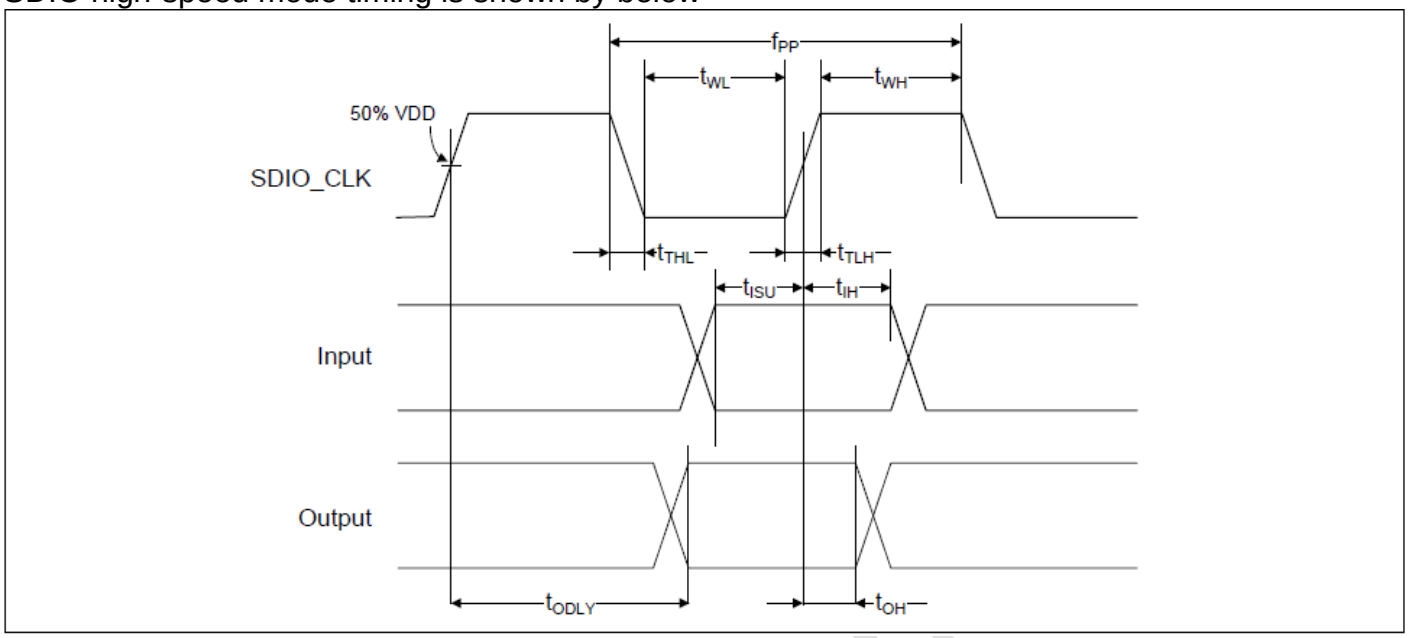



**SDIO Bus Timing (Default Mode)**

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| SDIO CLK (All values are referred to minimum VIH and maximum VILb) | | | | | |
| Frequency – Data Transfer mode | fPP | 0 | – | 25 | MHz |
| Frequency – Identification mode | fOD | 0 | – | 400 | kHz |
| Clock low time | tWL | 10 | – | – | ns |
| Clock high time | tWH | 10 | – | – | ns |
| Clock rise time | tTLH | – | – | 10 | ns |
| Clock low time | tTHL | – | – | 10 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup time | tISU | 5 | – | – | ns |
| Input hold time | tIH | 5 | – | – | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time – Data Transfer mode | tODLY | 0 | – | 14 | ns |
| Output delay time – Identification mode | tODLY | 0 | – | 50 | ns |

**SDIO Bus Timinga Parameters (Default Mode)**

SDIO high-speed mode timing is shown by below




**SDIO Bus Timing (High-speed Mode)**

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| SDIO CLK (all values are referred to minimum VIH and maximum VIL[b]) | | | | | |
| Frequency – Data Transfer Mode | fPP | 0 | – | 50 | MHz |
| Frequency – Identification Mode | fOD | 0 | – | 400 | kHz |
| Clock low time | tWL | 7 | – | – | ns |
| Clock high time | tWH | 7 | – | – | ns |
| Clock rise time | tTLH | – | – | 3 | ns |
| Clock low time | tTHL | – | – | 3 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup Time | tISU | 6 | – | – | ns |
| Input hold Time | tIH | 2 | – | – | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time – Data Transfer Mode | tODLY | – | – | 14 | ns |
| Output hold time | tOH | 2.5 | – | – | ns |
| Total system capacitance (each line) | CL | – | – | 40 | pF |

**SDIO Bus Timinga Parameters (Default Mode)**

### 3.4.2 Sequencing of Reset and Regulator Control Signals

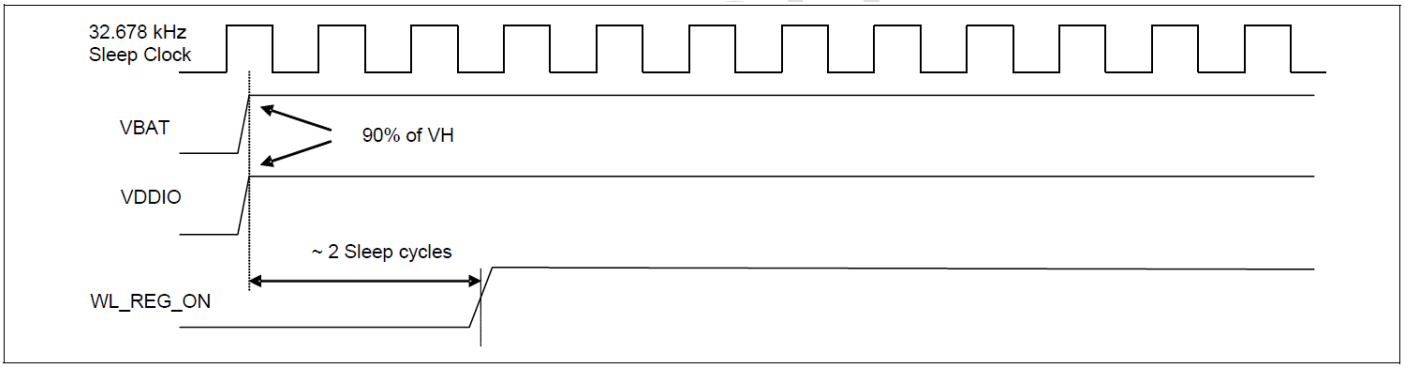
The AW-NM432SM has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

**Note**:

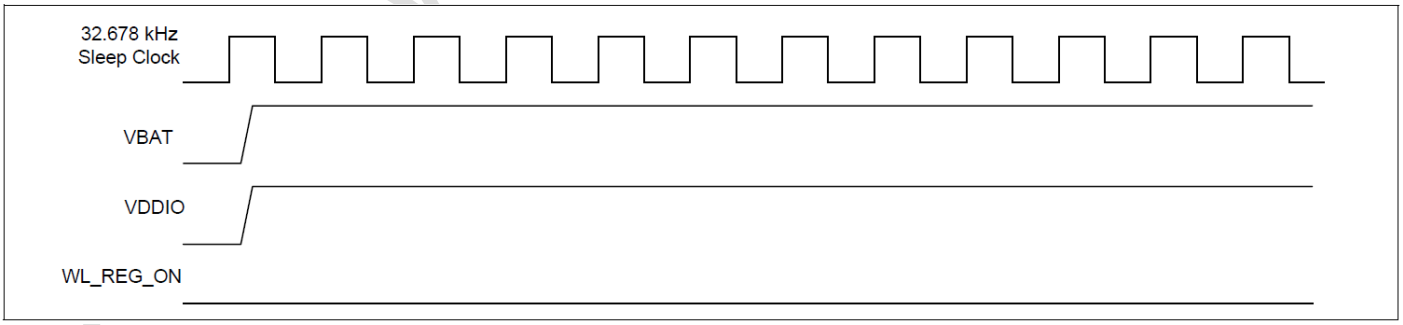
The AW-NM432SM has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

VBAT and VDDIO should not rise faster than 40 µs. VBAT should be up before or at the same time as VDDIO. VDDIO should not be present first or be held high before VBAT is high.

**WLAN=ON**




**WLAN=OFF**



## 3.5 Power Consumption*

### 3.5.1 WLAN

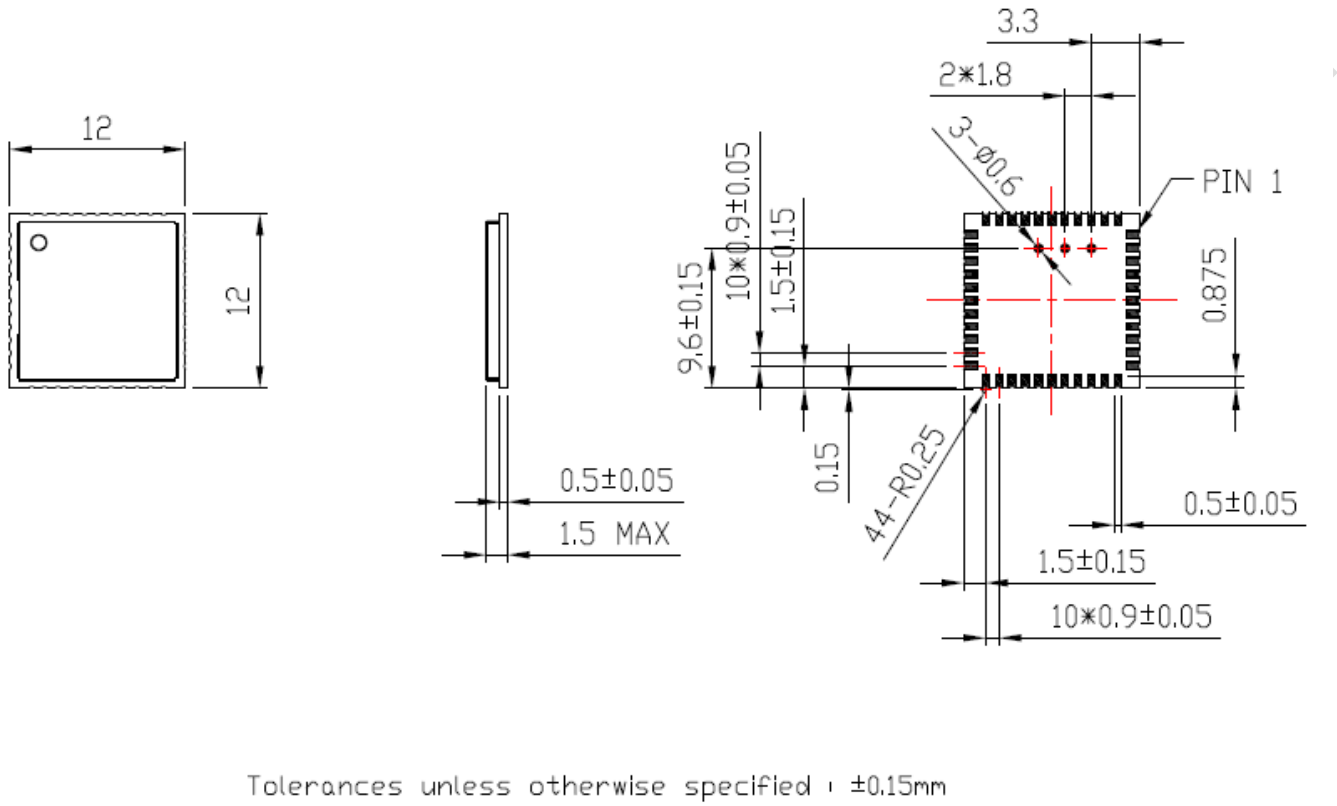
| | Item | | | VBAT=3.3V | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Transmit | | | Receive | |
| Band (GHz) | Mode | BW (MHz) | RF Power (dBm) | Max. | Avg. | DUTY % | Max. | Avg. |
| 2.4 | 11b@1Mbps | 20 | 17 | TBD | TBD | TBD | TBD | TBD |
| | 11b@11Mbps | 20 | 17 | TBD | TBD | TBD | TBD | TBD |
| | 11g@6Mbps | 20 | 15 | TBD | TBD | TBD | TBD | TBD |
| | 11g@54Mbps | 20 | 15 | TBD | TBD | TBD | TBD | TBD |
| | 11n@MCS0 | 20 | 13 | TBD | TBD | TBD | TBD | TBD |
| | 11n@MCS7 | 20 | 13 | TBD | TBD | TBD | TBD | TBD |

**Current Unit: mA**

* The power consumption is based on Azurewave test environment, these data for reference only.

# 4. Mechanical Information

## 4.1 Mechanical Drawing




Tolerances unless otherwise specified : ±0.15mm

# 5. Packaging Information

## 5.1


## 5.2


## 5.3

## 5.4


## 5.5

1 Carton= 5 Boxes


## 5.6