

AW-NM230NF-H

IEEE 802.11 b/g/n Wireless LAN and Bluetooth Module

Datasheet

Rev. A

B2

(For Standard)



Features

- Integrates Broadcom solutions of CYW43438_A1 WiFi /BT/FM RX SoC
- SDIO v2.0 interfaces support for WLAN
- High speed UART and PCM for Bluetooth
- Lead-free Design
- 16.0mm(L) x 12.0mm(W) x 1.53 mm(H) 108 pin LGA package

WiFi

- Single band 2.4 GHz 802.11 b/g/n
- SDIO v2.0, including DS and HS modes
- Security–WEP, WPA/WPA2 (personal), AES (HW), TKIP (HW), CKIP (SW), WMM/WMM-PS/WMM-SA
- Dara Rate up to 72.2Mbps

Bluetooth

 Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets

- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Maximum UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.2 packet types
- Fully supports Bluetooth Core Specification
 4.2 + (Enhanced Data Rate) EDR features:
 - Adaptive Frequency Hopping (AFH)
 - Quality of Service (QoS)
 - Extended Synchronous Connections (eSCO) — Voice Connections
 - Fast Connect (interlaced page and inquiry scans)
 - Secure Simple Pairing (SSP)
 - Sniff Subrating (SSR)
 - Encryption Pause Resume (EPR)
 - Extended Inquiry Response (EIR)
 - Link Supervision Timeout (LST)
- Interface support Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data



Revision History

Document NO: R2-2230NF-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
0.1	2015/4/17		Initial Version	Chao Lee	Amos Fu
0.2	2015/4/24		 Update Power Specifications Table 	Chao Lee	Amos Fu
0.3	2015/6/16		• Update ME drawing	Chao Lee	Amos Fu
0.4	2015/7/31		Update Block Diagram	Chao Lee	Amos Fu
0.5	2015/8/17		• Add power consumption	Chao Lee	Amos Fu
0.6	2015/11/26		Update Electrical Characteristics	Chao Lee	Amos Fu
0.7	2016/06/27		 Added description for pin 11 & pin 12. 	Steven Jian	Chihhao Liao
0.8	2018/12/24		 Updated Document Format BT support 4.2 	Steven Jian	Chihhao Liao
0.9	2019/11/06		• Updated 1.4	Steven Jian	Chihhao Liao
A	2020/03/14	DCN016857	 Changed Document format Updated 3. Electrical Characteristics Updated 1.3.3 Bluetooth 	Steven Jian	Chihhao Liao



Table of Contents

Revision History	3
Table of Contents	4
1. Introduction	5
1.1 Product Overview	5
1.2 Block Diagram	6
1.3 Specifications Table	7
1.3.1 General	7
1.3.2 WLAN	7
1.3.3 Bluetooth	8
1.3.4 Operating Conditions	9
2. Pin Definition	10
2.1 Pin Map	
2.2 Pin Table	11
3. Electrical Characteristics	16
3.1 Absolute Maximum Ratings	
3.2 Recommended Operating Conditions	
3.3 Digital IO Pin DC Characteristics	
3.4 Host Interface	
3.4.1 SDIO	
3.4.2 UART Interface	
3.4.3 PCM Interface Timing	
3.5 Power up Timing Sequence	
3.6 Frequency References	
3.7 Power Consumption*	
3.7.1 WLAN	
3.7.2 Bluetooth	
4. Mechanical Information	27
4.1 Mechanical Drawing	27
5. Packaging Information	



1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced IEEE 802.11 b/g/n WLAN and Bluetooth combo module - AW-NM230NF-H. The module is targeted to mobile and embedded devices which need small footprint package, low power consumption, and multiple OS support. The module supports 2.4GHz IEEE 802.11n MAC/baseband/radio, and Bluetooth 4.2 functionality. It also features an integrated Power Management Unit (PMU), Power Amplifiers (PAs), and a Low Noise Amplifier (LNA) to address the needs of mobile devices that require minimal power consumption and compact size. By using AW-NM230NF-H, the customers can easily enable the Wi-Fi and BT embedded applications with the benefits of high design flexibility, short development cycle, and quick time-to-market. Specified in the IEEE 802.11 standard minimize the system power requirements by using AW-NM230NF-H. In addition to the support of WPA/WPA2 (personal) and WEP encryption, the AW-NM230NF-H also supports the IEEE 802.11i security standard through AES and TKIP acceleration hardware for faster data encryption. For the video, voice and multimedia applications the AW-NM230NF-H support 802.11e Quality of Service (QoS). The host interface is SDIO v2.0 interface.

For Bluetooth operation, the AW-NM230NF-H is Bluetooth 4.2 compliant. The Bluetooth transmitter also features a Class 1 power amplifier. The AW-NM230NF-H supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets, and Adaptive Frequency Hopping (AFH) for reducing radio frequency interference. It also incorporates all Bluetooth 4.2 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume. An independent, high-speed UART is provided for the Bluetooth host interface. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high speed UART and PCM for audio.

FORM NO.: FR2-015_A Responsible Department : WBU Expirv Date: Forever The information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of AzureWave.



A simplified block diagram of the AW-NM230NF-H module is depicted in the figure below.



1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 b/g/n Wireless LAN and Bluetooth M.2 Combo Module
Major Chipset	Cypress CYW43438_A1
Host Interface	WLAN: SDIO v2.0 Bluetooth: UART
Dimension	16.0mm(L) x 12.0mm(W) x 1.53mm(H)
Package	M.2 1216 Solder down
Antenna	2.4G Ant: WiFi/BT
Weight	0.5g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant
WLAN VID/PID	N/A
WLAN SVID/SPID	N/A
Frequency Rage	WLAN: 2.4 GHz
Modulation	DSSS, OFDM, BPSK(9/6Mbps), QPSK(18/12Mbps), DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps), 16-QAM(36/24Mbps), 64-QAM (72.2/54/48Mbps)
Number of Channels	802.11b: USA, Canada and Taiwan $-1 \sim 11$ Most European Countries $-1 \sim 13$ Japan $-1 \sim 14$ 802.11g: USA and Canada $-1 \sim 11$ Most European Countries $-1 \sim 13$ 802.11n: USA and Canada $-1 \sim 11$ Most European Countries $-1 \sim 13$

FORM NO.: FR2-015_AResponsible Department : WBUExpiry Date: ForeverThe information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or
disclosed in whole or in part without prior written permission of AzureWave.Expiry Date: Forever

7

	2.4G				
		Min	Тур	Max	Unit
Output Power	11b (11Mbps) @EVM<35%	15	17	19	dBm
	11g (54Mbps) @EVM≦-25 dB	13	15	17	dBm
	11n (HT20 MCS7) @EVM≦-27 dB	11	13	15	dBm
	2.4G				
		Min	Тур	Max	Unit
	11b (1Mbps)		-96	-91	dBm
Receiver Sensitivity	11g (6Mbps)		-91	-84	dBm
	11b (11Mbps)		-89	-82	dBm
	11g (54Mbps)		-76	-68	dBm
	11n (HT20 MCS0)		-91	-84	dBm
	11n (HT20 MCS7)		-73	-66	dBm
Data Rate	802.11b: 1, 2, 5.5, 11Mb 802.11g: 6, 9, 12, 18, 24 802.11n:MCS 0~7 HT20	ops 1, 36, 48, 54)	Mbps		
Security	 WPA[™]- and WPA2[™]- (Personal) support for powerful encryption and authentication AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility Cisco® Compatible Extension- (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX5.0) certified Wi-Fi Protected Setup (WPS) WEP WMM / WMM-SA CKIP(Software) 				

1.3.3 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth 4.2
Bluetooth VID/PID	N/A
Frequency Rage	2400~2483.5MHz
Modulation	GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)

FORM NO.: FR2-015_AResponsible Department : WBUExpiry Date: ForeverThe information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or
disclosed in whole or in part without prior written permission of AzureWave.Expiry Date: Forever

8

Output Power	Basic Rate : 7.5dBm +/- 2.5dBm (Max Settings)				
		Min	Тур	Max	Unit
Receiver Sensitivity	DH5		-91	-82	dBm
Receiver Sensitivity	2DH5		-93	-84	dBm
	3DH5		-87	-76	dBm

1.3.4 Operating Conditions

Features	Description			
Operating Conditions				
Voltage	Input supply for host I/O : 3.3V			
Operating Temperature	-30~70 °C (Optimal RF performance guarantee -20~70 °C)			
Operating Humidity	less than 85% R.H.			
Storage Temperature	-20~85 °C			
Storage Humidity	less than 60% R.H.			
ESD Protection				
Human Body Model	±1.25KV			
Changed Device Model	±175V			

2.1 Pin Map

2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Туре
1	NC	No Connect		Floating
2	NC	No Connect		Floating
3	NC	No Connect		Floating
4	3.3V	3.3V power pin	3.3V	VCC
5	3.3V	3.3V power pin	3.3V	VCC
6	GND	Ground.		GND
7	NC	No Connect		Floating
8	NC	No Connect		Floating
9	NC	No Connect		Floating
10	NC	No Connect		Floating
11	GPIO1	Programmable. Can be configured as WLAN SECI Tx output to an LTE IC	3.3V	I/O
12	GPIO2	Programmable. Can be configured as WLAN SECI Rx input from an LTE IC	3.3V	1/0
13	NC	No Connect		Floating
14	NC	No Connect		Floating
15	NC	No Connect		Floating
16	NC	No Connect		Floating
17	GND	Ground.		GND
18	NC	No Connect		Floating
19	NC	No Connect		Floating
20	GND	Ground.		GND
21	NC	No Connect		Floating
22	NC	No Connect		Floating
23	GND	Ground		GND
24	BT_HOST_WAKE_D EV	BT Device Wake	3.3V	I
25	NC	No Connect		Floating
26	GND	Ground		GND

27	SUSCLK(32kHz)	External sleep clock input (32.768 kHz).	3.3V	I
28	WL_DIS#	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.	3.3V	1
29	NC	No Connect		Floating
30	NC	No Connect		Floating
31	NC	No Connect		Floating
32	GND	Ground		GND
33	NC	No Connect		Floating
34	NC	No Connect		Floating
35	GND	Ground		GND
36	NC	No Connect		Floating
37	NC	No Connect		Floating
38	GND	Ground		GND
39	NC	No Connect		Floating
40	NC	No Connect		Floating
41	GND	Ground		GND
42	NC	No Connect		Floating
43	NC	No Connect		Floating
44	NC	No Connect		Floating
45	WL_DIS#	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.	3.3V	1
46	WL_DEV_WAKE_H OST	WL Host Wake	3.3V	0
47	SDIO_D3	SDIO Data Line 3	3.3V	I/O
48	SDIO_D2	SDIO Data Line 2	3.3V	I/O

49	SDIO_D1	SDIO Data Line 1	3.3V	I/O
50	SDIO_D20	SDIO Data Line 0	3.3V	I/O
51	SDIO_CMD	SDIO Command Input	3.3V	I/O
52	SDIO_CLK	SDIO Clock Input	3.3V	I
53	BT_DEV_WAKE_HO ST	BT Host Wake	3.3V	ο
54	UART_CTS	High-Speed UART CTS	3.3V	I
55	UART_OUT	High-Speed UART Data Out	3.3V	0
56	UART_IN	High-Speed UART Data In	3.3V	I
57	UART_RTS	High-Speed UART RTS	3.3V	0
58	PCM_SYNC	PCM Synchronization control	3.3V	0
59	PCM_IN	PCM data Input	3.3V	I
60	PCM_OUT	PCM data Out	3.3V	0
61	PCM_CLK	PCM Clock	3.3V	I/O
62	GND	Ground		GND
63	BT_DIS#	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.	3.3V	1
64	NC	No Connect		Floating
65	NC	No Connect		Floating
66	NC	No Connect		Floating
67	NC	No Connect		Floating
68	GND	Ground		GND
69	NC	No Connect		Floating
70	NC	No Connect		Floating
71	GND	Ground		GND
72	3.3V	3.3V power pin	3.3V	VCC
73	3.3V	3.3V power pin	3.3V	VCC

74	GND	Ground	GND
75	GND	Ground	GND
76	GND	Ground	GND
77	GND	Ground	GND
78	GND	Ground	GND
79	GND	Ground	GND
80	GND	Ground	GND
81	GND	Ground	GND
82	GND	Ground	GND
83	GND	Ground	GND
84	GND	Ground	GND
85	GND	Ground	GND
86	GND	Ground	GND
87	GND	Ground	GND
88	GND	Ground	GND
89	GND	Ground	GND
90	GND	Ground	GND
91	GND	Ground	GND
92	GND	Ground	GND
93	GND	Ground	GND
94	GND	Ground	GND
95	GND	Ground	GND
96	GND	Ground	GND
G1	GND	Ground	GND
G2	GND	Ground	GND
G3	GND	Ground	GND
G4	GND	Ground	GND
G5	GND	Ground	GND
G6	GND	Ground	GND
G7	GND	Ground	GND

G8	GND	Ground	GND
G9	GND	Ground	GND
G10	GND	Ground	GND
G11	GND	Ground	GND
G12	GND	Ground	GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	Power supply for Internal Regulators	-0.5		3.9	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	Power supply for Internal Regulators	3*	3.3	3.46	V

*Optimal RF performance is guaranteed only for 3.2V<VBAT<3.46V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit					
For SDIO	For SDIO Interface VDDIO =3.3V									
VIH	Input high voltage	2.06	-	-	V					
VIL	Input low voltage	-	-	0.82	V					
VOH	Output High Voltage @ 2mA	2.47	-	-	V					
VOL	Output Low Voltage @ 2mA	-	-	0.41	V					
Other Dig	ital Interface VDDIO=3.3V	·								
VIH	Input high voltage	2	-	-	V					
VIL	Input low voltage	-	-	0.8	V					
VOH	Output High Voltage @ 2mA	2.9	-	-	V					
VOL	Output Low Voltage @ 2mA	-	-	0.4	V					

3.4 Host Interface

3.4.1 SDIO

SDIO Bus Timing (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit				
SDIO CLK (All values are referred to minimum VIH and maximum VIL*)									
Frequency – Data Transfer mode	fPP	0	_	25	MHz				
Frequency – Identification mode	fOD	0	_	400	kHz				
Clock low time	tWL	10	_	_	ns				
Clock high time	tWH	10	_	_	ns				
Clock rise time	tTLH	_	_	10	ns				
Clock low time	tTHL	_	_	10	ns				
Inputs: CMD, DAT (referenced to CLK)									
Input setup time	tISU	5	_	_	ns				
Input hold time	tIH	5	_	_	ns				
Outputs: CMD, DAT (referenced to CLK)	Outputs: CMD, DAT (referenced to CLK)								
Output delay time – Data Transfer mode	tODLY	0	_	14	ns				
Output delay time – Identification mode	tODLY	0	_	50	ns				

17

Expiry Date: Forever

SDIO Bus Timing Parameters (Default Mode)

* min(VIH) = $0.7 \times VDDIO$ and max(VIL) = $0.2 \times VDDIO$

SDIO Bus Timing (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit				
SDIO CLK (all values are referred to minimum VIH and maximum VIL*)									
Frequency – Data Transfer Mode	fPP	0	_	50	MHz				
Frequency – Identification Mode	fOD	0	_	400	kHz				
Clock low time	tWL	7	_	_	ns				
Clock high time	tWH	7	_	_	ns				
Clock rise time	tTLH	-	_	3	ns				
Clock low time	tTHL	-	_	3	ns				
Inputs: CMD, DAT (referenced to CLK)			·	·					
Input setup Time	tISU	6	-	-	ns				
Input hold Time	tIH	2	_	_	ns				
Outputs: CMD, DAT (referenced to CLK)			·	·					
Output delay time – Data Transfer Mode	tODLY	-	_	14	ns				
Output hold time	tOH	2.5	_	_	ns				
Total system capacitance (each line)	CL	_	_	40	pF				

SDIO Bus Timing a Parameters (High-Speed Mode)

* min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO

FORM NO.: FR2-015_A

Expiry Date: Forever

The information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of AzureWave.

3.4.2 UART Interface

The AW-NM230NF-H includes a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification ("Three-wire UART Transport Layer").Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The AW-NM230NF-H UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-NM230NF-H UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

FORM NO.: FR2-015 A Responsible Department : WBU Expiry Date: Forever The information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of AzureWave.

UART Timing

UANI						
	Reference Characteristics	Minimum	Typical	Maximum	Unit	
1	Delay time, UART_CTS_N low to UART_TXD valid	-	-	1.5	Bit periods	
2	Setup time, UART_CTS_N high before midpoint of stop bit	(Ð	0.5	Bit periods	
3	Delay time, midpoint of stop bit to UART_RTS_N high	- ()	-	0.5	Bit periods	

UART Timing Specifications

3.4.3 PCM Interface Timing

PCM Timing Diagram(Short Frame Sync, Master Mode)

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC delay	0		25	ns
5	PCM_OUT delay	0		25	ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

PCM Timing Diagram(Short Frame Sync, Slave Mode)

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC setup	8			ns
5	PCM_SYNC hold	8			ns
6	PCM_OUT delay	0		25	ns
7	PCM_IN setup	8			ns

	.			
8	PCM_IN hold	8		ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	25	ns

PCM Timing Diagram(Long Frame Sync, Master Mode)

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC delay	0		25	ns
5	PCM_OUT delay	0		25	ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

PCM Timing Diagram(Long Frame Sync, Slave Mode)

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12	MHz
2	PCM bit clock low	41			ns
3	PCM bit clock high	41			ns
4	PCM_SYNC setup	8			ns
5	PCM_SYNC hold	8			ns
6	PCM_OUT delay	0		25	ns
7	PCM_IN setup	8			ns
8	PCM_IN hold	8			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0		25	ns

3.5 Power up Timing Sequence

WLAN = ON, Bluetooth = ON

FORM NO.: FR2-015_AResponsible Department : WBUExpiry Date: ForeverThe information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or
disclosed in whole or in part without prior written permission of AzureWave.Expiry Date: Forever

23

WLAN = OFF, Bluetooth = OFF

32.678 kHz Sleep Clock	
3.3V	$\cdot $
WL_DIS#	XVV
BT_DIS#	
WLAN = ON. Bluetooth = OFF	
32.678 kHz Sleep Clock	
90% of VH	
3.3V ~ 2 Sleep cycles	
WL_DIS#	
BT_DIS#	
WLAN = OFF, Bluetooth = ON	
32.678 kHz Sleep Clock	
32.678 kHz Sleep Clock 90% of VH	
32.678 kHz Sleep Clock 90% of VH 3.3V ~ 2 Sleep cycles	
32.678 kHz Sleep Clock 90% of VH 3.3V ~ 2 Sleep cycles WL_DIS#	
32.678 kHz Sleep Clock 90% of VH 3.3V ~ 2 Sleep cycles WL_DIS# BT_DIS#	

 Expiry Date: Forever

 FORM NO.: FR2-015_A Responsible Department : WBU Expiry Date: Forever

 The information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of AzureWave.

3.6 Frequency References

The AW-NM230NF-H uses an internal 26MHz xtal for normal operation and an external secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz \pm 30% over process, voltage, and temperature, which is adequate for some applications. However, a trade-off caused by this wide LPO tolerance is a small current consumption increase during WLAN power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

The preferred approach for WLAN is to connect a precision external 32.768 kHz clock that meets the requirements listed in Table below.

Parameter	LPO	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+-200	ppm
Duty cycle	30 - 70	%
Input signal amplitude	200 - 3300	mV,p-p
Input impedance	>100	kΩ
	<5	pF
Signal type	Square-wave or sine-wave	-
Clock jitter (during initial start-up)	<10000 ppm	

3.7 Power Consumption*

3.7.1 WLAN

Test Bed		ThinkPad T60
Test OS		Ubuntu 12.04
Test AP		RT-AC66U
Driver Version		1.201.34
Test Voltage		3.3V
Item		Current value
No connect AP	AVG	17.1 mA
	MAX	19.8 mA
	MIN	16.9 mA
Connect AP *(1)	AVG	58.4 mA
	MAX	255.2 mA
	MIN	58.3 mA
WLAN RF OFF *(2)		13.5 mA
Transmit by HT20		252.8 mA

Receiver by HT20

101.7 mA

(1) DTIM = 1, Beacon Interval = 100 ms.

(2) WL-DIS =LOW

3.7.2 Bluetooth

(1) Using Bluetooth tool to Meausure TX/RX

(2) No connect BT device is download firmware then did not do anything.

(3) BT-DIS =LOW.

(4) DH5 Output power @ 6 dBm

* The power consumption is based on Azurewave test environment, these data for reference only.

FORM NO.: FR2-015_AResponsible Department : WBUExpiry Date: ForeverThe information contained herein is the exclusive property of AzureWave and shall not be distributed, reproduced, or
disclosed in whole or in part without prior written permission of AzureWave.Expiry Date: Forever

26

4. Mechanical Information

4.1 Mechanical Drawing

5. Packaging Information

5.1

HUMIDITY INDICATOR CARD

AFFIX PACKING LABEL

5.2

AFFIX PACKING LAB

AFFIX PACKING LABEL

5.3

PINK BUBBLE WRAP

AFFIX PACKING LABEL

