

AW-CM467S

IEEE 802.11 a/b/g/n/ac and Bluetooth 5.0 Module

Datasheet

Rev. A

DF

(For Standard)

Features

Wi-Fi

- Dual band 802.11 a/b/g/n/ac/d/r/w/e/h/i/k
- Single-stream spatial multiplexing up to 433.3 Mbps
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Security: WEP, WPA/WPA2 (personal), AES (HW), TKIP (HW), CKIP (software support)

Bluetooth

- Qualified for Bluetooth Core Specification 5.0 with all Bluetooth 4.2 optional features
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.

Revision History

Document NO:

| Version | Revision Date | DCN NO. | Description | Initials | Approved |
|---------|---------------|---------|---|----------|--------------|
| A | 2020/04/15 | | <ul style="list-style-type: none"> Initial Version | JM.Pang | Chihhao Liao |
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1. Introduction

1.1 Product Overview

The Cypress AW-CM467S device provides the highest level of integration for embedded and IoT wireless systems with integrated single-stream IEEE 802.11a/b/g/n/ac, MAC/baseband/radio and Bluetooth 5.0 (Basic Rate, Enhanced Data Rate and Bluetooth Low Energy).

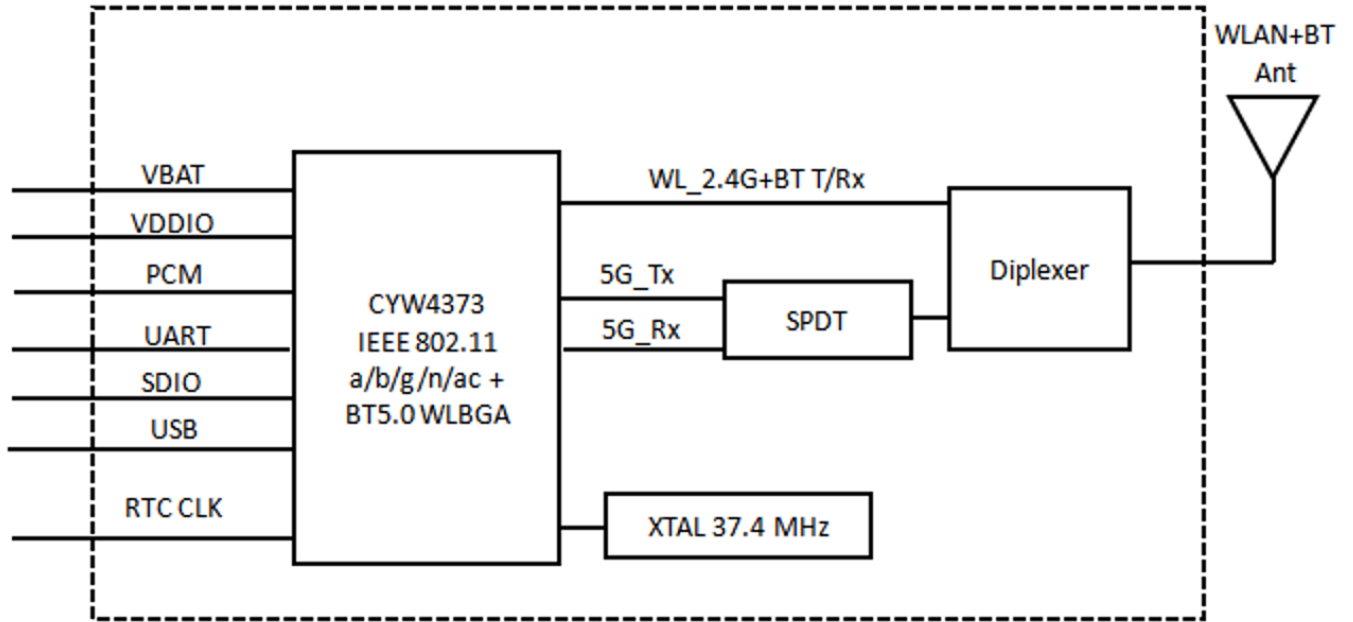
AW-CM467S supports all rates specified in the IEEE 802.11 a/b/g/n/ac specifications. IEEE 802.11ac's 256-QAM is supported for MCS8 in 20 MHz channels and MCS8/MCS9 in 40 MHz & 80 MHz channels to enable data rates of up to 433.3 Mbps. Included on-chip are 2.4 GHz and 5 GHz power amplifiers and low-noise amplifiers.

The WLAN section supports the following host interface options: an SDIO v3.0 interface that can operate in 4b or 1b mode and a USB 2.0 interface. The Bluetooth section supports USB 2.0, USB 1.1, SDIO and a high-speed 4-wire UART interface. An on-chip USB 2.0 hub provides a shared single USB connection to both WLAN and Bluetooth target devices.

Using advanced design techniques and process technology to reduce active and idle power, the AW-CM467S is designed to address the need of mobile devices that require minimal power consumption and compact size. It includes a power management unit (PMU) which simplifies the system power topology and allows for direct operation from a mobile platform battery while maximizing battery life.

The AW-CM467S implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on an embedded and IoT system is achieved.

1.2 Block Diagram



AW-CM467S BLOCK DIAGRAM

1.3 Specifications Table

1.3.1 General

| Features | Description |
|---------------------|---|
| Product Description | IEEE 802.11 a/b/g/n/ac Wireless LAN and Bluetooth Module |
| Major Chipset | Cypress CYW4373 |
| Host Interface | Wi Fi : SDIO,USB Bluetooth : UART,USB |
| Dimension | 14mm(L) x 13mm(W) x 2mm(H) |
| Package | LGA |
| Antenna | 1 antenna to support 1(Transmit) x 1(Receive) technology and Bluetooth 1 antenna to support Bluetooth (option) |
| Weight | TBD |

1.3.2 WLAN

| Features | Description |
|--------------------|---|
| WLAN Standard | IEEE 802.11a/b/g/n/ac |
| WLAN VID/PID | N/A |
| WLAN SVID/SPID | N/A |
| Frequency Range | WLAN: 2.4 GHz / 5GHz Band |
| Modulation | DSSS DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) OFDM BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9) |
| Number of Channels | 802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 Japan – 1 ~ 13 802.11g: USA and Canada – 1 ~ 11 |

Most European Countries – 1 ~ 13
 802.11n:
 USA and Canada – 1 ~ 11
 Most European Countries – 1 ~ 13
 802.11a:
 USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120,
 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

2.4G

| | Min | Typ | Max | Unit |
|----------------------------------|-----|-----|-----|------|
| 11b (11Mbps) @EVM<35% | TBD | TBD | TBD | dBm |
| 11g (54Mbps) @EVM ≤ -27 dB | TBD | TBD | TBD | dBm |
| 11n (HT20 MCS7) @EVM ≤ -28 dB | TBD | TBD | TBD | dBm |

5G

| | Min | Typ | Max | Unit |
|------------------------------------|-----|-----|-----|------|
| 11a (54Mbps) @EVM ≤ -25 dB | TBD | TBD | TBD | dBm |
| 11n (HT20 MCS7) @EVM ≤ -27 dB | TBD | TBD | TBD | dBm |
| 11n (HT40 MCS7) @EVM ≤ -27 dB | TBD | TBD | TBD | dBm |
| 11ac (VHT20 MCS8) @EVM ≤ -30 dB | TBD | TBD | TBD | dBm |
| 11ac (VHT40 MCS9) @EVM ≤ -32 dB | TBD | TBD | TBD | dBm |
| 11ac (VHT80 MCS9) @EVM ≤ -32 dB | TBD | TBD | TBD | dBm |

2.4G

| | Min | Typ | Max | Unit |
|-----------------|-----|-----|-----|------|
| 11b (11Mbps) | | TBD | TBD | dBm |
| 11g (54Mbps) | | TBD | TBD | dBm |
| 11n (HT20 MCS7) | | TBD | TBD | dBm |

5G(n/ac packets with LDPC)

| | Min | Typ | Max | Unit |
|-----------------|-----|-----|-----|------|
| 11a (54Mbps) | | TBD | TBD | dBm |
| 11n (HT20 MCS7) | | TBD | TBD | dBm |
| 11n (HT40 MCS7) | | TBD | TBD | dBm |

| | | | | | |
|-----------|---|--|-----|-----|-----|
| | 11ac (VHT20 MCS8) | | TBD | TBD | dBm |
| | 11ac (VHT40 MCS9) | | TBD | TBD | dBm |
| | 11ac (VHT80 MCS9) | | TBD | TBD | dBm |
| Data Rate | 802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n: MCS0~7 HT20/HT40 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11ac: MCS0~8 VHT20 802.11ac: MCS0~9 VHT40/VHT80 | | | | |
| Security | <ul style="list-style-type: none"> ● WPA™- and WPA2™- (Personal) support for powerful encryption and authentication ● AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility ● Wi-Fi Protected Setup (WPS) ● WEP ● CKIP(Software) | | | | |

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

| Features | Description | | | | |
|----------------------|--|-----|-----|-----|------|
| Bluetooth Standard | Bluetooth 2.1+Enhanced Data Rate (EDR)/BT3.0/BT4.2/BT5.0 | | | | |
| Bluetooth VID/PID | N/A | | | | |
| Frequency Range | 2400~2483.5MHz | | | | |
| Modulation | GFSK (1Mbps), $\pi/4$ DQPSK (2Mbps) and 8DPSK (3Mbps) | | | | |
| Output Power | | Min | Typ | Max | Unit |
| | DH5 | TBD | TBD | TBD | dBm |
| | 2DH5 | TBD | TBD | TBD | dBm |
| | 3DH5 | TBD | TBD | TBD | dBm |
| Receiver Sensitivity | | Min | Typ | Max | Unit |
| | DH5 | TBD | TBD | TBD | dBm |
| | 2DH5 | TBD | TBD | TBD | dBm |
| | 3DH5 | TBD | TBD | TBD | dBm |

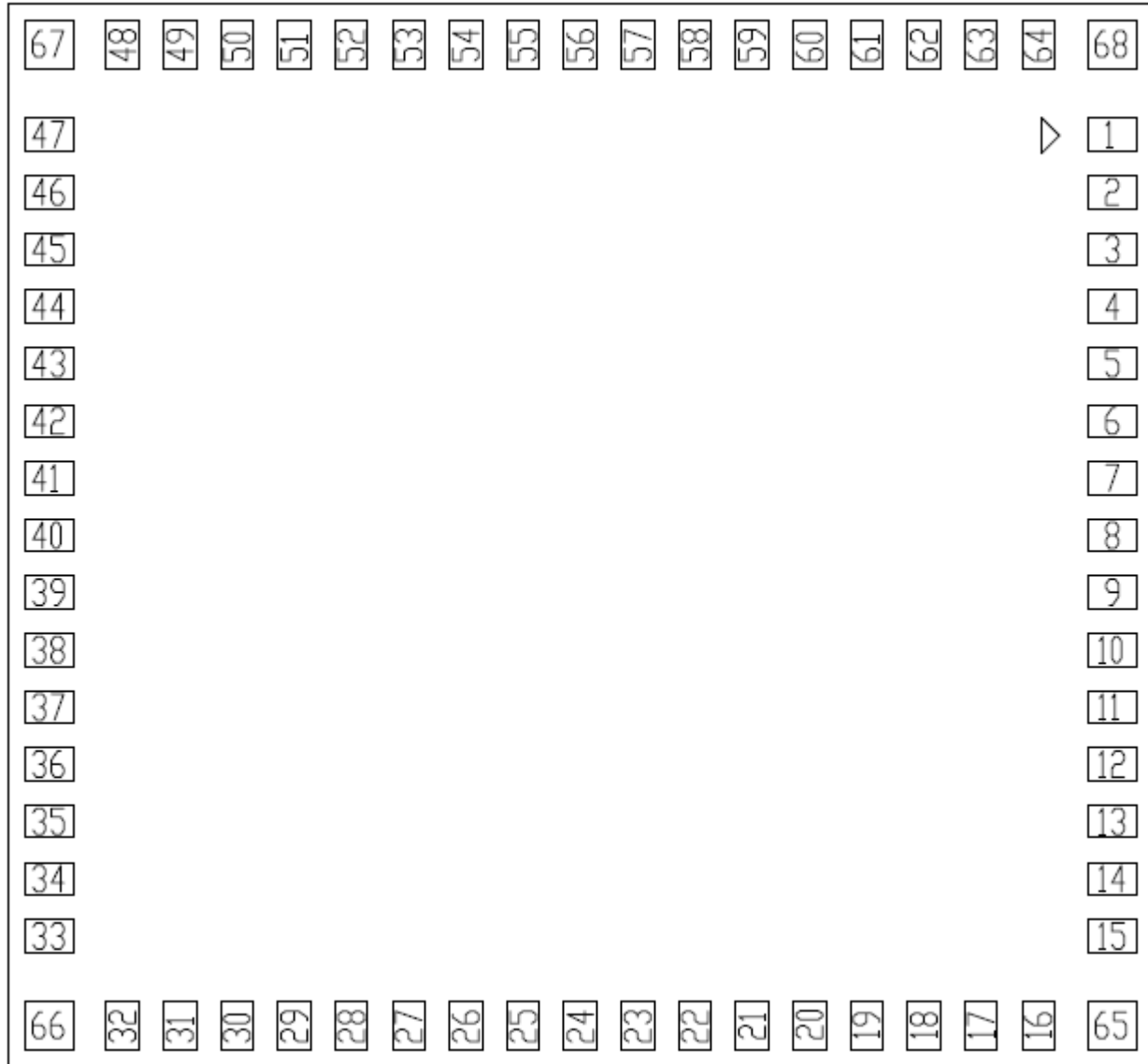
1.3.4 Operating Conditions

| Features | Description |
|-----------------------|--------------------|
| Operating Conditions | |
| Voltage | 3.6 V– 4.8 V |
| Operating Temperature | -10~60°C |
| Operating Humidity | less than 85% R.H. |
| Storage Temperature | -40~85°C |
| Storage Humidity | less than 60% R.H. |
| ESD Protection | |
| Human Body Model | TBD |
| Charged Device Model | TBD |

2. Pin Definition

2.1 Pin Map

AW-CM467S Bottom View Pin Map



2.2 Pin Table

| Pin No | Definition | Basic Description | Voltage | Type |
|--------|---------------|---|---------|----------|
| 1 | GND | Ground | | GND |
| 2 | WL_REG_ON | Used by PMU to power-up or power down the internal CYW4373 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. | VDDIO | I |
| 3 | GND | Ground | | GND |
| 4 | NC | Floating Pin | | Floating |
| 5 | USB_DP | Data plus of shared USB2.0 port. | 3.3V | I/O |
| 6 | USB_DM | Data minus of shared USB2.0 port. | 3.3V | I/O |
| 7 | NC | Floating Pin | | Floating |
| 8 | NC | Floating Pin | | Floating |
| 9 | WL_HOST_WAKE | WL Host Wake | VDDIO | O |
| 10 | BT_REG_ON | Used by PMU to power-up or power down the internal CYW4373 regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. | VDDIO | I |
| 11 | BT_PCM_IN | PCM data input. | VDDIO | I |
| 12 | LPO | External 32K or RTC clock | | I |
| 13 | BT_PCM_CLK | PCM clock; can be master (output) or slave (input). | VDDIO | I/O |
| 14 | BT_PCM_SYNC | PCM sync; can be master (output) or slave (input), or SLIMbus data. | VDDIO | I/O |
| 15 | BT_PCM_OUT | PCM data output. | VDDIO | O |
| 16 | BT_DEV_WAKE | Bluetooth DEV_WAKE. | VDDIO | I/O |
| 17 | BT_UART_CTS_N | UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface. | VDDIO | I |
| 18 | BT_UART_TXD | UART serial output. Serial data output for the HCI UART interface. | VDDIO | O |
| 19 | BT_UART_RXD | UART serial input. Serial data input for the HCI UART interface. | VDDIO | I |
| 20 | BT_HOST_WAKE | Bluetooth HOST_WAKE. | VDDIO | I/O |
| 21 | BT_UART_RTS_N | UART request-to-send. Active-low request-to-send signal for the HCI UART interface. | VDDIO | O |
| 22 | NC | Floating Pin | | Floating |
| 23 | NC | Floating Pin | | Floating |
| 24 | NC | Floating Pin | | Floating |
| 25 | NC | Floating Pin | | Floating |

| | | | | |
|----|---------------|---|----------|----------|
| 26 | GND | Ground | | GND |
| 27 | BT_ANT | BT RF TX/RX path. | | RF |
| 28 | GND | Ground | | GND |
| 29 | NC | Floating Pin | | Floating |
| 30 | GND | Ground | | GND |
| 31 | WL_BT_ANT | WLAN/BT RF TX/RX path | | RF |
| 32 | GND | Ground | | GND |
| 33 | NC | Floating Pin | | Floating |
| 34 | NC | Floating Pin | | Floating |
| 35 | NC | Floating Pin | | Floating |
| 36 | GND | Ground | | GND |
| 37 | NC | Floating Pin | | Floating |
| 38 | NC | Floating Pin | | Floating |
| 39 | NC | Floating Pin | | Floating |
| 40 | NC | Floating Pin | | Floating |
| 41 | VBAT | Power Pin | 3.6~4.8V | VCC |
| 42 | NC | Floating Pin | | Floating |
| 43 | NC | Floating Pin | | Floating |
| 44 | RF_SW_CTRL5 | Programmable RF switch control lines. | 3.3V | O |
| 45 | GND | Ground | | GND |
| 46 | NC | Floating Pin | | Floating |
| 47 | NC | Floating Pin | | Floating |
| 48 | NC | Floating Pin | | Floating |
| 49 | NC | Floating Pin | | Floating |
| 50 | NC | Floating Pin | | Floating |
| 51 | NC | Floating Pin | | Floating |
| 52 | GND | Ground | | GND |
| 53 | VDDIO | VDDIO supply for WLAN and BT | 1.8/3.3V | VCC |
| 54 | GND | Ground | | GND |
| 55 | NC | Floating Pin | | Floating |
| 56 | STRAP_0 | SDIO_PADVDDIO sel, XTAL sel in USB mode | VDDIO | I |
| 57 | STRAP_2 | USB_DISABLE | VDDIO | I |
| 58 | GND | Ground | | GND |
| 59 | SDIO_DATA_1 | SDIO data line 1 | VDDIO | I/O |
| 60 | SDIO_DATA_0 | SDIO data line 0 | VDDIO | I/O |
| 61 | SDIO_DATA_3 | SDIO data line 3 | VDDIO | I/O |
| 62 | SDIO_DATA_2 | SDIO data line 2 | VDDIO | I/O |
| 63 | SDIO_DATA_CMD | SDIO command line | VDDIO | I/O |
| 64 | SDIO_DATA_CLK | SDIO clock input | VDDIO | I |
| 65 | GND | Ground | | GND |
| 66 | GND | Ground | | GND |
| 67 | GND | Ground | | GND |
| 68 | GND | Ground | | GND |

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|--------|---|---------|---------|---------|------|
| VBAT | DC supply for the VBAT and PA driver supply | -0.5 | - | 5.5 | V |
| VDDIO | DC supply voltage for digital I/O | -0.5 | - | 3.9 | V |
| Tj | Maximum junction temperature | - | - | 125 | °C |

3.2 Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|--------|---|---------|---------|---------|------|
| VBAT | Power supply for Internal Regulator and FEM | 3.2 | 3.6 | 4.8 | V |
| VDDIO | DC supply voltage for digital I/O | 1.62 | 1.8/3.3 | 3.63 | V |

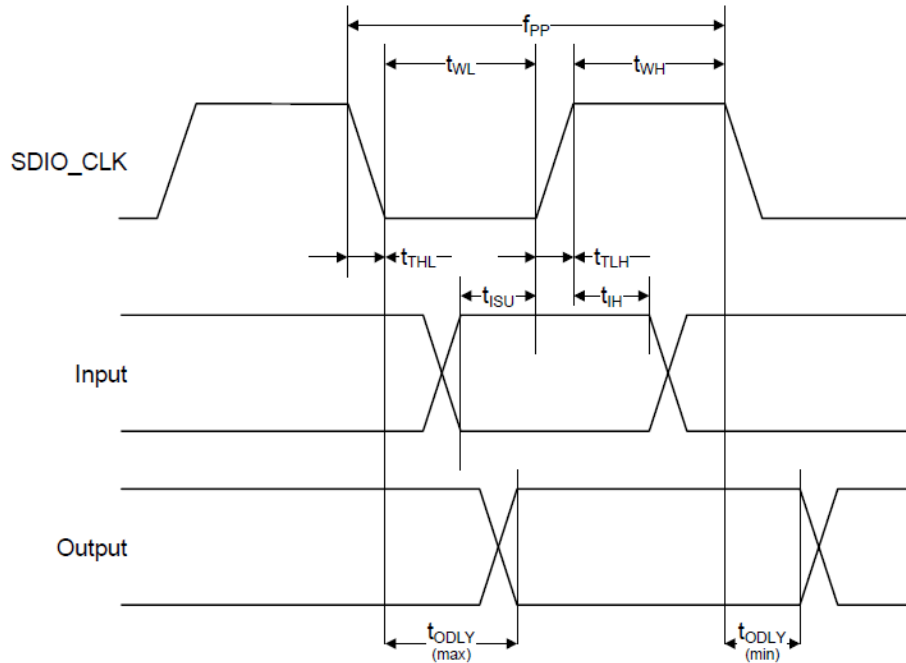
3.3 Digital IO Pin DC Characteristics

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|------------------------------|---------------------|--------------|---------|--------------|------|
| Digital I/O pins, VDDIO=1.8V | | | | | |
| V _{IH} | Input high voltage | 0.65 × VDDIO | - | - | V |
| V _{IL} | Input low voltage | - | - | 0.35 × VDDIO | V |
| V _{OH} | Output high voltage | VDDIO – 0.45 | - | - | V |
| V _{OL} | Output Low Voltage | - | - | 0.45 | V |
| Digital I/O pins, VDDIO=3.3V | | | | | |
| V _{IH} | Input high voltage | 2.00 | - | - | V |
| V _{IL} | Input low voltage | - | - | 0.80 | V |
| V _{OH} | Output high voltage | VDDIO – 0.4 | - | - | V |
| V _{OL} | Output low Voltage | - | - | 0.40 | V |

3.4 Host Interface

3.4.1 SDIO Interface

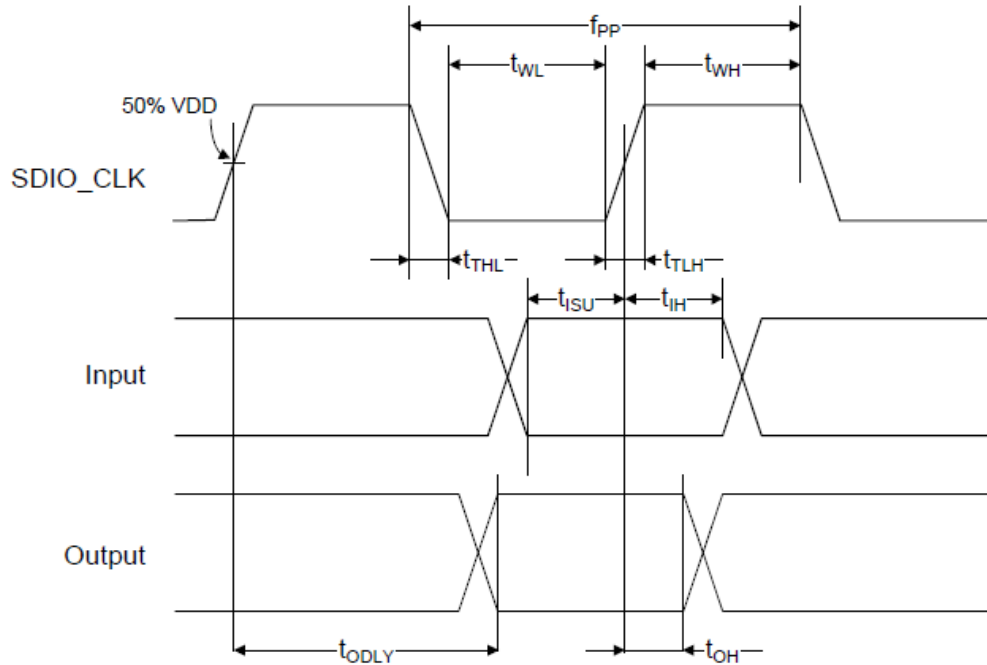
SDIO Bus Timing (Default Mode)



SDIO Bus Timing Parameters (Default Mode)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|------------|---------|---------|---------|------|
| SDIO CLK (All values are referred to minimum VIH and maximum VIL) | | | | | |
| Frequency – Data Transfer mode | f_{PP} | 0 | – | 25 | MHz |
| Frequency – Identification mode | f_{OD} | 0 | – | 400 | kHz |
| Clock low time | t_{WL} | 10 | – | – | ns |
| Clock high time | t_{WH} | 10 | – | – | ns |
| Clock rise time | t_{TLH} | – | – | 10 | ns |
| Clock low time | t_{THL} | – | – | 10 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup time | t_{ISU} | 5 | – | – | ns |
| Input hold time | t_{IH} | 5 | – | – | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time – Data Transfer mode | t_{ODLY} | 0 | – | 14 | ns |
| Output delay time – Identification mode | t_{ODLY} | 0 | – | 50 | ns |

SDIO Bus Timing (High-Speed Mode)



SDIO Bus Timing Parameters (High-Speed Mode)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|------------|---------|---------|---------|------|
| SDIO CLK (all values are referred to minimum V_{IH} and maximum V_{IL}^b) | | | | | |
| Frequency – Data Transfer Mode | f_{PP} | 0 | – | 50 | MHz |
| Frequency – Identification Mode | f_{OD} | 0 | – | 400 | kHz |
| Clock low time | t_{WL} | 7 | – | – | ns |
| Clock high time | t_{WH} | 7 | – | – | ns |
| Clock rise time | t_{TLH} | – | – | 3 | ns |
| Clock low time | t_{THL} | – | – | 3 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup Time | t_{ISU} | 6 | – | – | ns |
| Input hold Time | t_{IH} | 2 | – | – | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time – Data Transfer Mode | t_{ODLY} | – | – | 14 | ns |
| Output hold time | t_{OH} | 2.5 | – | – | ns |
| Total system capacitance (each line) | CL | – | – | 40 | pF |

3.4.2 UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth UART HCI specification: H4 and a custom Extended H4. The default baud rate is 115.2 Kbaud.

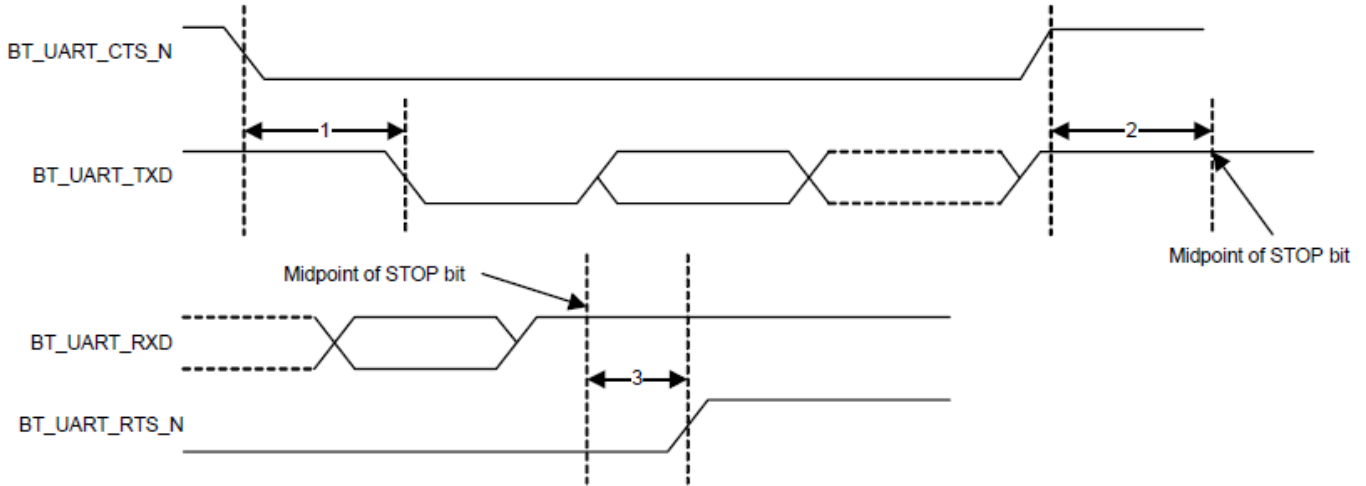
The AW-CM467S UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP).

It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-CM467S UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

UART Interface Signals

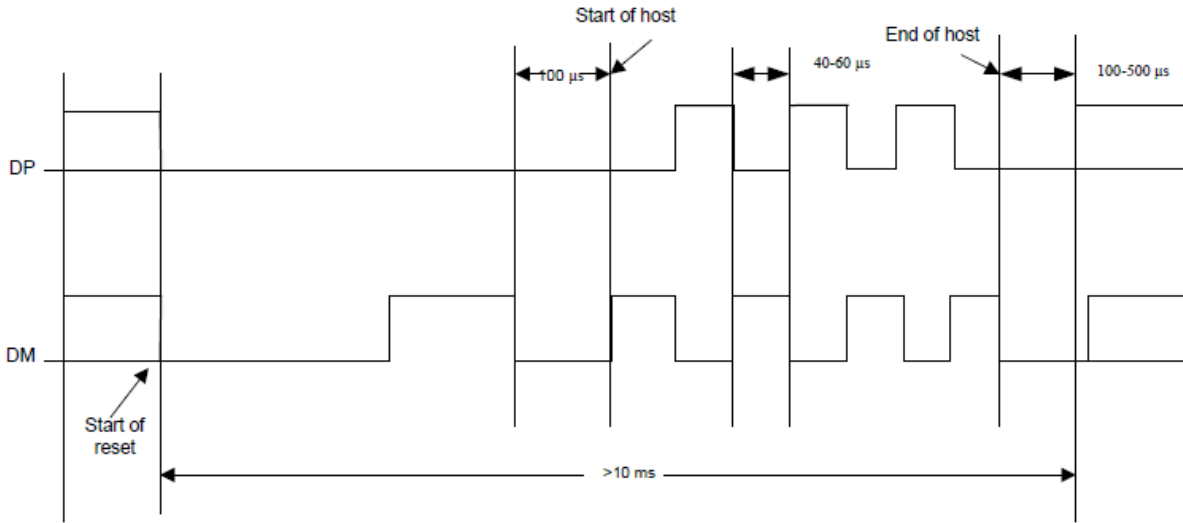
| PIN No. | Name | Description | Type |
|---------|---------------|--|------|
| 18 | BT_UART_TXD | Bluetooth UART Serial Output. Serial data output for the HCI UART Interface | O |
| 19 | BT_UART_RXD | Bluetooth UART Series Input. Serial data input for the HCI UART Interface | I |
| 21 | BT_UART_RTS_N | Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface | O |
| 17 | BT_UART_CTS_N | Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface. | I |



UART Timing

| | Reference Characteristics | Minimum | Typical | Maximum | Unit |
|---|--|---------|---------|---------|-------------|
| 1 | Delay time, BT_UART_CTS_N low to BT_UART_TXD valid | — | — | 1.5 | Bit periods |
| 2 | Setup time, BT_UART_CTS_N high before midpoint of stop bit | — | — | 0.5 | Bit periods |
| 3 | Delay time, midpoint of stop bit to BT_UART_RTS_N high | — | — | 0.5 | Bit periods |

3.4.2 WLAN/BT USB Timing



Note: The AW-CM467S has a USB2.0-PHY and HS HUB which can enable shared USB2.0 interface between WLAN and BT.

3.5 Power up Timing Sequence

The AW-CM467S has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals

■ WL_REG_ON:

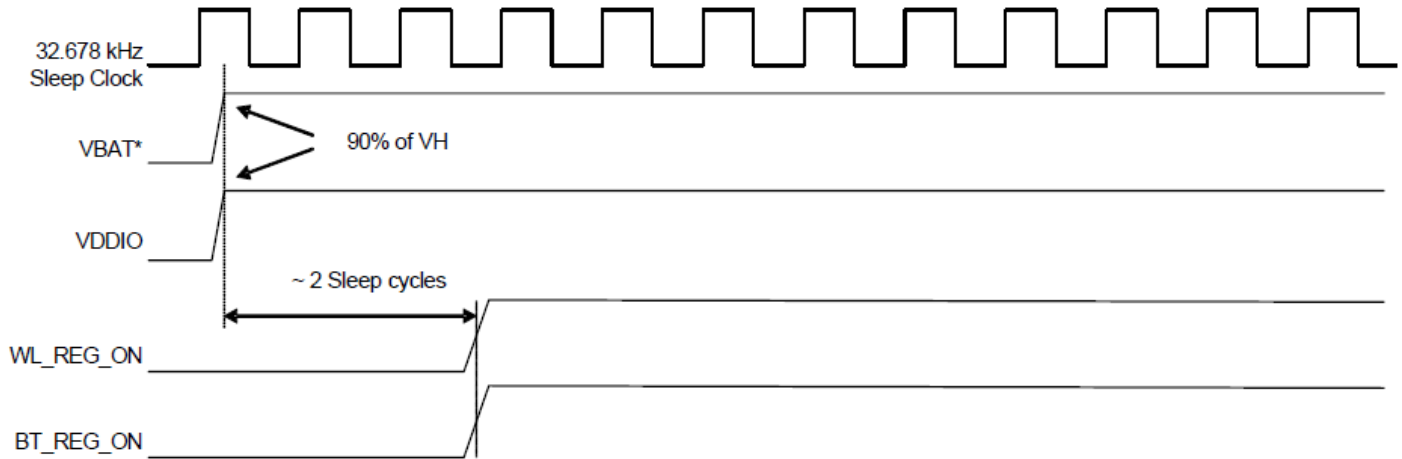
Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-CM467S regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

■ BT_REG_ON:

Used by the PMU (OR-gated with WL_REG_ON) to power up the internal AW-CM467S regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note:

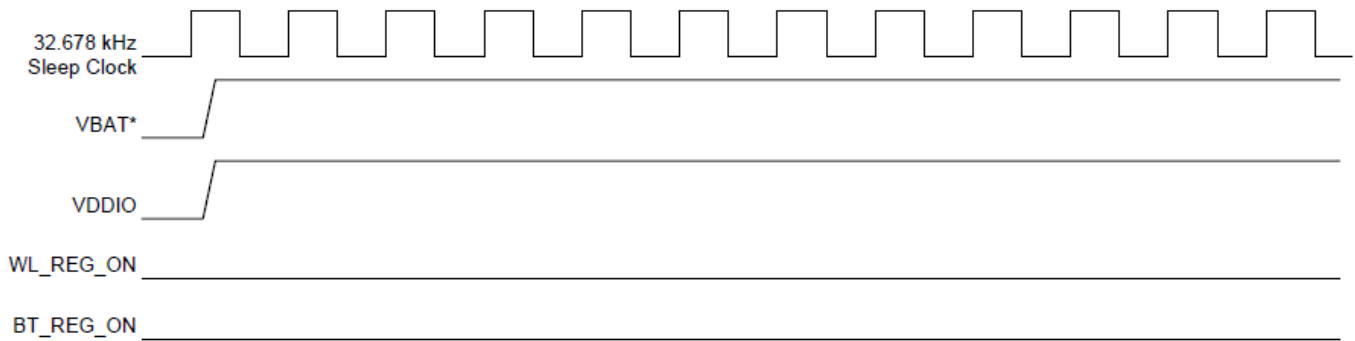
For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 msec time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.



***Notes:**

1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

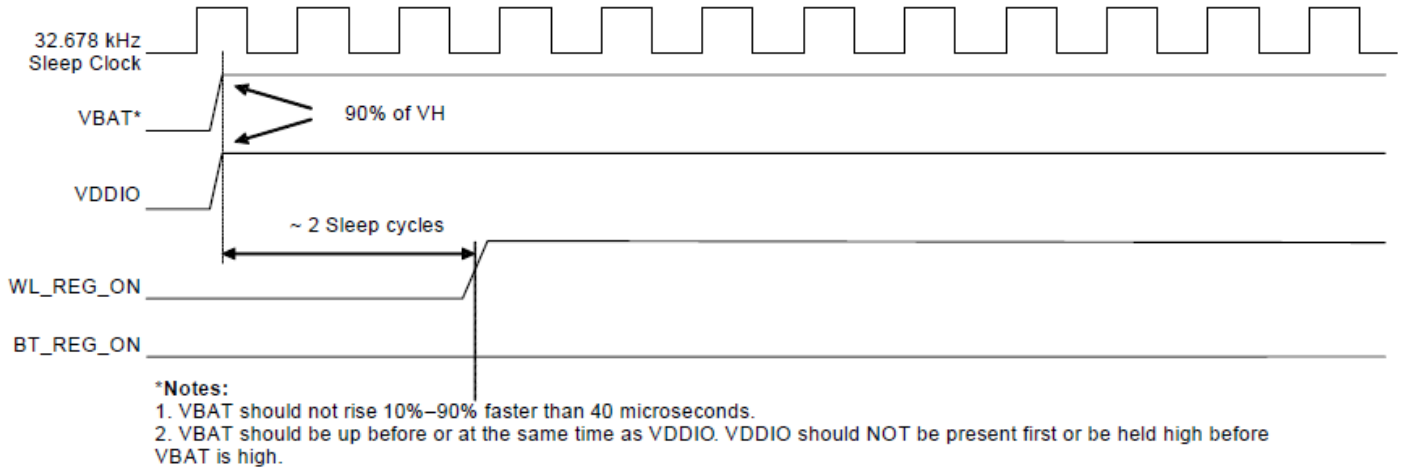
WLAN = ON, Bluetooth = ON



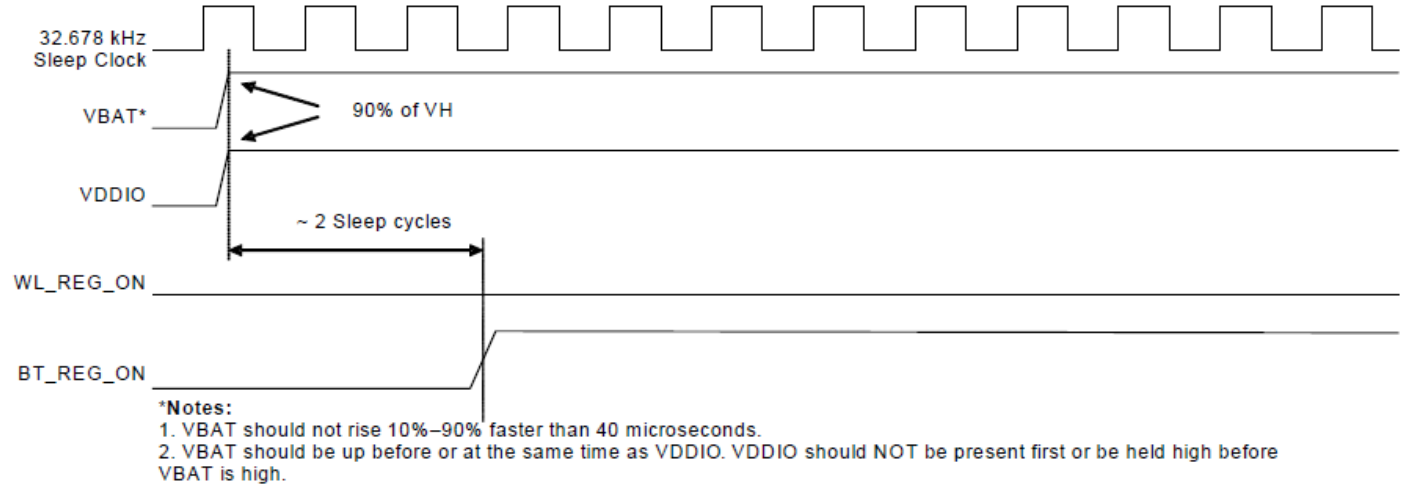
***Notes:**

1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF



WLAN = ON, Bluetooth = OFF



WLAN = OFF, Bluetooth = ON

3.6 Power Consumption*

3.6.1 WLAN

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

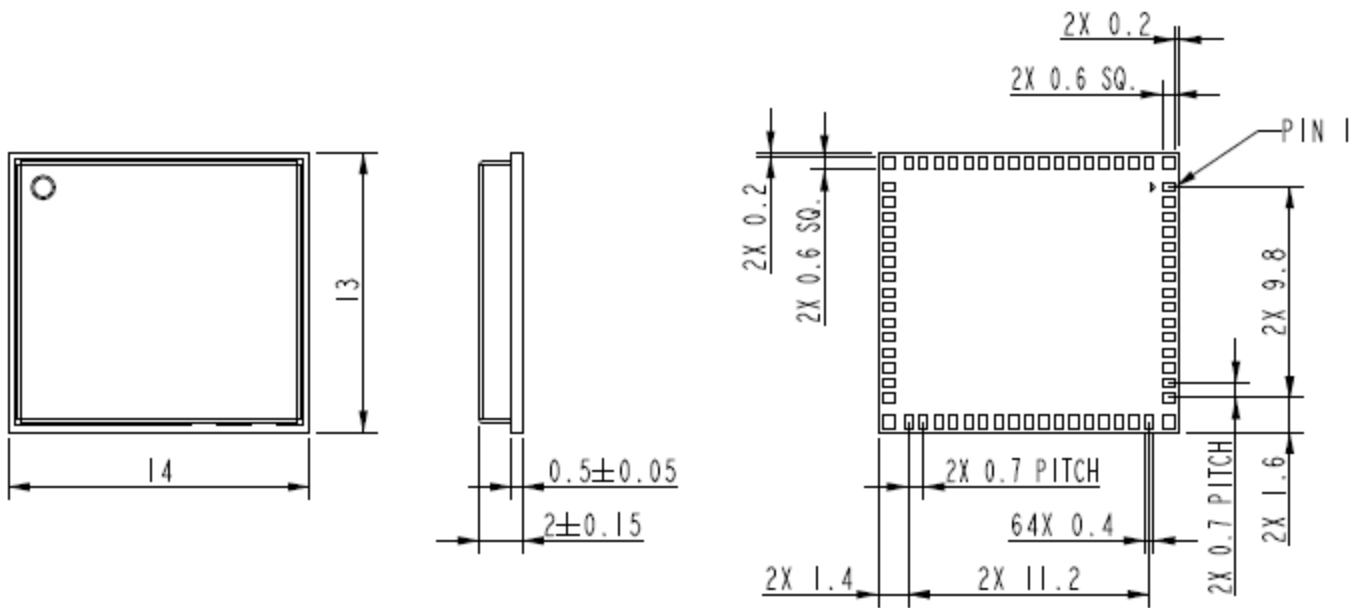
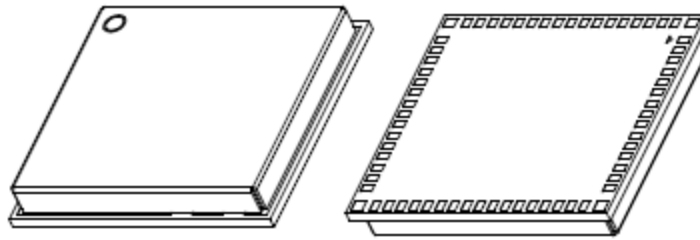
3.6.2 Bluetooth

TBD

* The power consumption is based on Azurewave test environment, these data for reference only.

4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCES UNLESS OTHERWISE SPECIFIED: ± 0.1 mm

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5. Packaging Information

TBD

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