AW-CM410

IEEE 802.11a/b/g/n/ac Wireless LAN 2T2R and Bluetooth 4.2 1T1R Combo Module

Datasheet

Rev. 0.2

(For Standard)

Revision History

Revision	*Date*	*Description*	*Initials*	*Approved*
0.1	2018/11/07	Initial release	Licheng Wang	Chihhao Liao
0.2	2019/07/15	Update 2.2 Pin Table -Add pin 15 and pin 33 Add 2.3 Host Interface Selection	Licheng Wang	Chihhao Liao

AzureWave Technologies, Inc.

Table of Contents

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced IEEE 802.11 ac/a/b/g/n 2x2 MIMO WLAN and Bluetooth M.2 combo module - AW-CM410. The module is targeted to bring the latest mobile connectivity technology to automotive infotainment, telematics, and rear-seat entertainment. The module supports 2.4GHz and 5GHz bands IEEE 802.11ac MAC/baseband/radio and Bluetooth 4.2 in IEEE 802.11ac mode. It also features an integrated Power Management Unit (PMU), Power Amplifiers (PAs), and a Low Noise Amplifier (LNA) to address the needs of mobile devices that require minimal power consumption and compact size. By using AW-CM410, implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms that ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. Coexistence support for external radios (such as LTE cellular and GPS) is provided via an external interface. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on an automotive systems is achieved.

For the WLAN operation, the AW-CM410 uses DSSS, OFDM, DBPSK, DQPSK, CCK and QAM baseband modulation technologies. In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 867 Mbps. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CM410. In addition to the support of WPA/WPA2 (personal) and WEP encryption, the AW-CM410 also supports the IEEE 802.11i security standard through AES and TKIP acceleration hardware for faster data encryption.

For Bluetooth operation, the AW-CM410 is Bluetooth 4.2. The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability. The AW-CM410 supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets, and Adaptive Frequency Hopping (AFH) for reducing radio frequency interference. It incorporates all Bluetooth 4.0 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume.

1.2 Features

- Integrates CYPRESS solutions of CYW88359 Wi-Fi /BT Single Chip
- With LTE coexistence filter support
- Multiple power saving modes for low power consumption
- Lead-free /Halogen Free Design
- 16.6 mm(L) x 15 mm(W) x 2.25mm(H) 108 pin LGA package

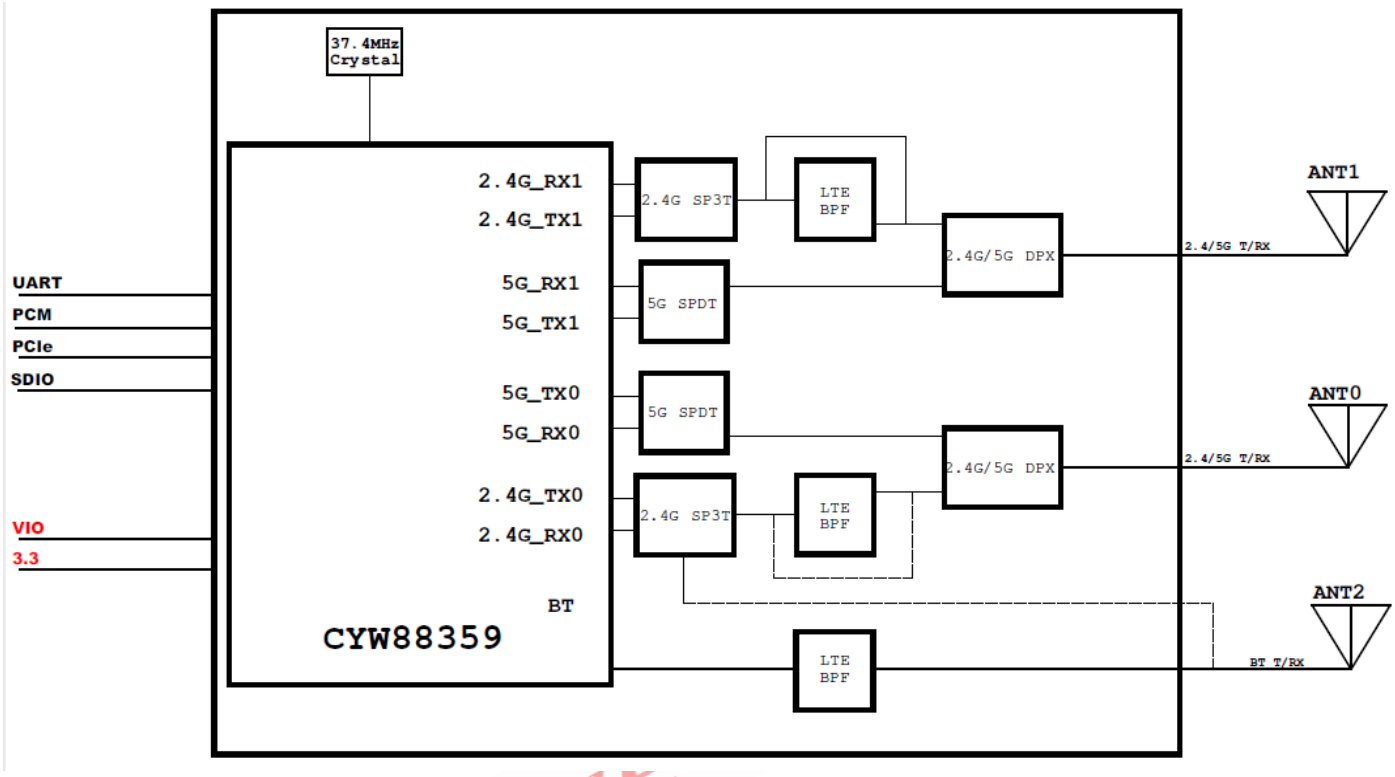
1.2.1 WLAN

- IEEE 802.11ac Draft compliant
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance
- IEEE 802.11ac 2x2 MIMO supports for 20, 40, and 80 MHz channels with optional SGI (256QAM modulation) provides data rates up to 866.7 Mbps.
- Tx and Rx low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE 802.11ac/n beamforming
- Supports real simultaneous dual-band (RSDB).
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE and GPS.
- PCIe mode complies with PCI Express base specification revision 3.0 for ×1 lane and power management running at Gen1 speeds.
- WLAN host interface options: SDIO and PCIe
- Security:
  1. WPA, WAPI STA, and WPA2 (Personal) support for powerful encryption and authentication.
  2. AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  3. Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Integrated ARM® Cortex ® R4 processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features.

1.2.2 Bluetooth

- Complies with Bluetooth Core Specification Version 4.2 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high speed UART interface and PCM for audio data.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.

1.3 Block Diagram



1.4 Specifications Table

1.4.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac Wireless LAN and Bluetooth Combo Module
Major Chipset	CYPRESS CYW88359
Host Interface	WLAN: SDIO and PCIe Bluetooth: UART/PCM
Dimension	16.6mm(L) x 15mm(W) x 2.25mm(H) (Typical)
Package	LGA
Antenna	Ant 0: WiFi Main Ant 1: WIFI AUX Ant 2: BT AUX
Weight	TBD

1.4.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant
WLAN SVID/SPID	TBD
Frequency Rage	WLAN: 2.4 GHz / 5GHz Band
Frequency Accuracy over Temperature	+-20 ppm
Modulation	● DSSS: DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps) ● OFDM: BPSK(9/6Mbps/MCS0), QPSK(18/12Mbps/MCS1~2), 16-QAM(36/24Mbps/MCS3~4), 64-QAM(72.2/54/48Mbps/MCS5~7), 256-QAM(MCS8~9)
Number of Channels	802.11b: ● USA, Canada and Taiwan – 1 ~ 13 ● Most European Countries – 1 ~ 13 ● Japan – 1 ~ 13 802.11g: ● USA and Canada – 1 ~ 13 ● Most European Countries – 1 ~ 13 802.11n: ● USA and Canada – 1 ~ 13 ● Most European Countries – 1 ~ 13

802.11a:

- USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

Output Power (Board Level Limit)*

2.4G
SISO

	Min	Typ	Max	Unit
11b (1Mbps) @EVM<8%		TBD		dBm
11b (1Mbps) @EVM<11%		TBD		dBm
11g (6Mbps) @EVM≦-14 dB		TBD		dBm
11g (54Mbps) @EVM≦-28 dB		TBD		dBm
11n (HT20 MCS0) @EVM≦-16 dB		TBD		dBm
11n (HT20 MCS7) @EVM≦-30 dB		TBD		dBm

MIMO

11n (HT20 MCS8) @EVM≦-16 dB		TBD		dBm
11n (HT20 MCS15) @EVM≦-30 dB		TBD		dBm

5G
SISO

	Min	Typ	Max	Unit
11a (6Mbps) @EVM≦-14 dB		TBD		dBm
11a (54Mbps) @EVM≦-28 dB		TBD		dBm
11n (HT20 MCS0) @EVM≦-16 dB		TBD		dBm
11n (HT20 MCS7) @EVM≦-30 dB		TBD		dBm
11n (HT40 MCS0) @EVM≦-16 dB		TBD		dBm
11n (HT40 MCS7) @EVM≦-30 dB		TBD		dBm
11ac (VHT80 MCS0) @EVM≦-16 dB		TBD		dBm
11ac (VHT80 MCS9)		TBD		dBm

@EVM≦-34 dB				

MIMO:

	Min	Typ	Max	Unit
11n (HT20 MCS8) @EVM≦-16 dB		TBD		dBm
11n (HT20 MCS15) @EVM≦-30 dB		TBD		dBm
11n (HT40 MCS8) @EVM≦-16 dB		TBD		dBm
11n (HT40 MCS15) @EVM≦-30 dB		TBD		dBm
11ac (VHT80 MCS0) @EVM≦-16 dB		TBD		dBm
11ac (VHT80 MCS9) @EVM≦-34 dB		TBD		dBm

Receiver Sensitivity

2.4G
(SISO)

	Min	Typ	Max	Unit
11b (1Mbps)		TBD		dBm
11b (11Mbps)		TBD		dBm
11g (6Mbps)		TBD		dBm
11g (54Mbps)		TBD		dBm
11n (HT20 MCS0)		TBD		dBm
11n (HT20 MCS7)		TBD		dBm

(MIMO)

	Min	Typ	Max	Unit
11n (HT20 MCS8)		TBD		dBm
11n (HT20 MCS15)		TBD		dBm

5G
(SISO)

	Min	Typ	Max	Unit
11a (6Mbps)		TBD		dBm
11a (54Mbps)		TBD		dBm
11n (HT20 MCS0)		TBD		dBm
11n (HT20 MCS7)		TBD		dBm
11n (HT40 MCS0)		TBD		dBm
11n (HT40 MCS7)		TBD		dBm
11ac (VHT80 MCS0)		TBD		dBm
11ac (VHT80 MCS9)		TBD		dBm

(MIMO)

	Min	Typ	Max	Unit
11n (HT20 MCS8)		TBD		dBm
11n (HT20 MCS15)		TBD		dBm
11n (HT40 MCS8)		TBD		dBm
11n (HT40 MCS15)		TBD		dBm
11ac (VHT80 MCS0)		TBD		dBm
11ac (VHT80 MCS9)		TBD		dBm

Data Rate

- 802.11b: 1, 2, 5.5, 11Mbps
- 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- 802.11n: MCS0~7 HT20/HT40
- 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- 802.11ac: MCS0~8 VHT20
- 802.11ac: MCS0~9 VHT40/VHT80

Security	● WPA™- and WPA2™- (Personal) support for powerful encryption and authentication ● AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility ● Wi-Fi Protected Setup (WPS)

* If you have any certification questions about output power please contact FAE directly.

1.4.3 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth 2.1+Enhanced Data Rate (EDR) / BT4.2
Bluetooth VID/PID	TBD
Frequency Rage	2400~2483.5MHz
Modulation	GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)
Output Power	
Receiver Sensitivity	BT Sensitivity

Output Power

	Min	Typ	Max	Unit
BR		TBD		dBm
EDR(2M)		TBD		dBm
EDR(3M)		TBD		dBm
Low Energy		TBD		dBm

Receiver Sensitivity

	Min	Typ	Max	Unit
BR		TBD		dBm
EDR(2M)		TBD		dBm
EDR(3M)		TBD		dBm
Low Energy		TBD		dBm

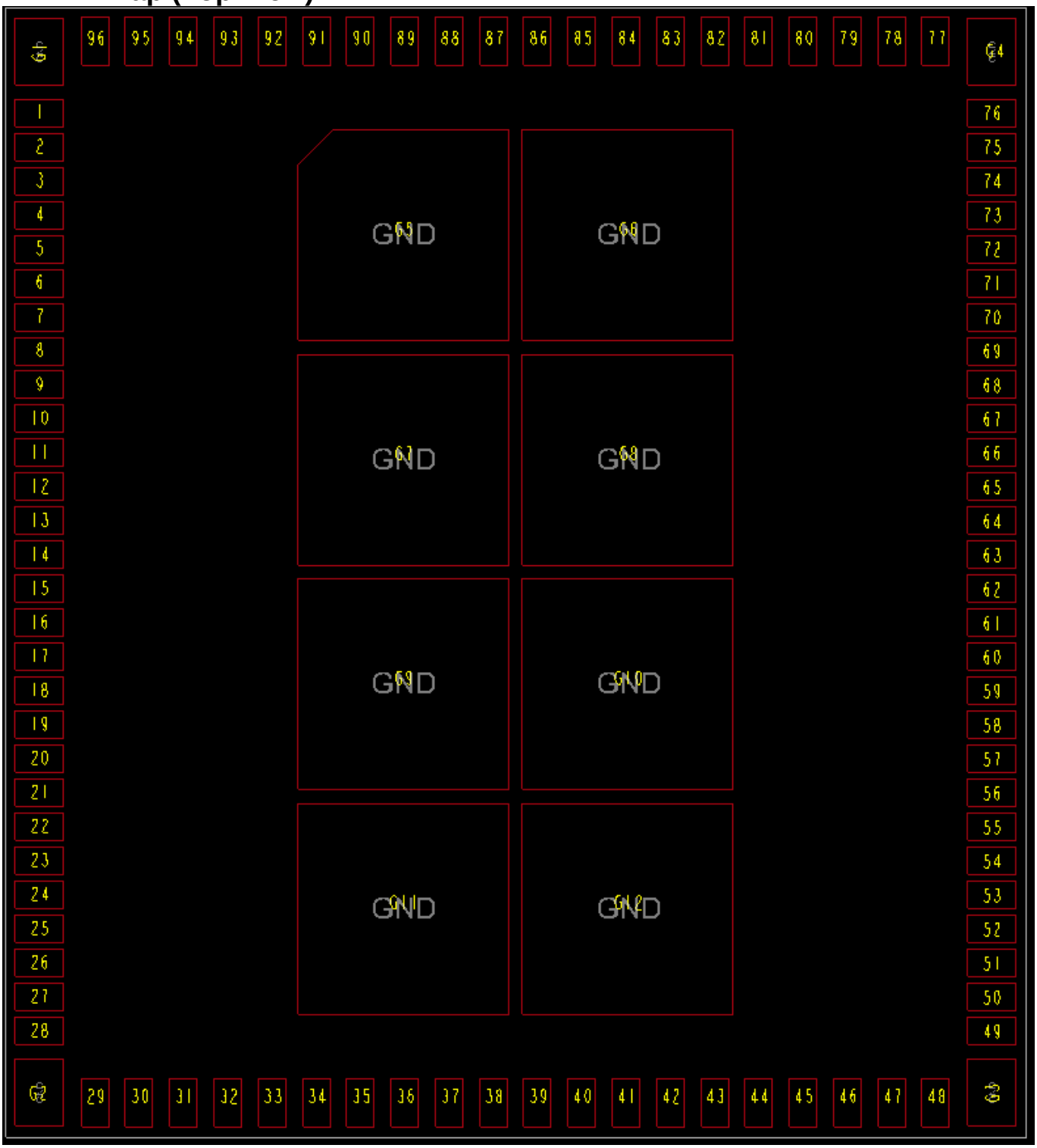
1.4.4 Operating Conditions

Features	Description
Operating Conditions	
Voltage	Power supply for host:3.3V
Operating Temperature	0~80°C
Operating Humidity	<85% (non condensing)
Storage Temperature	-40~125°C
Storage Humidity	<60 % (non condensing)
ESD Protection	

Human Body Model	1 KV
Changed Device Model	250 V

2. Pin Definition

2.1 Pin Map (Top View)



2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	BT_DEV_WAKE	Bluetooth DEV_WAKE.	VIO	I/O
2	CLK_REQ	Reference clock request (shared by BT and WLAN). If not used, this can be no-connect.	VIO	I/O
3	EXT_LPO	External sleep clock input (32.768 kHz).	VIO	I/O
4	GND	Ground.		GND
5	GPIO_2	GPIO	VIO	I/O
6	GPIO_3	GPIO	VIO	I/O
7	GPIO_1_ WL_DEV_WAKE	WLAN DEV_WAKE.	VIO	I/O
8	GPIO_5	GPIO	VIO	I/O
9	GPIO_0_ WL_HOST_WAKE	WLAN HOST_WAKE.	VIO	I/O
10	GPIO_4	GPIO	VIO	I/O
11	GPIO_6	GPIO	VIO	I/O
12	GPIO_7	GPIO	VIO	I/O
13	GND	Ground.		GND
14	NC	Floating Pin , No connect to anything.		Floating
15	GPIO_18_SDIO_DISABLE	SDIO_DISABLE: 0 = SDIO enabled, 1 = SDIO disabled; either PCIe or SDIO or both have to be present.	VIO	I
16	NC	Floating Pin , No connect to anything.		Floating
17	GPIO_17_SDIO_PADVDDIO	Select for I/O voltage: 0 = 3.3V, 1 = 1.8V.	VIO	I
18	GND	Ground.		GND
19	PCIE_WAKEn	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.	VIO	OD
20	PCIE_PERST_L	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1. PCIE_PERST_L pad excludes internal pull-up.	VIO	I
21	PCIE_CLKREQ_L	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.	VIO	OD
22	GND	Ground.		GND
23	PCIE_RDP	Receiver differential pair (×1 lane).	VIO	I
24	PCIE_RDN	Receiver differential pair (×1 lane).	VIO	I
25	GND	Ground.		GND
26	PCIE_REFCLK_P	PCIE Differential Clock inputs (negative and positive). 100 MHz differential	VIO	I

27	PCIE_REFCLK_N	PCIE Differential Clock inputs (negative and positive). 100 MHz differential	VIO	I
28	GND	Ground.		GND
29	GND	Ground.		GND
30	PCIE_TDN	Transmitter differential pair (×1 lane).	VIO	O
31	PCIE_TDP	Transmitter differential pair (×1 lane).	VIO	O
32	GND	Ground.		GND
33	GPIO_19_PCIE_ENABLE	PCIE_ENABLE: 0 = PCIe disabled, 1 = PCIe enabled; either PCIe or SDIO or both have to be present.	VIO	I
34	WL_REG_ON	Used by PMU to power up or power down the internal AW-CM410 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.	VIO	I
35	GND	Ground.		GND
36	SDIO_CMD	SDIO command line	VIO	I/O
37	GND	Ground.		GND
38	SDIO_CLK	SDIO Clock input	VIO	I
39	SDIO_DATA_3	SDIO data line 3.	VIO	I/O
40	SDIO_DATA_2	SDIO data line 2.	VIO	I/O
41	SDIO_DATA_1	SDIO data line 1.	VIO	I/O
42	SDIO_DATA_0	SDIO data line 0.	VIO	I/O
43	GND	Ground.		GND
44	GND	Ground.		GND
45	BT_PCM_SYNC	PCM synchronous data output, connected to PCM_IN on the host.		Out
46	BT_PCM_IN	PCM Clock		I/O
47	BT_PCM_OUT	PCM synchronous data input, connected to PCM_OUT on the host.		IN
48	BT_PCM_CLK	PCM synchronous data SYNC		I/O
49	VIO	VDDIO power supply. Can be select as 1.8V/3.3V	1.8V/3.3V	VIO
50	GND	Ground.		GND
51	3.3V	3.3V power supply	3.3V	VCC
52	3.3V	3.3V power supply	3.3V	VCC
53	3.3V	3.3V power supply	3.3V	VCC
54	GND	Ground.		GND
55	BT_REG_ON	Used by PMU to power up or power down the internal AW-CM410 regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through	VIO	I

		programming.		
56	GND	Ground.		GND
57	BT_RF_CORE0	BT RF TX/RX path. (ANT2)		RF
58	GND	Ground.		GND
59	BT_HOST_WAKE	Bluetooth HOST_WAKE.		
60	BT_UART_CTS	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	VIO	I
61	BT_UART_TXD	UART serial output. Serial data output for the HCI UART interface.	VIO	O
62	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	VIO	I
63	BT_UART_RTS	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.	VIO	O
64	GND	Ground.		GND
65	BT_IN	Connect with BT_RF_CORE0 or floating.	RF	GND
66	GND	Ground.		GND
67	GND	Ground.		GND
68	GND	Ground.		GND
69	GND	Ground.		GND
70	GND	Ground.		GND
71	GND	Ground.		GND
72	GND	Ground.		GND
73	GND	Ground.		GND
74	GND	Ground.		GND
75	GND	Ground.		GND
76	GND	Ground.		GND
77	GND	Ground.		GND
78	RF_CORE0_OUT	WLAN RF TX/RX path.(ANT0)		RF
79	GND	Ground.		GND
80	GND	Ground.		GND
81	GND	Ground.		GND
82	GND	Ground.		GND
83	GND	Ground.		GND
84	GND	Ground.		GND
85	GND	Ground.		GND
86	GND	Ground.		GND
87	GND	Ground.		GND
88	GND	Ground.		GND
89	GND	Ground.		GND

90	GND	Ground.		GND
91	GND	Ground.		GND
92	GND	Ground.		GND
93	GND	Ground.		GND
94	GND	Ground.		GND
95	RF_CORE1_OUT	WLAN RF TX/RX path.(ANT1)		RF
96	GND	Ground.		GND
G1	G1	Ground.		GND
G2	G2	Ground.		GND
G3	G3	Ground.		GND
G4	G4	Ground.		GND
G5	G5	Ground.		GND
G6	G6	Ground.		GND
G7	G7	Ground.		GND
G8	G8	Ground.		GND
G9	G9	Ground.		GND
G10	G10	Ground.		GND
G11	G11	Ground.		GND
G12	G12	Ground.		GND

2.3 Host Interface Selection

Note: The strapping options are defined in such a way that defaults have internal pull-ups, so that it is easy to configure the strap value in opposite manner on a board (put a pull-down on the board). To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

PCIe Enable	SDIO Disable	SDIO PADVDDIO/ SPROM Absent	Mode
1	1	1	PCIe; VIO can be 3.3/1.8
1	1	0	PCIe + SPROM; VIO can be 3.3/1.8V
0	0	1	1.8V SDIO; Connect VIO to 1.8V
0	0	0	3.3V SDIO; Connect VIO to 3.3V

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	DC supply for VBAT , PA driver supply and digital I/O	-0.5		6	V
VIO	DC supply voltage for digital I/O	-0.5		3.9	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3.3V	Power supply for Internal Regulators	3	3.3	3.6	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
SDIO Interface I/O Pins						
V_{IH}	Input high voltage (V_{DDIO})	VDDIO=1.8V	1.27	-	-	V
V_{IL}	Input low voltage (V_{DDIO})	VDDIO=1.8V	-	-	0.58	V
V_{OH}	Output High Voltage @ 2mA	VDDIO=1.8V	1.4	-	-	V
V_{OL}	Output Low Voltage @ 2mA	VDDIO=1.8V	-	-	0.45	V
V_{IH}	Input high voltage (V_{DDIO})	VDDIO=3.3V	0.625xVDDIO	-	-	V
V_{IL}	Input low voltage (V_{DDIO})	VDDIO=3.3V	-	-	0.25xVDDIO	V
V_{OH}	Output High Voltage @ 2mA	VDDIO=3.3V	0.75xVDDIO	-	-	V
V_{OL}	Output Low Voltage @ 2mA	VDDIO=3.3V	-	-	0.125xVDDIO	V
Other Digital I/O pins						
V_{IH}	Input high voltage (V_{DDIO})	VDDIO=1.8V	0.65xVDDIO	-	-	V
V_{IL}	Input low voltage (V_{DDIO})	VDDIO=1.8V	-	-	0.35xVDDIO	V
V_{OH}	Output High Voltage @ 2mA	VDDIO=1.8V	VDDIO-0.45	-	-	V
V_{OL}	Output Low Voltage @ 2mA	VDDIO=1.8V	-	-	0.45	V
VIH	Input high voltage (VDDIO)	VDDIO=3.3V	2	-	-	V
VIL	Input low voltage (VDDIO)	VDDIO=3.3V	-	-	0.8	V

VOH	Output High Voltage @ 2mA	VDDIO=3.3V	VDDIO-0.4	-	-	V
VOL	Output Low Voltage @ 2mA	VDDIO=3.3V	-	-	0.4	V

3.4 Power up Timing Sequence

3.4.1 Sequencing of Reset and Regulator Control Signals

The AW-CM410 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.
Note:

- The AW-CM410 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO and PCIe accesses.

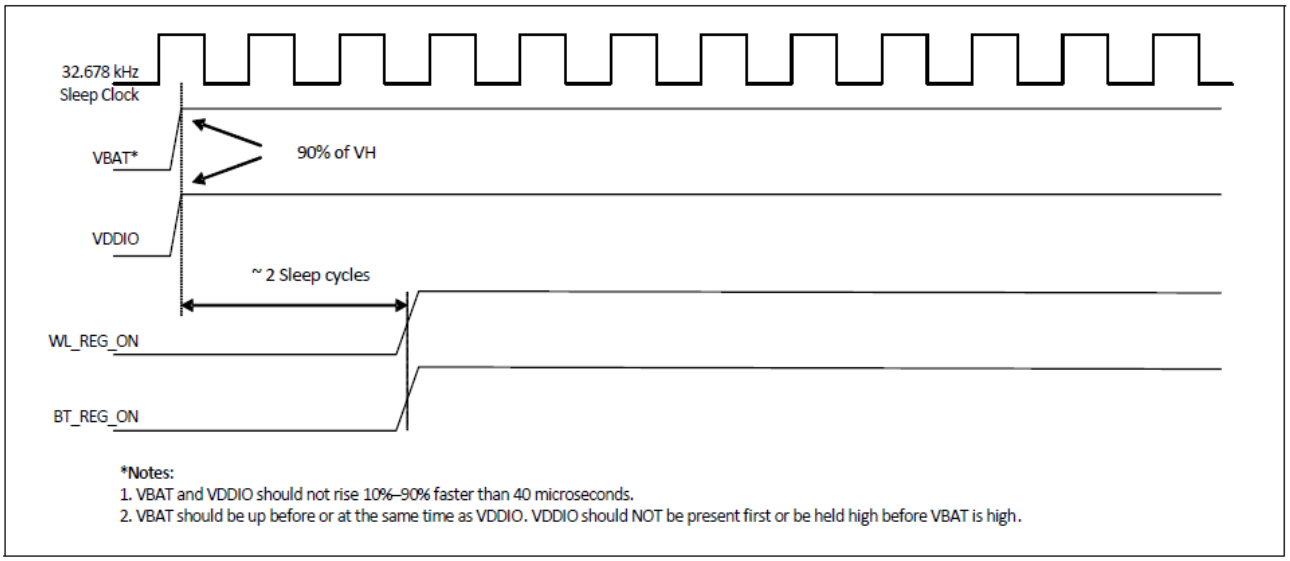
3.4.2 Description of Control Signals

The AW-CM410 has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption

1. WL_REG_ON: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal AW-CM410 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
2. BT_REG_ON: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW8x359 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

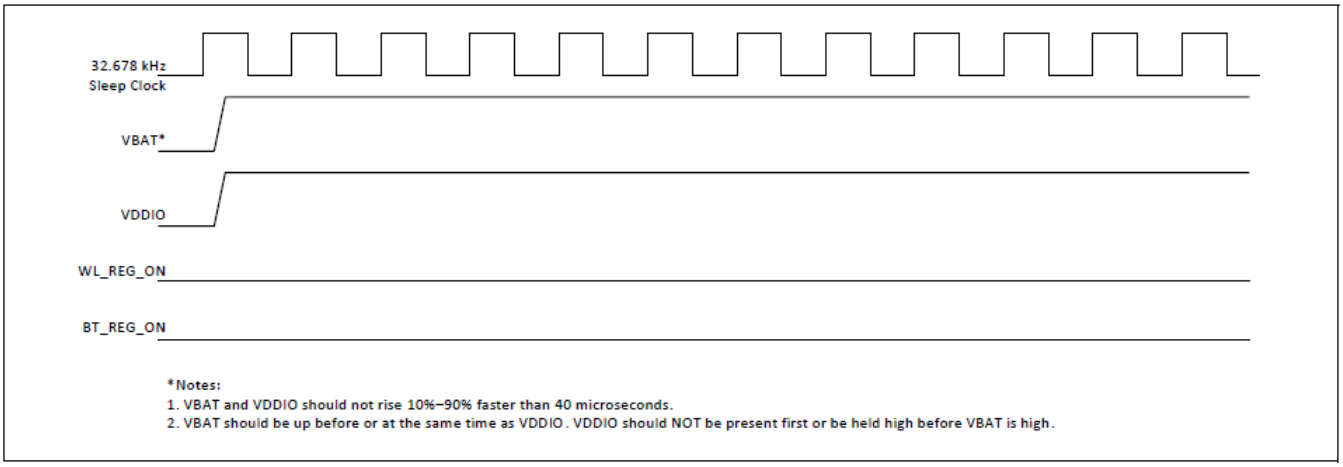
3.4.3 Control Signal Timing Diagrams

WLAN = ON, Bluetooth = ON



*Notes:
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF



*Notes:
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF

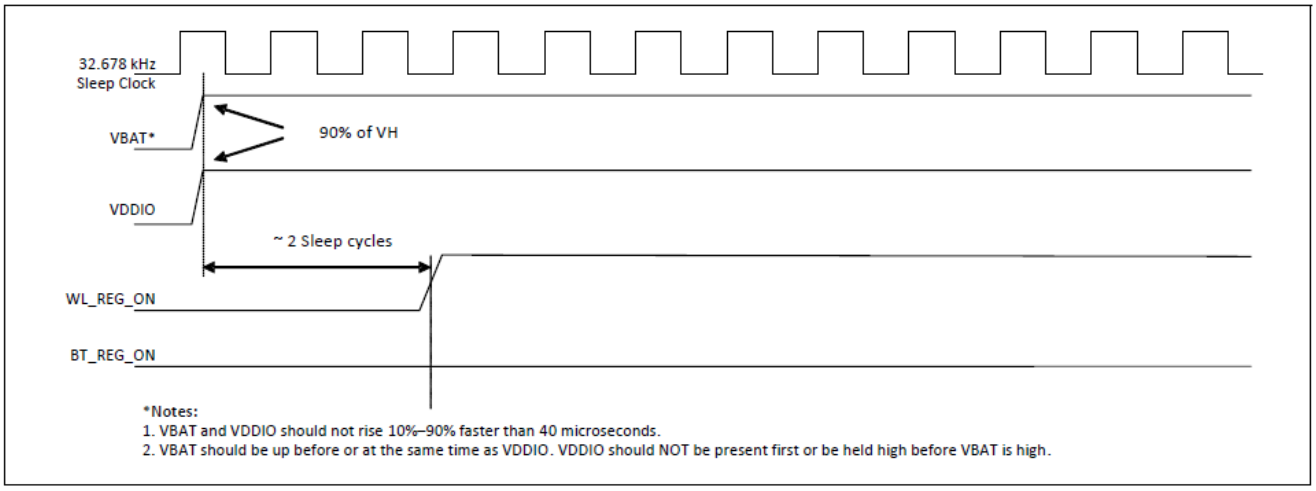
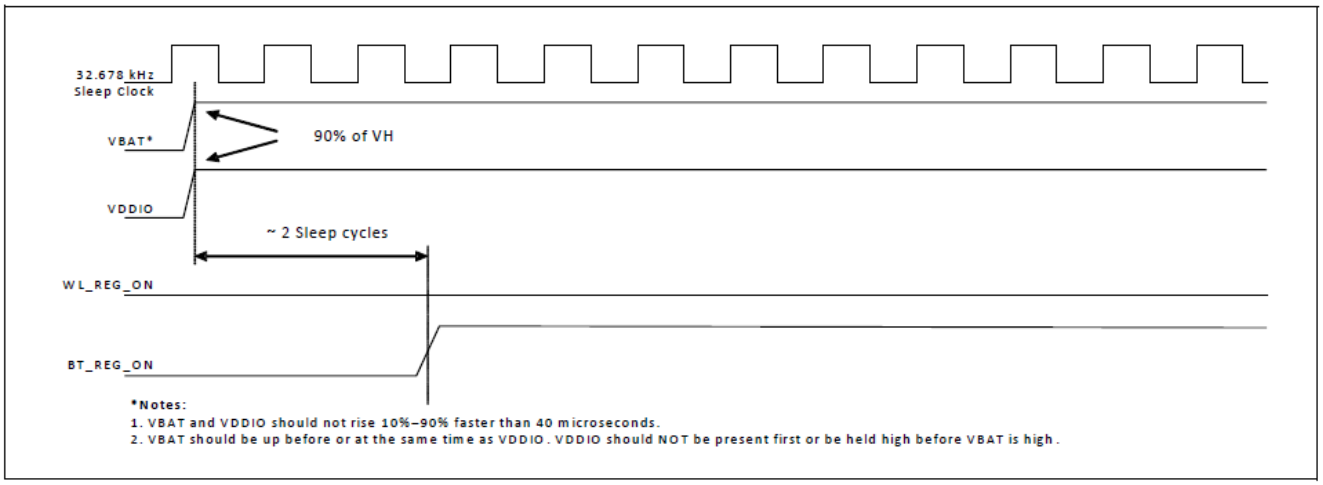


Figure 44. WLAN = OFF, Bluetooth = ON



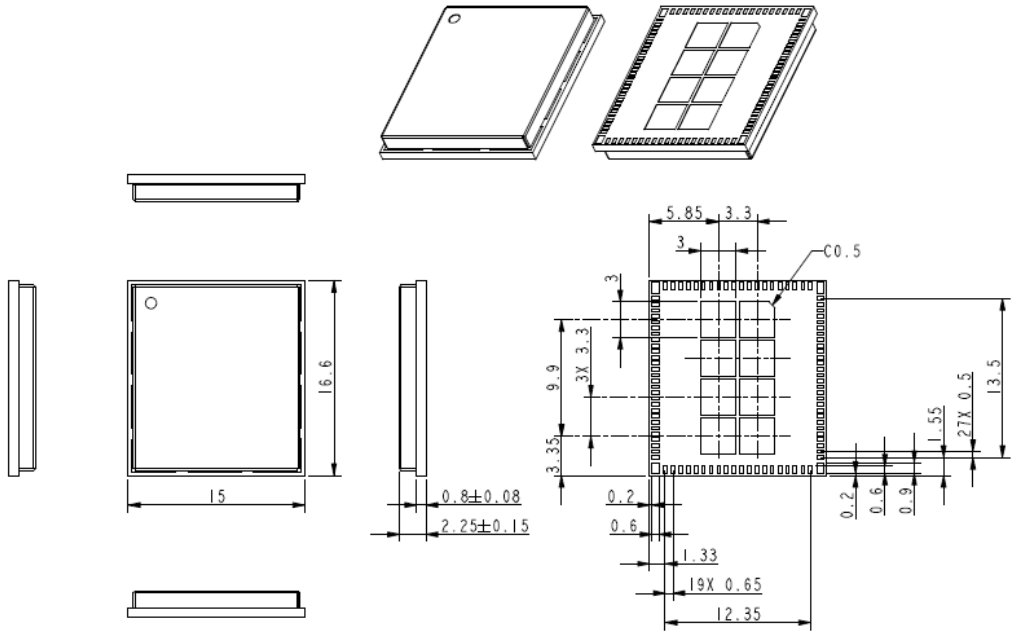
3.5 Power Consumption*

3.5.1 WLAN
TBD

3.5.2 Bluetooth
TBD

4. Mechanical Information

4.1 Mechanical Drawing



TOLERANCES UNLESS OTHERWISE SPECIFIED:±0.1mm

AzureWave					MODEL NO. 2410		DESCRIPTION OUTLINE DRAWING					DOCUMENT LEVEL CONFIDENTIAL	APPROVAL
DIM.	0~80	80~180	180~315	315~800	PART NO.	DRAWING NO.	MATERIAL	UNIT	SCALE	REV	PAGE	DATE	DESIGNED
TOL.	±0.1	±0.15	±0.20	±0.25		R2-2410-COD-01_A		mm	1/1	A	1/1	2018/10/09	STEVE CHANG

5. Packaging Information

TBD