AW-CH303-H

IEEE 802.11 1x1 a/b/g/n/ac WLAN with Bluetooth 5.0 LGA SIP Module

Datasheet

Rev. B

DF

(For VIO3.3V)

Features

WLAN

- High speed wireless connection up to 433.3Mbps transmit/receive PHY rate using 80MHz bandwidth
- 1 antennas to support 1(Transmit) × 1(Receive) technology and Bluetooth
- WCS (Wireless Coexistence System)
- Low power consumption and high performance
- Enhanced wireless security
- Fully speed operation with Piconet and Scatternet support
- 7.9mm(L) x 7.3mm(W) x1.1mm(H) LGA package
- Dual - band 2.4 GHz and 5GHz 802.11 a/b/g/n/ac

Bluetooth

- 1 antennas to support 1(Transmit) × 1(Receive) technology and Bluetooth
- Compliant Bluetooth BT5.0
- Enhanced Data Rate(EDR) compliant for both 2Mbps and 3Mbps supported
- High speed UART and PCM for Bluetooth

AzureWave Technologies, Inc.

Revision History

Document NO: R2-1303-DST-02

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/01/08	DCN016583	● Initial Version	Licheng Wang	Chihhao Liao
B	2020/02/18	DCN016742	● Modify VIO voltage level ● Modify Power Consumption	Licheng Wang	Chihhao Liao

Table of Contents

Features 2
Revision History 3
Table of Contents 4
1. Introduction 5
1.1 Product Overview 5
1.2 Block Diagram 6
1.3 Specifications Table 7
1.3.1 General 7
1.3.2 WLAN 7
1.3.3 Bluetooth 9
1.3.4 Operating Conditions 10
2. Pin Definition 11
2.1 Pin Map 11
2.2 Pin Table 12
3. Electrical Characteristics 15
3.1 Absolute Maximum Ratings 15
3.2 Recommended Operating Conditions 15
3.3 Digital IO Pin DC Characteristics 15
3.4 Interface 16
3.4.1 SDIO Host Interface Specification 19
3.4.2 UART Interface 20
3.5 Power Consumption* 22
3.5.1 WLAN 22
3.5.2 Bluetooth 23
4. Mechanical Information 25
4.1 Mechanical Drawing 25
5. Packaging Information 26

1. Introduction

1.1 Product Overview

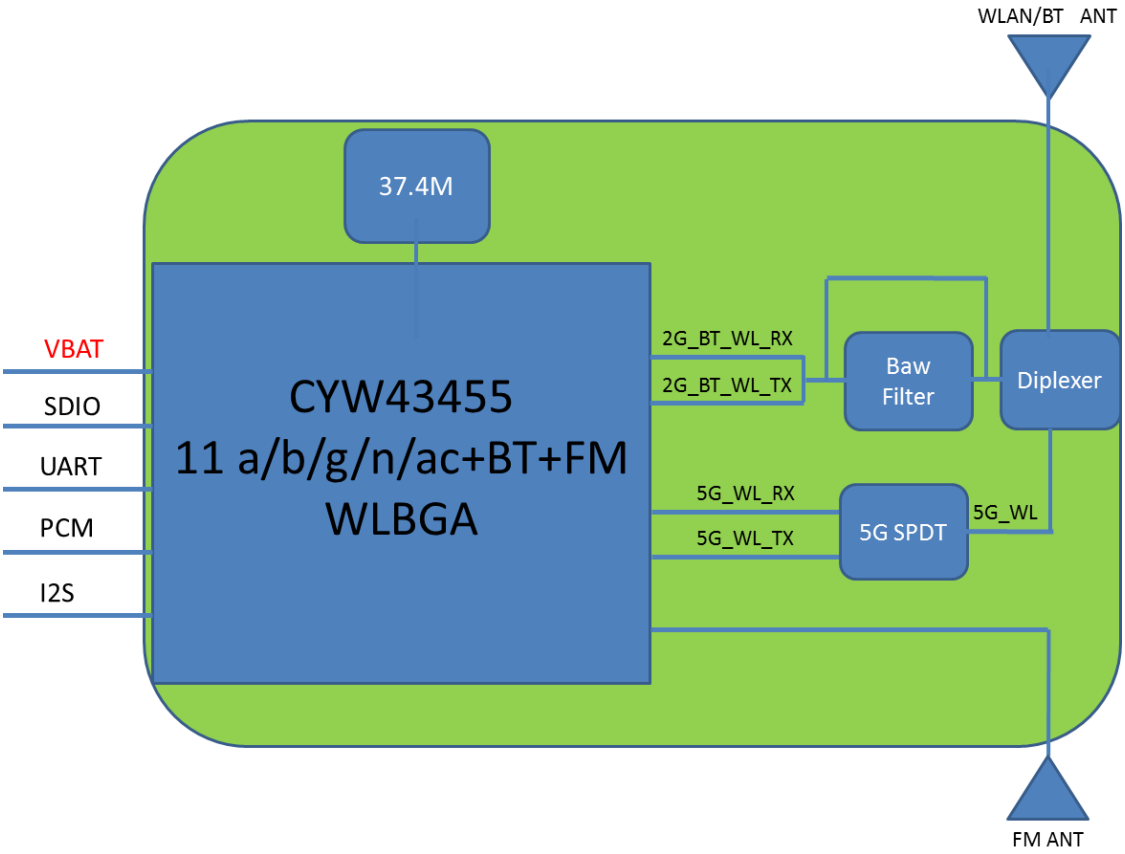
AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.11 a/b/g/n/ac WIFI with BT 5.0 combo SDIO and UART combo SIP Module --- AW-CH303-H. The AW-CH303-H IEEE 802.11 a/b/g/n/ac WIFI with BT 5.0 combo SIP module is a highly integrated wireless local area network (WLAN) solution to let users enjoy the digital content through the latest wireless technology without using the extra cables and cords. It combines with Bluetooth 5.0 and provides a complete 2.4GHz Bluetooth system which is fully compliant to BT 5.0 and v2.1 that supports EDR of 2Mbps and 3Mbps for data and audio communications. It enables a high performance, cost effective, low power, compact solution that easily fits onto the SDIO and UART combo SIP module.

Compliant with the IEEE 802.11a/b/g/n/ac standard, AW-CH303 uses Direct Sequence Spread Spectrum (DSSS), Orthogonal Frequency Division Multiplexing (OFDM), BPSK, QPSK, CCK and QAM baseband modulation technologies.

Compare to 802.11n technology, 802.11ac standard makes big improvement on speed and range.

AW-CH303 SIP module adopts Cypress solution. The module design is based on the Cypress CYW43455 single chip.

1.2 Block Diagram



1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11 a/b/g/n/ac Wi-Fi with BT5.0 combo SiP module
Major Chipset	CYW43455
Host Interface	Wi-Fi :SDIO , BT: UART
Dimension	7.9 mm X 7.3mm x 1.1 mm
Package	SIP (LGA Type)
Antenna	1X1
Weight	0.1620~0.1640g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant
WLAN VID/PID	1A3B / 2256
WLAN SVID/SPID	2.4 GHz ISM Bands 2.412-2.472 GHz 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada
Frequency Rage	802.11a/g/n/ac: OFDM 802.11b: CCK(11, 5.5Mbps), DQPSK(2Mbps), BPSK(1Mbps)
Modulation	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant
Number of Channels	**2.4GHz** ■ USA, NORTH AMERICA, Canada and Taiwan – 1 ~ 11 ■ China, Australia, Most European Countries – 1 ~ 13 **5GHz** USA, EUROPE – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165

Output Power[1] (Board Level Limit)*

2.4G

	Min	Typ	Max	Unit
11b (11Mbps) @EVM<35%	15	17	19	dBm
11g (54Mbps) @EVM≦-27 dB	12	14	16	dBm
11n (HT20 MCS7) @EVM≦-28 dB	11	13	15	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps) @EVM≦-27 dB	13	15	17	dBm
11n (HT20 MCS7) @EVM≦-28 dB	13	15	17	dBm
11n (HT40 MCS7) @EVM≦-28 dB	13	15	17	dBm
11ac (VHT20 MCS8) @EVM≦-30 dB	12	14	16	dBm
11ac (VHT40 MCS9) @EVM≦-32 dB	11	13	15	dBm
11ac (VHT80 MCS9) @EVM≦-32 dB	10	12	14	dBm

Receiver Sensitivity

2.4G

	Min	Typ	Max	Unit
11b (11Mbps)		-86	-83	dBm
11g (54Mbps)		-69.5	-66.5	dBm
11n (HT20 MCS7)		-70	-67	dBm

5G

	Min	Typ	Max	Unit
11a (54Mbps)		-71.5	-68.5	dBm
11n (HT20 MCS7)		-70	-67	dBm
11n (HT40 MCS7)		-66.5	-63.6	dBm
11ac (VHT20 MCS8)		-64	-61	dBm
11ac (VHT40 MCS9)		-62	-59	dBm
11ac (VHT80 MCS9)		-58.5	-55.5	dBm

Data Rate

WLAN:
802.11b : 1, 2, 5.5, 11Mbps
802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
802.11ac/n : Maximum data rates up to 86.7 Mbps(20MHz channel),200 Mbps (40 MHz channel), 433 Mbps (80 MHz channel)

[1] EVM Spec are under typical test conditions.

Security	WPA and WPA2 (Personal) support for powerful encryption and authentication. AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility. Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, and CCX 4.0). Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS).

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Bluetooth

Features	Description
Bluetooth Standard	BT5.0+Enhanced Data Rate (EDR)
Bluetooth VID/PID	N/A
Frequency Rage	2402MHz~2483MHz
Modulation	Header GFSK Payload 2M: 4-DQPSK Payload 3M: 8DPSK
Output Power	

	Min	Typ	Max	Unit
GFSK		9	11	dBm

Receiver Sensitivity

	Min	Typ	Max	Unit
BR		-80	-77	dBm
EDR(8DPSK)		-77	-74	dBm

1.3.4 Operating Conditions

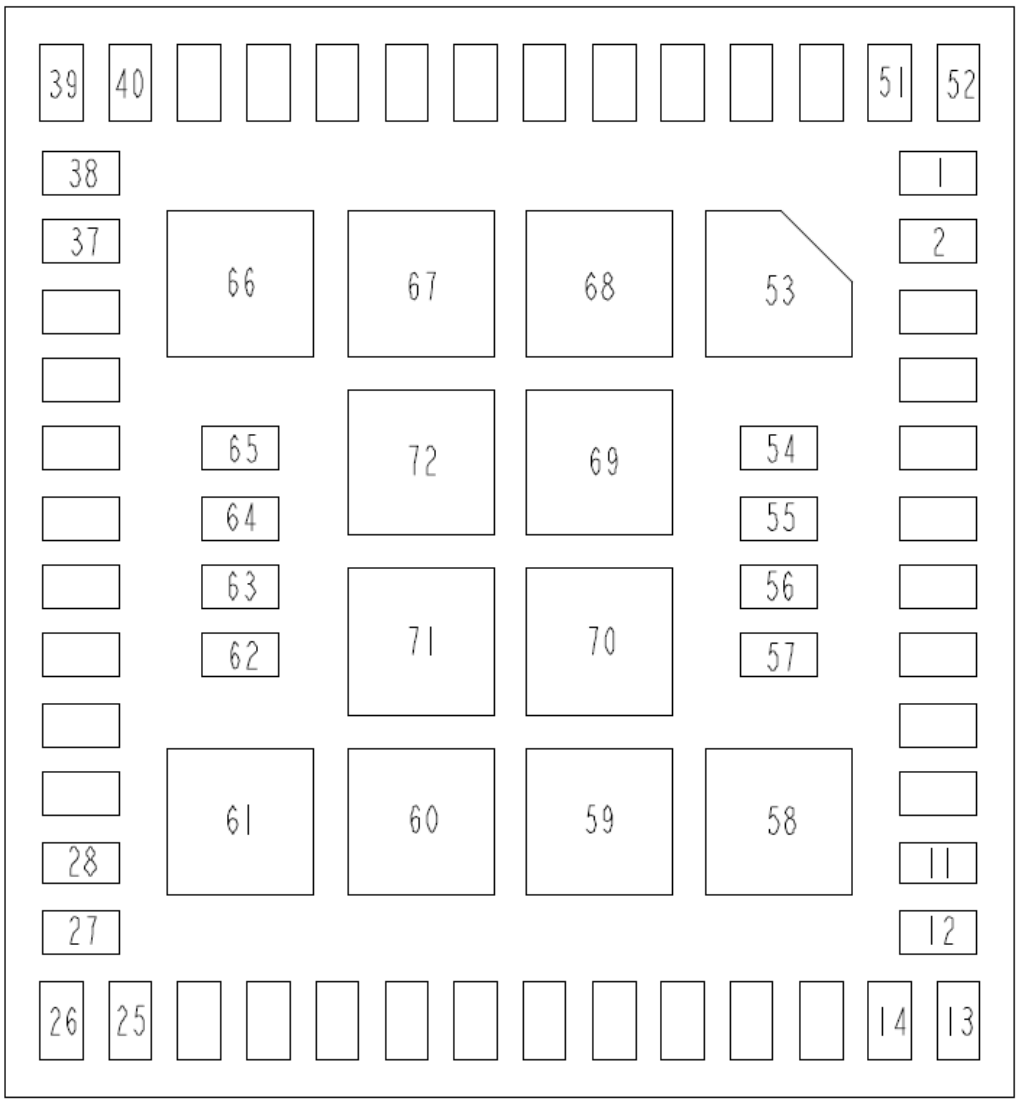
Features	Description
Operating Conditions	
Voltage	VBAT: 3.35 ~ 4.2V ; typical: 3.6V VIO : 2.97~3.63V ; typical: 3.3V
Operating Temperature	-30 to +85 °C[2]
Operating Humidity	less than 85% R.H.
Storage Temperature	-40 to +85 °C
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	1KV per JEDEC EID/JESD22-A114
Changed Device Model	250V per JEDEC EIA/JESD22-C101

[2] Functionality is guaranteed across this ambient temperature range. Optimal RF performance specified in the data sheet, however, is guaranteed only for –20°C to 75°C.

2. Pin Definition

2.1 Pin Map

AW-CH303-H BOT View Pin Map



2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	GPIO_6	GPIO configuration pin		I/O
2	GPIO_0	GPIO configuration pin.		I/O
3	GPIO_3	GPIO configuration pin		I/O
4	GPIO_5	GPIO configuration pin		I/O
5	GPIO_1	GPIO configuration pin		I/O
6	GPIO_4	GPIO configuration pin		I/O
7	GPIO_2	GPIO configuration pin		I/O
8	WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.		I
9	BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.		I
10	GND	Ground.		GND
11	VDDIO	3.3V VDDIO supply for WLAN and BT	3.3V	VCC
12	GND	Ground.		GND
13	GND	Ground.		GND
14	SDIO_DATA_0	SDIO Data Line 0		I/O
15	SDIO_CMD	SDIO Command Input		I/O
16	SDIO_DATA_1	SDIO Data Line 1		I/O
17	SDIO_DATA_2	SDIO Data Line 2		I/O
18	SDIO_DATA_3	SDIO Data Line 3		I/O
19	GND	Ground.		GND
20	SDIO_CLK	SDIO Clock Input		I
21	GND	Ground.		GND
22	VBAT_LDO	Power Supply	3.6V	VCC
23	VBAT_SR	Power Supply		VCC

24	SR_PVSS	Ground.		GND
25	VIN_LDO	Internal Buck voltage generation pin		VCC
26	SR_PVSS	Ground.		GND
27	SR_PVSS	Ground.		GND
28	SR_VLX	Internal Buck voltage generation pin		VCC
29	GND	Ground.		GND
30	LPO_IN	External 32K or RTC clock		I
31	GND	Ground.		GND
32	BT_PCM_IN	PCM data Input		I
33	BT_PCM_SYNC	PCM Synchronization control		I/O
34	BT_PCM_OUT	PCM data Out		O
35	BT_PCM_CLK	PCM Clock		I/O
36	I2S_DO	I2S data output		I/O
37	I2S_CLK	I2S clock, can be master (output) or slave (input).		I/O
38	I2S_WS	I2S WS; can be master (output) or slave (input).		I/O
39	GND	Ground.		GND
40	BT_DEV_WAKE	BT Device Wake		I
41	BT_HOST_WAKE	BT Host Wake		O
42	GND	Ground.		GND
43	FM_IN	FM radio antenna port		I
44	GND	Ground.		GND
45	BT_UART_RXD	High-Speed UART Data In		I
46	BT_UART_TXD	High-Speed UART Data Out		O
47	BT_UART_RTS_N	High-Speed UART RTS		O
48	BT_UART_CTS_N	High-Speed UART CTS		I
49	GND	Ground.		GND
50	WL_BT_ANT	WLAN/BT RF TX/RX path.		RF
51	GND	Ground.		GND

52	GND	Ground.		GND
53	GND	Ground.		GND
54	GND	Ground.		GND
55	GND	Ground.		GND
56	GND	Ground.		GND
57	JTAG_SEL	This pin must connected to ground if the JTAG/SWD interface is not used. It must be high to select SWD OR JTAG. When JTAG_SEL=1 GPIO_2=TCK/SWCLK GPIO_3=TMS/SWDIO GPIO_4=TDIO GPIO_5=TDO GPIO_6=TRST_L		
58	GND	Ground.		GND
59	GND	Ground.		GND
60	GND	Ground.		GND
61	GND	Ground.		GND
62	BT_GPIO_4	Bluetooth general-purpose I/O		I/O
63	BT_GPIO_3	Bluetooth general-purpose I/O		I/O
64	BT_GPIO_2	Bluetooth general-purpose I/O		I/O
65	BT_GPIO_5	Bluetooth general-purpose I/O		I/O
66	GND	Ground.		GND
67	GND	Ground.		GND
68	GND	Ground.		GND
69	GND	Ground.		GND
70	GND	Ground.		GND
71	GND	Ground.		GND
72	GND	Ground.		GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	0	-	+5.0	V
VDDIO	DC supply voltage for digital I/o	0	-	+3.9	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	DC supply for the VBAT and PA driver supply	3.35	3.6	4.2	V
VDDIO	DC supply voltage for digital I/o	2.97	3.3	3.63	V

3.3 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDDIO=3.3V					
V_{IH}	Input high voltage (V_{DDIO})	2.0	-	-	V
V_{IL}	Input low voltage (V_{DDIO})	-	-	0.8	V
V_{OH}	Output High Voltage @ 2mA	2.9	-	-	V
V_{OL}	Output Low Voltage @ 2mA	-	-	0.4	V

3.4 Interface

The AW-CH303-H has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

Note:

- The WL_REG_ON and BT_REG_ON signals are ORed in the AW-CH303-H. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the AW-CH303 regulators.
- The AW-CH303-H has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

Description of Control Signals

The AW-CH303-H has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption.

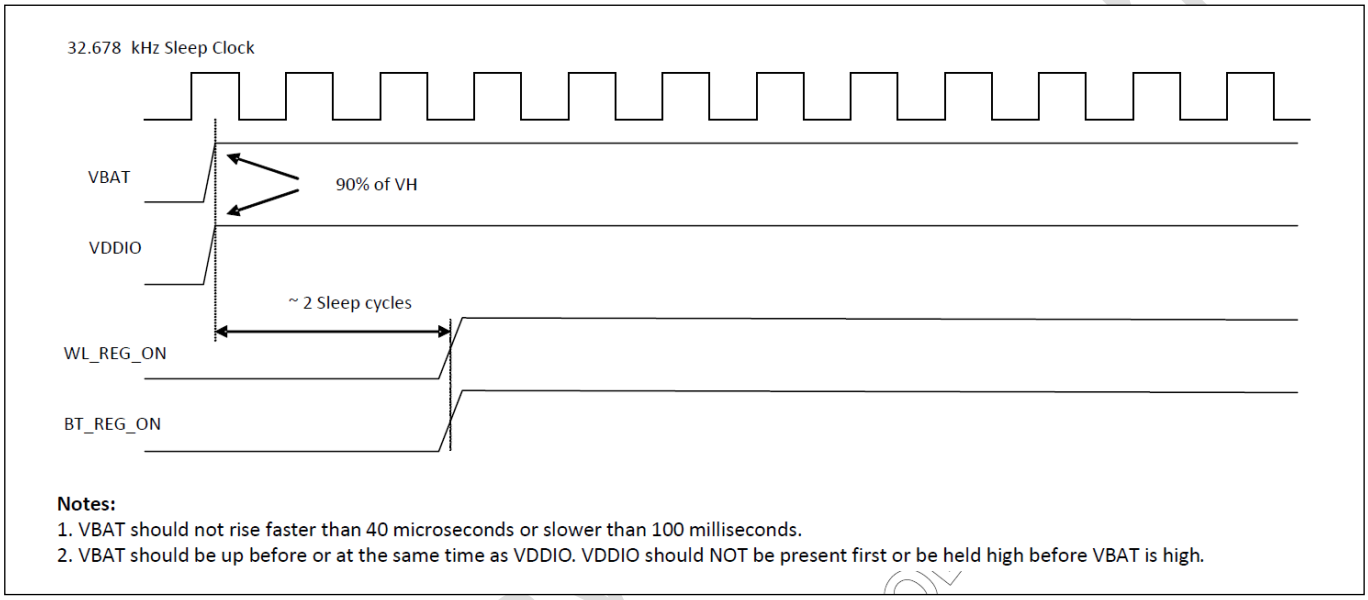
Power-Up/Power-Down/Reset Control Signals

Signal	***Description***
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also ORgated with the BT_REG_ON input to control the internal AW-NMNF regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal AW-CH303 regulators. If both BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

Note: For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 msec time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

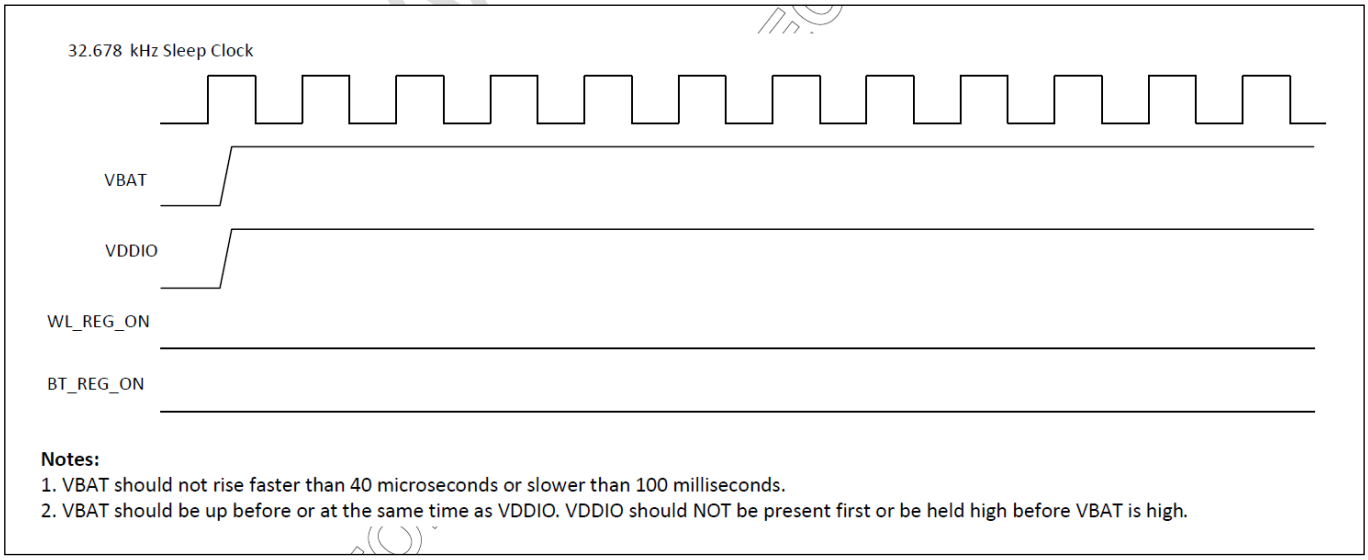
Control Signal Timing Diagrams

WLAN = ON, Bluetooth = ON



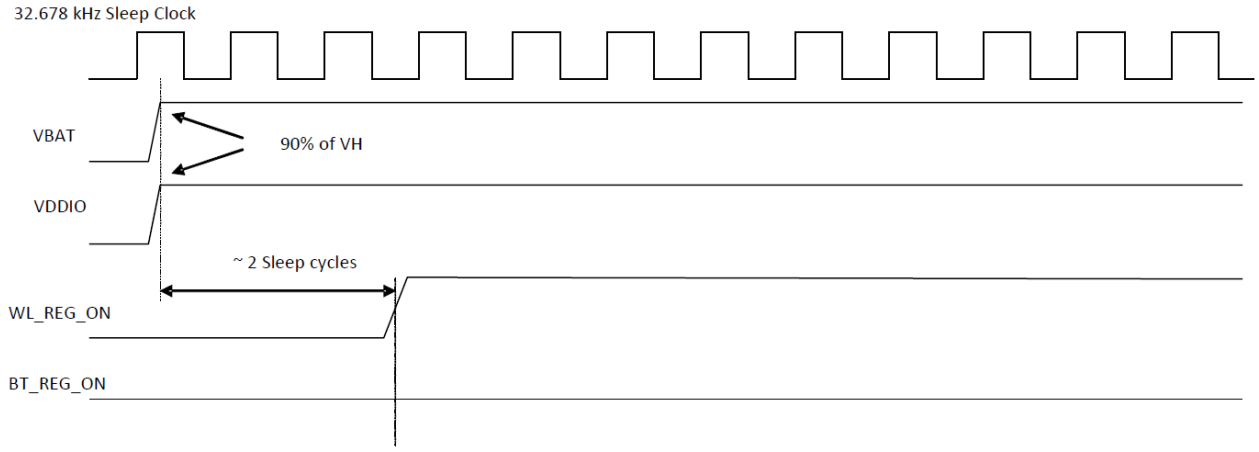
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF



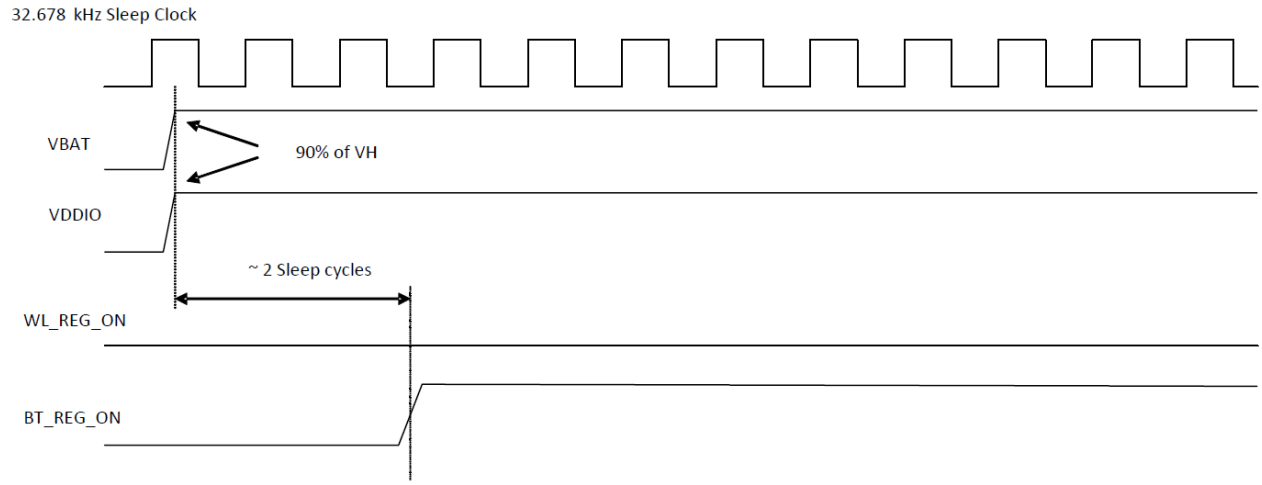
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF



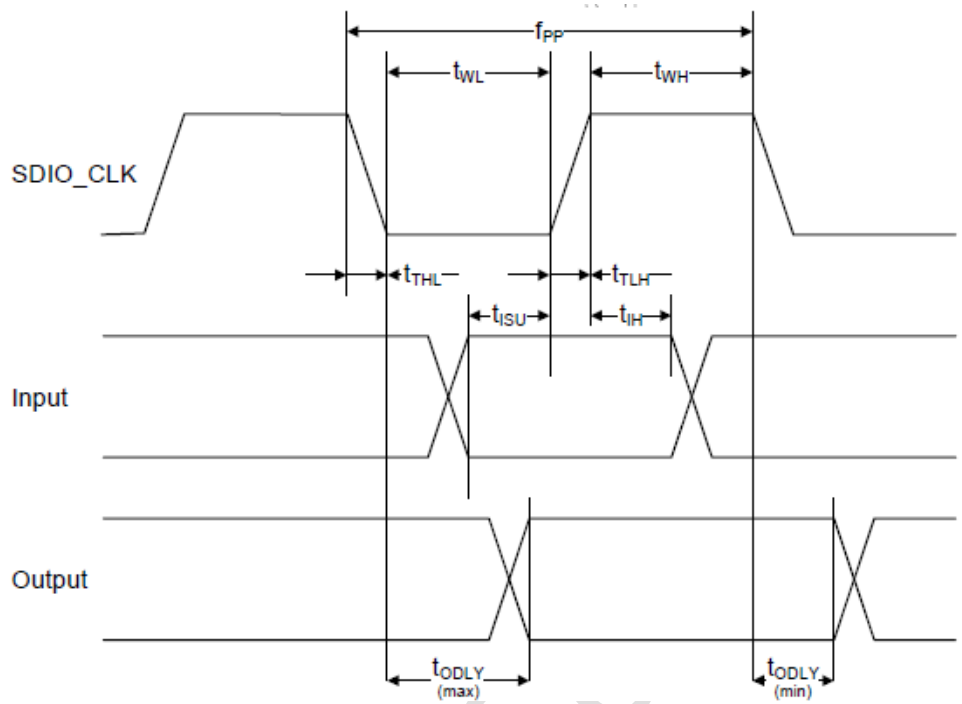
Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = ON



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

3.4.1 SDIO Host Interface Specification



SDIO Timing Data

Symbol	Parameter	Condition	Min	Max	Units
f_{pp}	CLK Frequency	Normal	0	25	MHz
		High Speed	0	50	
t_{WH}	CLK High Time	Normal	10	-	ns
		High Speed	7	-	
t_{WL}	CLK Low Time	Normal	10	-	
		High Speed	7	-	
tTLH	CLK rise Time	Normal	-	10	
		High Speed	-	3	
tTHL	CLK fall Time	Normal	-	10	
		High Speed	-	3	
t_{ISU}	Input Setup Time	Normal	5	-	
		High Speed	6	-	
t_{IH}	Input Hold Time	Normal	5	-	
		High Speed	2	-	
t_{ODLY}	Output Delay Time	Normal	-	14	
		High Speed	-	14	

3.4.2 UART Interface

The AW-CH303-H shares a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmits FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the BT 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

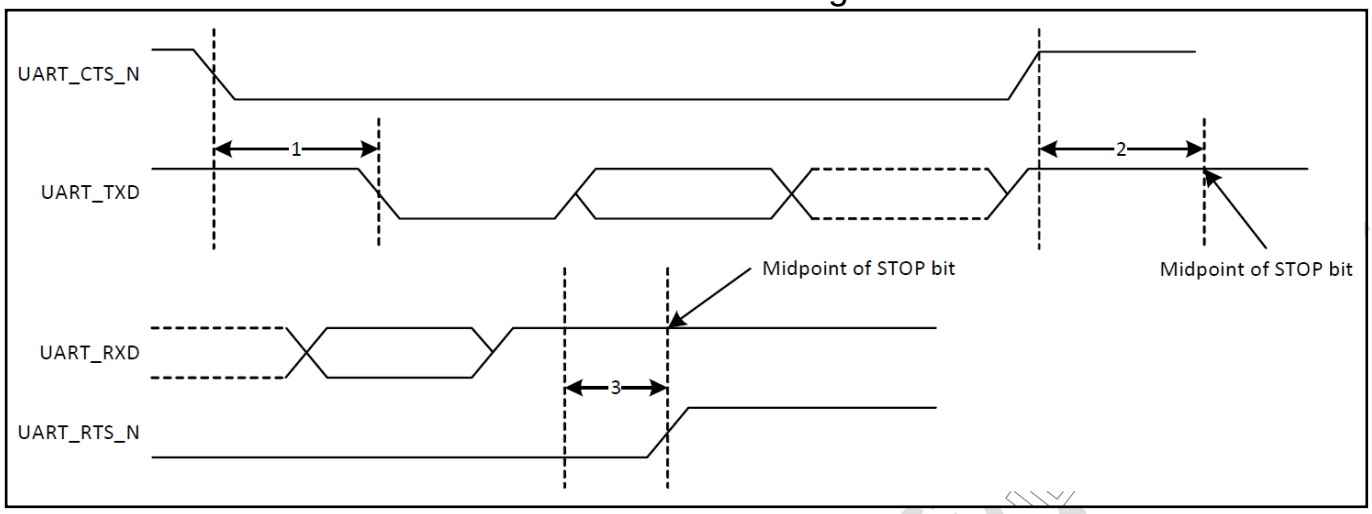
The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification ("Three-wire UART Transport Layer"). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-CH303-H UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

UART Interface Signals

PIN No.	Name	Description	Type
42	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	O
43	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	I
41	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	O
44	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	I

UART Timing



UART Timing Specifications

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

3.5 Power Consumption*

3.5.1 WLAN

No.	Item	Total(VDDIO+VBAT)_IN=3.3V	
		Max.	Avg.
1	power off*(1)(2)(4)	10.2uA	2.67uA
2	Deepsleep (VBAT)(2)(3)(4)(5)	2.15mA	60.7uA
3	Deepsleep (VDDIO)(2)(3)(4)(5)	400uA	350uA
4	Deepsleep (total)(2)(3)(4)(5)	2.48mA	440uA
5	Power Save (2.4G)(2)(3)(4)(6)(7)	57.7mA	2.15mA
6	Power Save (5G)(2)(3)(4)(6)(7)	108.7mA	2.16mA

Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit			Receive	
				Max.	Avg.	Duty %	Max.	Avg.
2.4	11b@1M	20	17	348.8	346.9	96	57.9	56.3
	11b@11M	20	17	345.1	341.2	92	57.4	57.3
	11g@6M	20	14	279.0	277.7	82	57.0	56.5
	11g@54M	20	14	170.8	170.0	41	58.1	58.0
	11n@MCS0	20	13	268.9	267.1	81	56.7	56.3
	11n@MCS7	20	13	173.6	173.0	44	58.8	58.7
5	11a@6M	20	15	306.0	303.6	95	71.6	71.2
	11n@MCS0	20	15	307.8	302.9	97	71.1	70.9
	11n@MCS7	20	15	256.8	255.2	77	73.6	73.4
	11n@MCS0	40	15	317.9	316.0	90	82.1	82.0
	11ac@MCS0 NSS1	80	12	299.0	297.8	82	108.9	108.8
	11ac@MCS9 NSS1	80	12	207.5	207.1	43	112.5	112.4

* The power consumption is based on Azurewave test environment, these data for reference only.

*Current Unit: mA

(1) Bring up WLAN, confirm WLAN was installed.(# ./wl ver)
  a). BT_REG_On=LOW (J12 pin)
  b). WL_REG_On=LOW (J13 pin)
(2) Using normal firmware.
(3) Link AP use ASUS RT-AC66U, DTIM = 1, Beacon Interval = 100 ms
(4) Measurement Instrument using Agilent 34411A Digit Multimeter
(5) ./wl deepsleep -1
(6) ./wl up -> ./wl join AP -> ./wl PM 2
(7)2.4GHz Fixed data rate =11b 1Mbps (./wl bg_rate =1) ,5GHz Fixed data rate =11a 6Mbps(./wl a_rate =6)

3.5.2 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	Total(VDDIO+VBAT)_IN=3.3V	
				Max.	Avg.
1	Transmit	DH5	9.1	53.8mA	31.0mA
2	Receive	3DH5	N/A	36.7mA	23.9mA

* Current Unit: mA

* The power consumption is based on Azurewave test environment, these data for reference only.

3.6 Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

The AW-CH303 uses a secondary low frequency clock for low-power-mode timing. Either the internal low- precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake-up earlier to avoid missing beacons. Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in below.

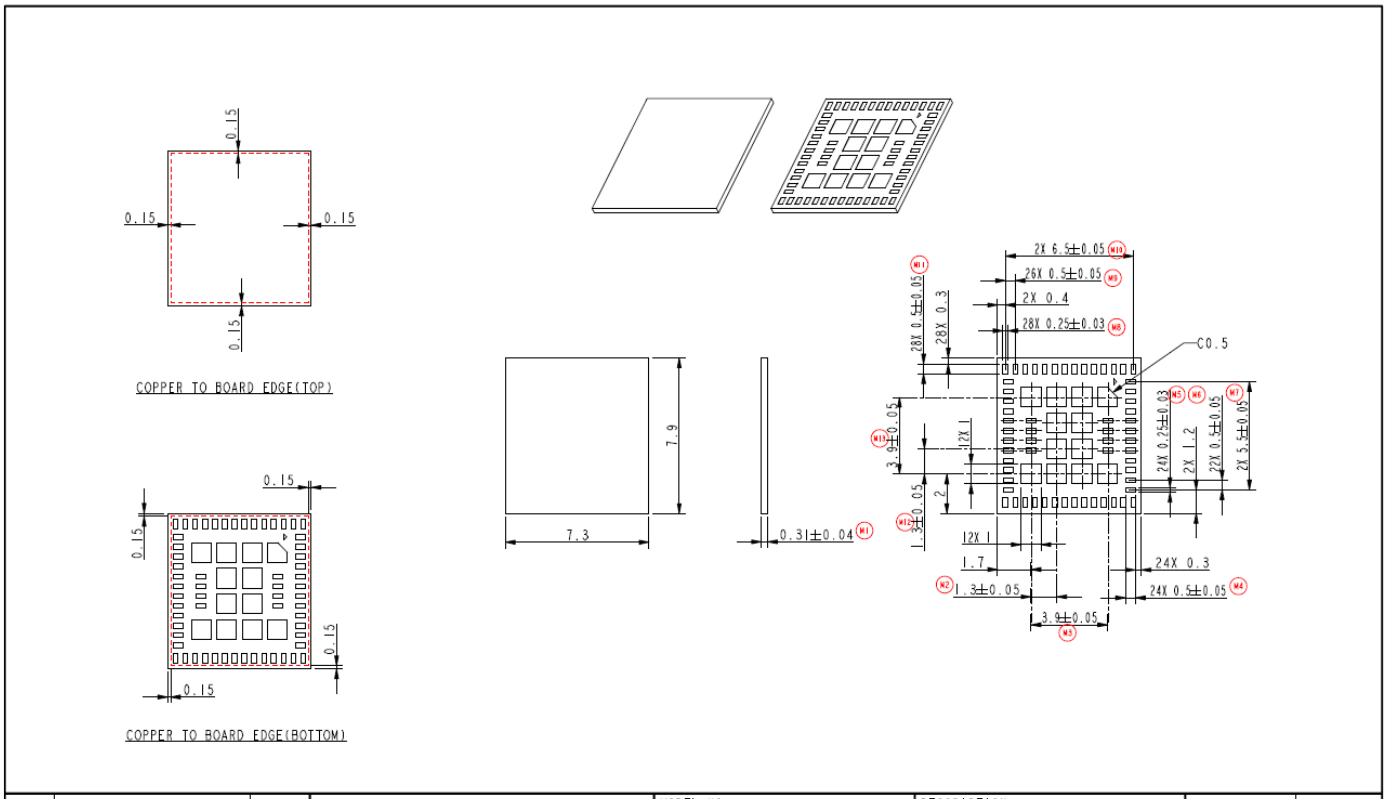
External 32.768 kHz Sleep Clock Specifications

Parameter	*LPO Clock*	*Units*
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[a]	>100k <5	Ω pF
Clock jitter (during initial start-up)	<10,000	ppm

a. When power is applied or switched off.

4. Mechanical Information

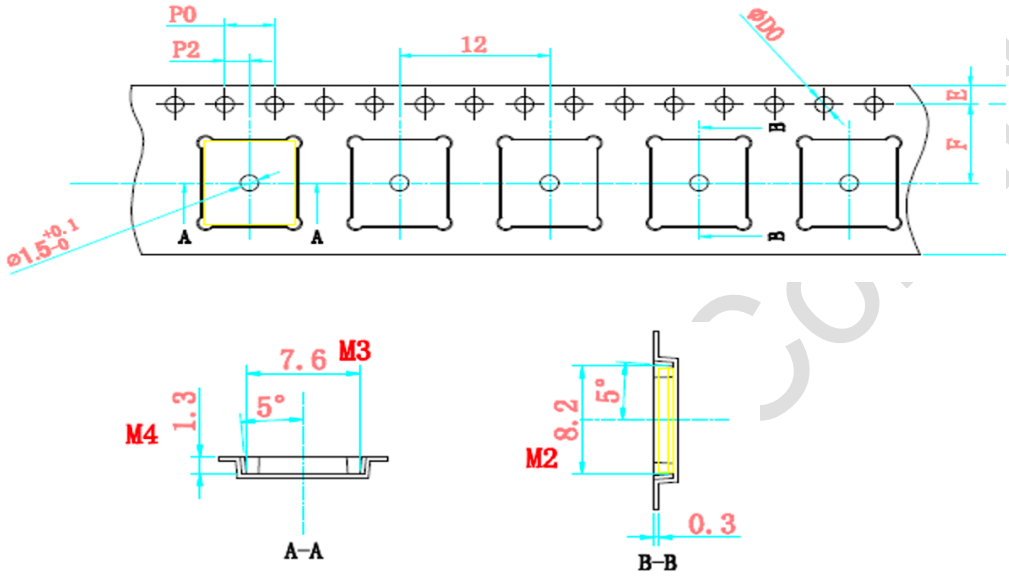
4.1 Mechanical Drawing



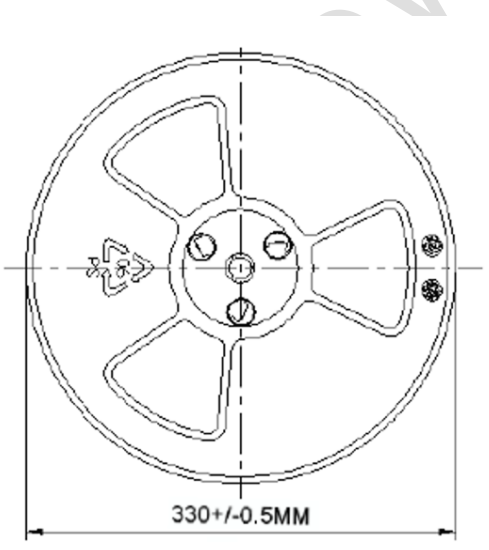
			AzureWave					MODEL NO.		DESCRIPTION					DOCUMENT LEVEL	APPROVAL
								1303		PCB LAYOUT MECHANICAL DRAWING					CONFIDENTIAL	
			DIM.	0~80	80~180	180~315	315~800	PART NO.	DRAWING NO.	MATERIAL	UNIT	SCALE	REV	PAGE	DATE	DESIGNED
ITEM	DESCRIPTION	DATE	TOL.	±0.1	±0.15	±0.20	±0.25	5-PP003993	1303-LMC-003-3993	BT	mm	4/1	A	1/1	2018/05/10	STEVE CHANG

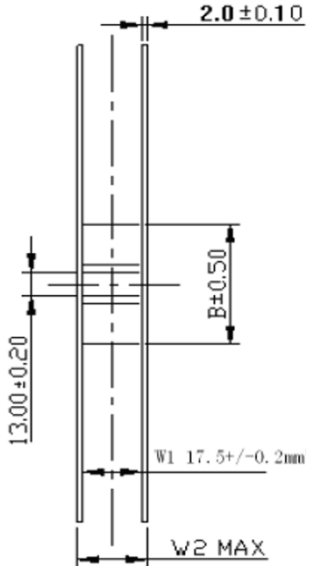
5. Packaging Information

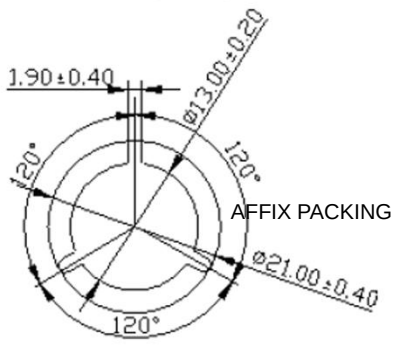
5-1 Put module in the same location.
The module polarity direction is on the upper left of the tape carrier.



Dimension	
E	1.75±0.10
E2	14.25 MIN
F	7.50±0.10
P2	2.00±0.10
ØDo	$1.50^{+0.10}_{-0.00}$
ØD1	
Po	4.00±0.10
10Po	40.00±0.20
W	16.00±0.30
P	12.00±0.10
Ao	7.60±0.10
B0	8.20±0.10
K0	1.30±0.10
t	0.30±0.05

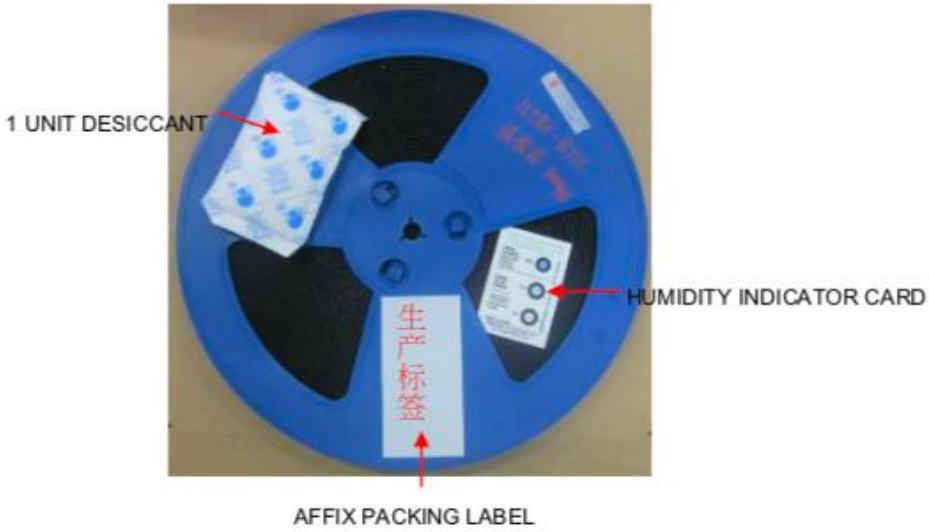




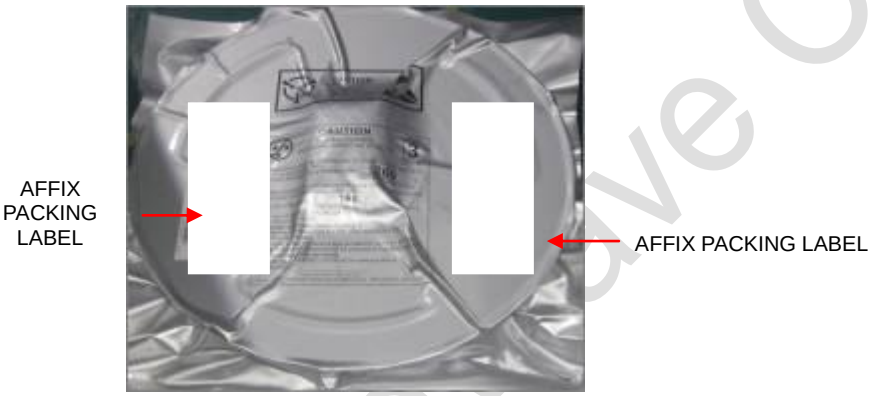


AFFIX PACKING LABEL

5-2



5-2



5-3

5-4

AFFIX PACKING LABEL

5-5

1 Carton= 5 Boxes

5-6

AFFIX PACKING LABEL

Note: 1 tape reel = 1 box = 3,500pcs

1 carton = 5 boxes = 5 * 3,500pcs=17,500pcs