AzureWave Technologies, Inc.

AW-BT315W

BT5.0 SiP Module

Datasheet

Rev. A

STD

(For Standard)

Features

Bluetooth Subsystem

- Complies with Bluetooth Core Specification v5.0 with LE 2 Mbps
- Supports Basic Rate (BR), Enhanced Data Rate (EDR) 2&3Mbps, Bluetooth Low Energy (BLE)
- Supports Adaptive Frequency Hopping (AFH)
- Ultra-low-power radio
- Asymmetric cryptographic methods (AES, 3DES, RSA, and ECC) and Hash functions (SHA-512, SHA-256)
- Up to 66 programmable IOs

Coexistence Support

- Support for Global Coexistence Interface for easy coexistence implementation with select Cypress Wi-Fi devices

MCU Subsystem

- 96-MHz Arm Cortex-M4 microcontroller unit MCU with floating point unit (FPU)
- Supports serial wire debug (SWD)
- Runs Bluetooth stack and application
- Option to execute from on-chip flash or RAM

Memory Subsystem

- 1 MB flash
- 512 KB RAM
- 2 MB ROM that stores Bluetooth stack and driver and offloads flash for user applications

Audio Features and Interfaces

- 1x I2S with master and slave modes
- 1x PCM
- PDM2
- Analog front end for analog microphone1

Clocks

- On-chip 32 kHz oscillator (LP-LPO)
- On-chip 128 kHz oscillator (HP-LPO)
- 32 kHz crystal oscillator (Optional if low power modes not required)
- 24 MHz crystal oscillator
- 48-bit real time clock (RTC)

Peripherals and Communication

- 6x 16-bit PWMs
- Programmable key-scan matrix interface, up to 8x20 keyscanning matrix1, 2
- Watchdog timer (WDT)
- 1x peripheral UART, 1x UART for programming and HCI
- 2x SPI (master or slave mode) Blocks (SPI, Quad SPI, and MIPI DBI-C)
- 1x I2C master/slave2 and 1x I2C master
- 1x 28-channel ADC (10-ENoB for DC measurement and 12-ENOB for Audio measurement)
- Hardware security engine

General Purpose Input Output (GPIO)

- 40 GPIOs on AW-BT315W
- Support up to 3.63 V operation
- Four GPIOs support 16 mA and 8 mA sink at 3.3 V and 1.8 V respectively

Operating Voltage and Low-power Support

- Wide operating voltage range: 1.76V to 3.63V
- 5 power modes to implement ultra-low power application – managed by real time operating system
- 0.4 µA current in HID-OFF2 mode (wake from GPIO).

Packages

- 4 mm × 4 mm 81-pin LGA

Applications

- Wearables and Fitness bands
- Headsets, earbuds, and other audio solutions
- Home automation
- Blood pressure monitors and other medical applications
- Proximity sensors
- Key Fobs
- Thermostats and thermometers
- Toys

Revision History

Document NO:

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	**2020/04/29**		**Initial Version**	**Licheng Wang**	**Chihhao Liao**

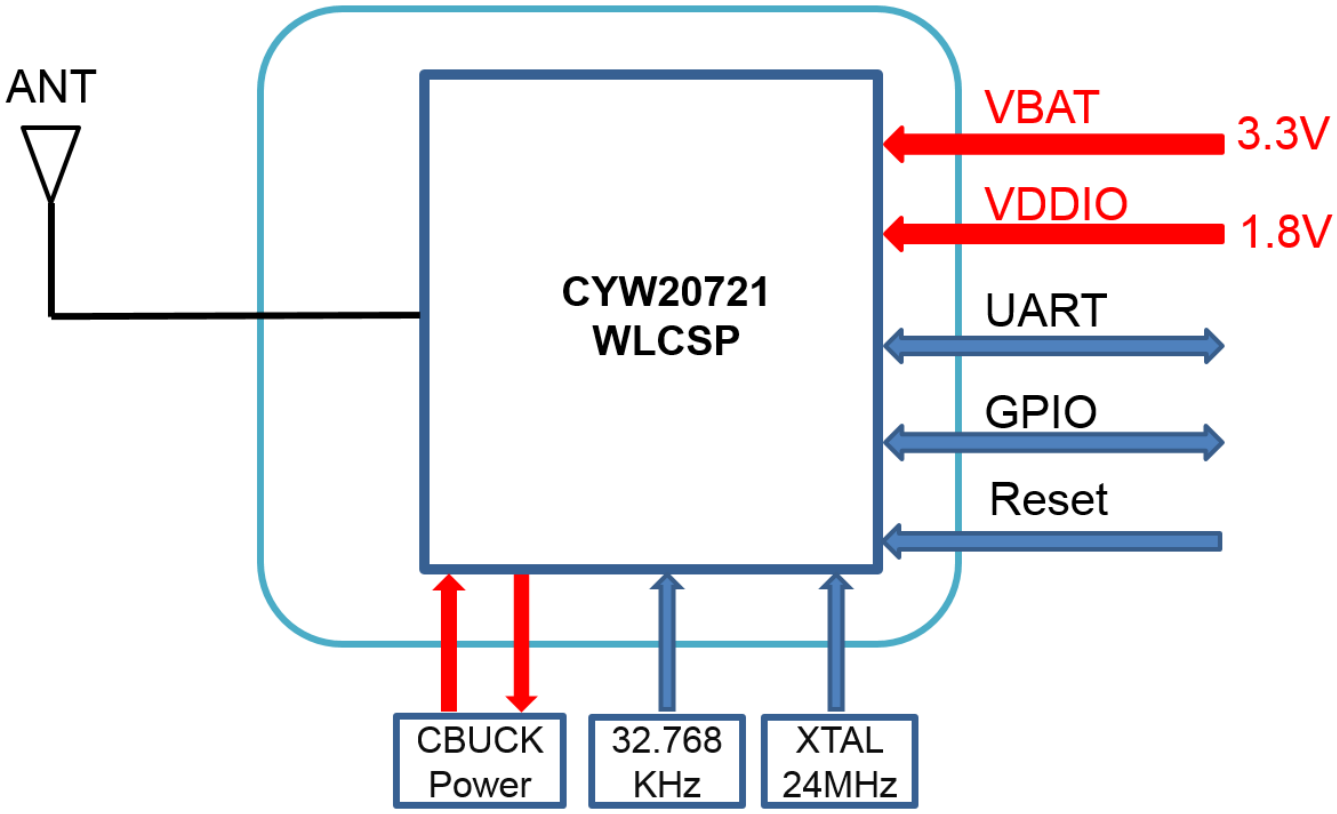
Table of Contents

1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced Bluetooth SiP module - AW-BT315W. The AW-BT315W is a BT 5.0-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver with BLE, EDR and BR. The device is intended for use in audio, IoT, sensors (medical, home, security, and so forth) and human interface device (HID) applications.This datasheet provides details of the functional, operational, and electrical characteristics of the AW-BT315W device. It is intended for hardware, design, application, and OEM engineers.

1.2 Block Diagram



**Support different HW configurations. Please contact Azurewave for the details.*

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	Bluetooth 5.0 SiP Module
Major Chipset	Cypress CYW20721B2(WLCSP)
Host Interface	UART
Dimension	4mm(L) x 4mm(W) x 0.92mm(H)
Package	LGA Module
Antenna	External PCB antenna
Weight	TBD

1.3.2 Bluetooth

Features	Description
Bluetooth Standard	BT5.0+Enhanced Data Rate (EDR)+BLE
Bluetooth VID/PID	n/a
Frequency Rage	2400~2483.5MHz
Modulation	GFSK (1Mbps), Π/4DQPSK (2Mbps) and 8DPSK (3Mbps)
Output Power	Basic Rate : TBD dBm +/- 2dBm (Max Settings) BLE: TBD dBm+/-2dBm
Receiver Sensitivity	

	Min	Typ	Max	Unit
DH5		TBD		dBm
2DH5		TBD		dBm
3DH5		TBD		dBm

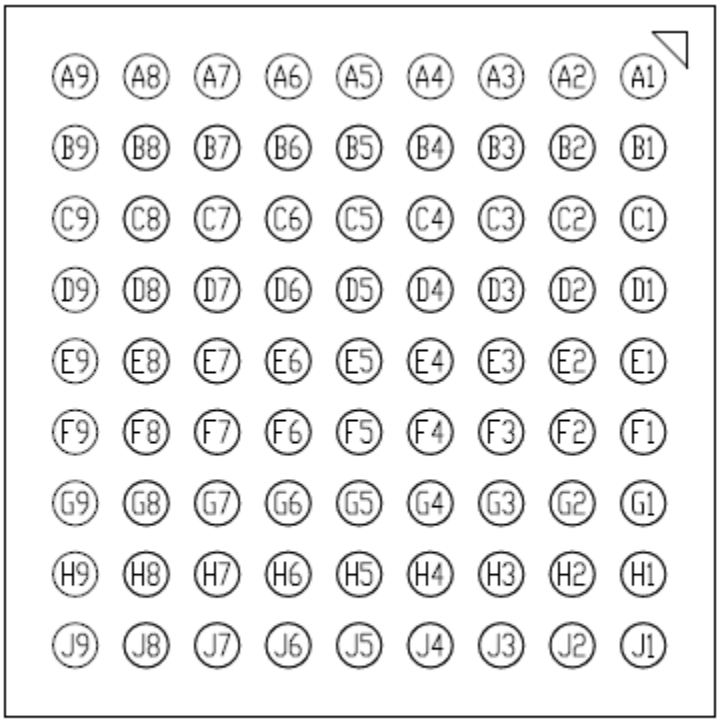
1.3.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VDD3P3:1.76V~3.63V (3.0V Typical) VDDIO:1.76V~3.63V (3.0V Typical)
Operating Temperature	-30~85°C
Operating Humidity	less than 85% R.H.
Storage Temperature	-40~150°C
Storage Humidity	less than 60% R.H.
ESD Protection	
Human Body Model	< 2KV
Changed Device Model	< 500V

2. Pin Definition

2.1 Pin Map

AW-BT315W Bot View Pin Map



PIN DEFINED (BOTTOM VIEW)

2.2 Pin Table[1]

Pin No	Definition	Basic Description	Voltage	Type
A1	GND-A1	Connect to GND.		GND
A2	VDD3P3	Core Buck Input	3V	VBAT
A3	BT_CBUCK_IN	Internal Buck voltage generation pin		VCC
A4	GND-A4	Connect to GND.		GND
A5	P13	■ GPIO: P13 ■ A/D converter input 22 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
A6	GND-A6	Connect to GND.		GND
A7	GND-A7	Connect to GND.		GND
A8	GND-A8	Connect to GND.		GND
A9	ANT	BT RF TX/RX path		RF
B1	BT_CBUCK_OUT	Internal Buck voltage generation pin		VCC
B2	GND-B2	Connect to GND.		GND
B3	P33	■ GPIO: P33 ■ A/D converter input 6 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
B4	P10	■ GPIO: P10 ■ Keyboard scan output (column): KSO2 ■ A/D converter input 25 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
B5	BT_GPIO_4	GPIO: Can also be configured as a GCI Pin		I/O
B6	BT_DEV_WAKE	A signal from the host to the AW-BT315W indicating that the host requires attention.		I
B7	P11	■ GPIO: P11 ■ A/D converter input 24 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
B8	P2	■ GPIO: P2 ■ Keyboard scan input (row): KSI2 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
B9	GND-B9	Connect to GND.		GND
C1	P31	■ GPIO: P31 ■ A/D converter input 8 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
C2	P24	■ GPIO: P24		I/O

[1] All GPIOs are super mux. All GPIOs can be programmed for any alternative functions as listed in Table 1. During power-on reset, all inputs are disabled.

		■ Supermux I/O functions as defined in 2.3 GPIO List		
C3	P27	■ GPIO: P27 ■ Current: 16 mA sink ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
C4	P0	■ GPIO: P0 ■ Keyboard scan input (row): KSI0 ■ A/D converter input 29 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
C5[2]	P37	■ GPIO: P37 ■ A/D converter input 2 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
C6	P8	■ GPIO: P8 ■ A/D converter input 27 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
C7	GND-C7	Connect to GND.		GND
C8	GND-C8	Connect to GND.		GND
C9	BT_XTALO	Crystal oscillator output.		O
D1	RST_N	Active-low system reset with internal pull-up resistor.		I
D2	P25	■ GPIO: P25 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
D3	P34	■ GPIO: P34 ■ A/D converter input 5 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
D4	P29	■ GPIO: P29 ■ A/D converter input 10 ■ Current: 16 mA sink ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
D5	P9	■ GPIO: P9 ■ A/D converter input 26 ■ External T/R switch control: tx_pd ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
D6	P7	■ GPIO: P7 ■ Keyboard scan input (row): KSI7 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
D7	P6	■ GPIO: P6		I/O

[2] Pin No:C5(P37) should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow
through these pins until the part comes out of reset.

		■ Keyboard scan input (row): KSI6 ■ Supermux I/O functions as defined in 2.3 GPIO List		
D8	GND-D8	Connect to GND.		GND
D9	BT_XTALI	Crystal oscillator input. The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth specification. Two external load capacitors are required to work with the crystal oscillator.		I
E1	P32	■ GPIO: P32 ■ A/D converter input 7 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
E2	P38	■ GPIO: P38 ■ A/D converter input 1 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
E3	P30	■ GPIO: P30 ■ A/D converter input 9 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
E4	P23	■ GPIO: P23 ■ A/D converter input 12 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
E5	GND-E5	Connect to GND.		GND
E6	GND-E6	Connect to GND.		GND
E7	GND-E7	Connect to GND.		GND
E8	GND-E8	Connect to GND.		GND
E9	GND-E9	Connect to GND.		GND
F1	P26	■ GPIO: P26 ■ Current: 16 mA sink ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
F2	NC	Leave unconnected.		
F3	P21	■ GPIO: P21 ■ A/D converter input 14 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
F4	NC	Leave unconnected.		
F5	P16	■ GPIO: P16 ■ A/D converter input 19 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
F6	BT_GPIO_3	GPIO: Can also be configured as a GCI Pin		I/O
F7	BT_GPIO_5	GPIO: Can also be configured as a GCI Pin		I/O
F8	BT_HOST_WAKE	A signal from the AW-BT315W device to the host indicating that the Bluetooth device requires attention		O
F9	GND-F9	Connect to GND.		GND
G1	P36	■ GPIO: P36 ■ A/D converter input 3		I/O

		■ Supermux I/O functions as defined in 2.3 GPIO List		
G2	P35	■ GPIO: P35 ■ A/D converter input 4 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
G3	P18	■ GPIO: P18 ■ A/D converter input 17 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
G4	P5	■ GPIO: P5 ■ Keyboard scan input (row): KSI5 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
G5	P3	■ GPIO: P3 ■ Keyboard scan input (row): KSI3 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
G6	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.		I
G7	GND-G7	Connect to GND.		GND
G8	GND-G8	Connect to GND.		GND
G9	BT_GPIO_2	GPIO: Can also be configured as a GCI Pin		I/O
H1	P1	■ GPIO: P1 ■ Keyboard scan input (row): KSI1 ■ A/D converter input 28 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
H2	P12	■ GPIO: P12 ■ A/D converter input 23 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
H3	P17	■ GPIO: P17 ■ A/D converter input 18 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
H4	P4	■ GPIO: P4 ■ Keyboard scan input (row): KSI4 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
H5[3]	P15	■ GPIO: P15 ■ A/D converter input 20 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
H6	BT_UART_TXD	UART serial output. Serial data output for the HCI UART interface.		O

[3] Pin No:H5(P15) should not be driven high externally while the part is held in reset (they can be floating or driven low). Failure to do so may cause some current to flow
through these pins until the part comes out of reset.

H7	BT_UART_RTS	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.		O
H8	BT_UART_CTS	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.		I
H9	GND-H9	Connect to GND.		GND
J1	GND-J1	Connect to GND.		GND
J2	NC	Leave unconnected.		
J3	P14	■ GPIO: P14 ■ A/D converter input 21 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
J4	P22	■ GPIO: P22 ■ A/D converter input 13 ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
J5	P28	■ GPIO: P28 ■ A/D converter input 11 ■ Current: 16 mA sink ■ Supermux I/O functions as defined in 2.3 GPIO List		I/O
J6	BT_XTAL_32K_I	Low-power oscillator input.		I
J7	BT_XTAL_32K_O	Low-power oscillator output		O
J8	GND-J8	Connect to GND.		GND
J9	VDDIO	VDDIO supply for I/O.	3V	VIO

2.3 GPIO List

Input	Description
SWDCK	Serial Wire Debugger Clock
SWDIO	Serial Wire Debugger I/O
spiffy1_clk[s]	SPIFFY 1 Clock (Slave)
spiffy1_cs[s]	SPIFFY 1 Chip Select (Slave)
spiffy1_mosi[s]	SPIFFY 1 MOSI (Slave)
spiffy1_miso[m]	SPIFFY 1 MISO (Master)
spiffy1_io2	SPIFFY 1 I/O 2 (Quad SPI)
spiffy1_io3	SPIFFY 1 I/O 3 (Quad SPI)
spiffy1_int[s]	SPIFFY 1 Interrupt (Slave)
spiffy2_clk[s]	SPIFFY 2 Clock (Slave)
spiffy2_cs[s]	SPIFFY 2 Chip Select (Slave)
spiffy2_mosi[s]	SPIFFY 2 MOSI (Slave)
spiffy2_miso[m]	SPIFFY 2 MISO (Master)
spiffy2_io2	SPIFFY 2 I/O 2
spiffy2_io3	SPIFFY 2 I/O 3
spiffy2_int[s]	SPIFFY 2 Interrupt (Slave)
puart_rx	Peripheral UART RX
puart_cts_n	Peripheral UART CTS
SCL	I2C Clock
SDA	I2C Data
SCL2	I2C2 Clock
SDA2	I2C2 Data
PCM_IN	PCM Input
PCM_CLK	PCM Clock
PCM_SYNC	PCM Sync
I2S_DI	I2S Data Input
I2S_WS	I2S Word Select
I2S_CLK	I2S Clock
PDM_IN_Ch_1	PDM Input Channel 1
PDM_IN_Ch 2	PDM Input Channel 2

Output	Description
do_P# (data out of GPIO. For example: 0)	
kso0	Key Scan output 0
kso1	Key Scan output 1
kso2	Key Scan output 2
kso3	Key Scan output 3
kso4	Key Scan output 4
kso5	Key Scan output 5
kso6	Key Scan output 6
kso7	Key Scan output 7
kso8	Key Scan output 8
kso9	Key Scan output 9
kso10	Key Scan output 10
kso11	Key Scan output 11
kso12	Key Scan output 12
kso13	Key Scan output 13
kso14	Key Scan output 14
kso15	Key Scan output 15
kso16	Key Scan output 16
kso17	Key Scan output 17
kso18	Key Scan output 18
kso19	Key Scan output 19
do_P# ^ pwm0	PWM Channel 0
do_P# ^ pwm1	PWM Channel 1
do_P# ^ pwm2	PWM Channel 2
do_P# ^ pwm3	PWM Channel 3
do_P# ^ pwm4	PWM Channel 4
do_P# ^ pwm5	PWM Channel 5
aclk0	Auxiliary clock Output 0
aclk1	Auxiliary clock Output 1
HID_OFF	HID-OFF Indicator
pa_ramp	External PA ramp
tx_pu	External PA Control Signal
rx_pu	External PA Control Signal
SWDIO	Serial Wire Debugger Input/ Output
SDA2	I2C 2 Data
SCL2	I2C 2 Clock
puart_tx (uart2_tx)	Peripheral UART TX

Output	Description
puart_rts_n (uart2_rts_n)	Peripheral UART RTS
spiffy1_CLK	SPIFFY 1 Clock
spiffy1_CS	SPIFFY 1 Chip Select
spiffy1_MOSI	SPIFFY 1 MOSI
spiffy1_MISO	SPIFFY 1 MISO
spiffy1_IO2	SPIFFY I/O 2
spiffy1_IO3	SPIFFY I/O 3
spiffy1_INT	SPIFFY Interrupt
spiffy1_DCX	MIPI-DBI Data/Command Indicator
spiffy2_CLK	SPIFFY 2 Clock
spiffy2_CS	SPIFFY 2 Chip Select
spiffy2_MOSI	SPIFFY 2 MOSI
spiffy2_MISO	SPIFFY 2 MISO
spiffy2_IO2	SPIFFY 2 I/O 2
spiffy2_IO3	SPIFFY 2 I/O 3
spiffy2_INT	SPIFFY 2 Interrupt
spiffy2_DCX	MIPI-DBI Data/Command Indicator
pcm_in_o	PCM IN
pcm_out_o	PCM Out
pcm_bclk_o	PCM Bit Clock
pcm_sync_o	PCM Sync Output
i2s_ssd	I2S Slave Serial Data
i2s_sws	I2S Slave Word Select
i2s_sck	I2S Slave Clock
i2s_msd	I2S Master Serial Data
i2s_mws	I2S Master Word Select
i2s_mck	I2S Master Clock

2.4 Reference for how to connect to Codec[4]

Pin Available for I2C		
Pin No.	Definition	I2C function
F8	P16	I2C_SDA
F10	P17	I2C_SCL

Pin Available for SPIO-FLASH:		
Pin No.	Definition	I2C function
E5	P0	SPI_MOSI
H4	P1	SPI_MISO
J5	P3	SPI_CLK
D2	P32	SPI_CS

Pin Availble for I2S		
Pin No.	Definition	I2C function
G9	P8	I2S_DO
J7	P9	I2S_DI
G7	P11	I2S_BCLK
G5	P12	I2S_LRCLK

Pin Available for SPI1-CODEC		
Pin No.	Definition	I2C function
F4	P35	SPI_MOSI
H2	P36	SPI_MISO
D4	P30	SPI_CLK
E11	P7	SPI_CS

[4] 2.4 Reference for how to connect to Codec is only for “reference”, please confirm it with Azurewave FAE and CODEC vendor.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD3P3	VBAT input	-0.5		3.795	V
VDDIO	Supply for I/O voltage	-0.5		3.795	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD3P3	VBAT input	1.76	3	3.63	V
VDDIO	Supply for I/O voltage	1.76	3	3.63	V

3.3 GPIO DC Characteristics

For VDDIO = 3V

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	Input high voltage	2.4			V
V_{IL}	Input low voltage			0.8	V
V_{OH}	Output High Voltage	VDDIO-0.45V			V
V_{OL}	Output Low Voltage			0.45	V

For VDDIO = 1.8V

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	Input high voltage	1.4			V
V_{IL}	Input low voltage			0.45	V
V_{OH}	Output High Voltage	VDDIO-0.45V			V
V_{OL}	Output Low Voltage			0.45	V

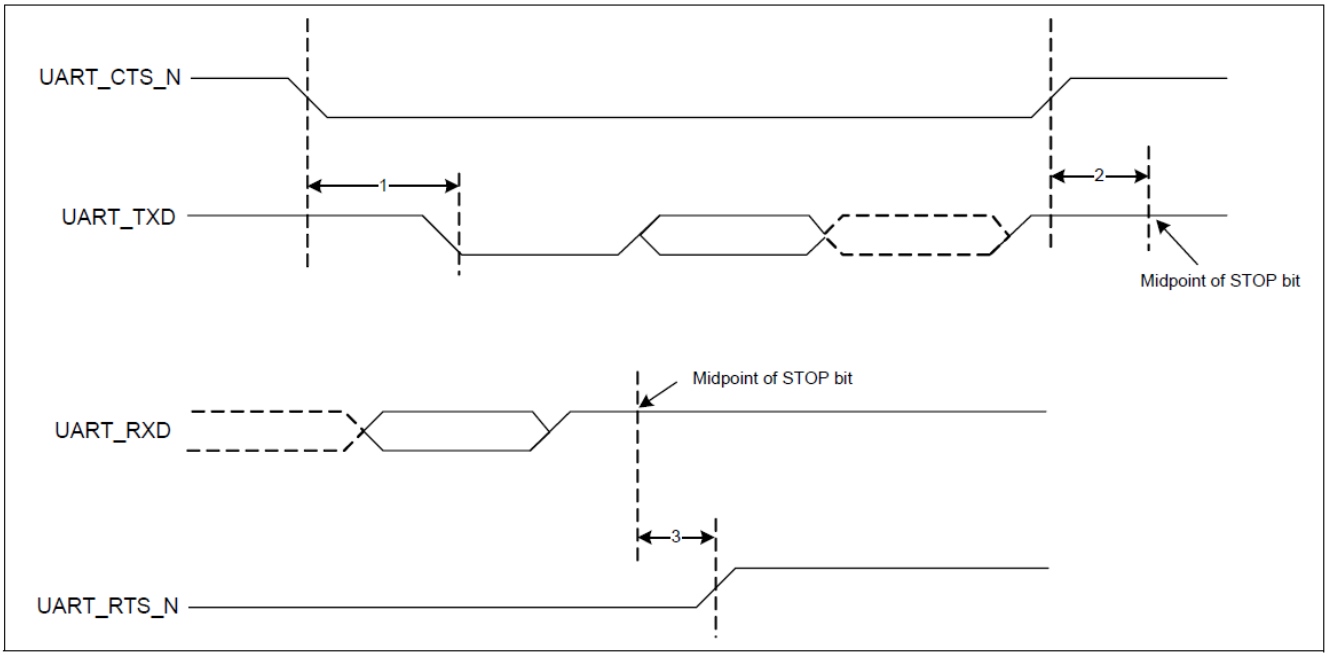
3.4 Host Interface

3.4.1 UART Timing

UART Timing Specifications

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid.	–	–	1.50	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit.	–	–	0.67	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high.	–	–	1.33	Bit periods

UART Timing

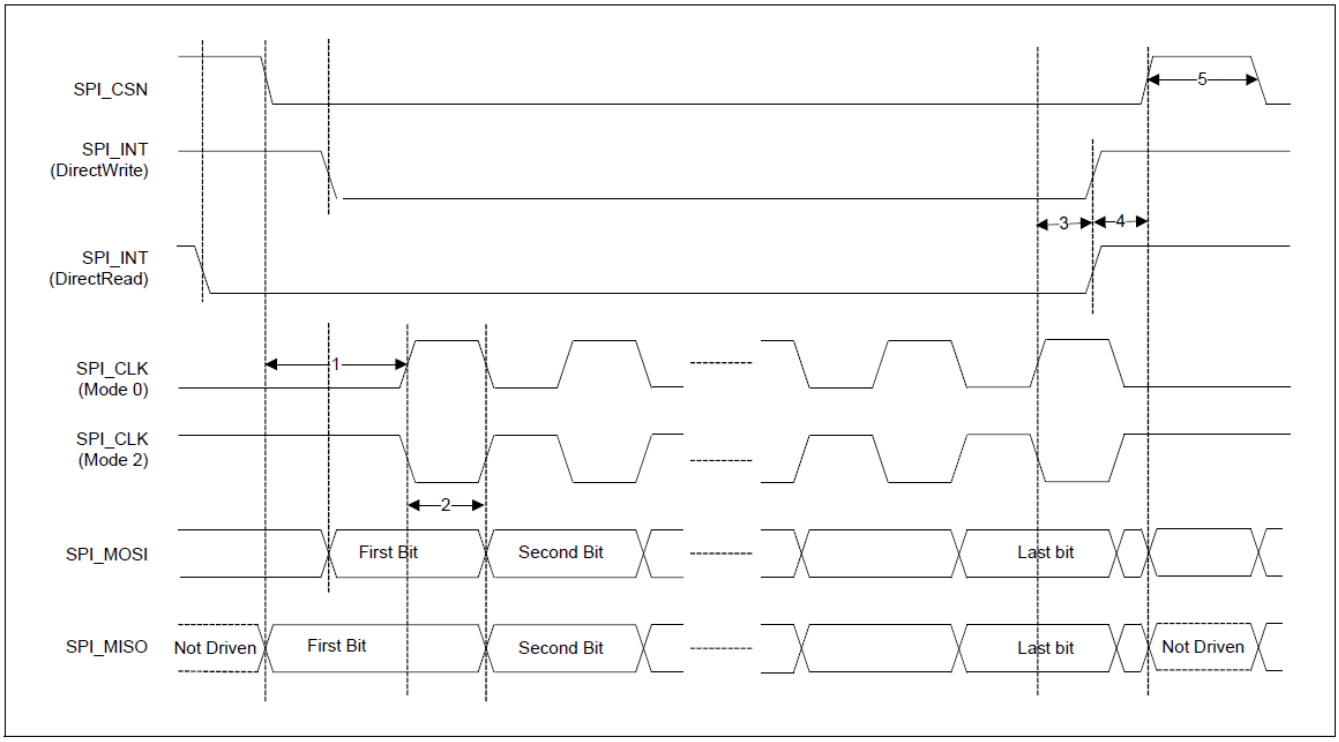


3.4.2 SPI Timing

SPI Mode 0 and 2

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

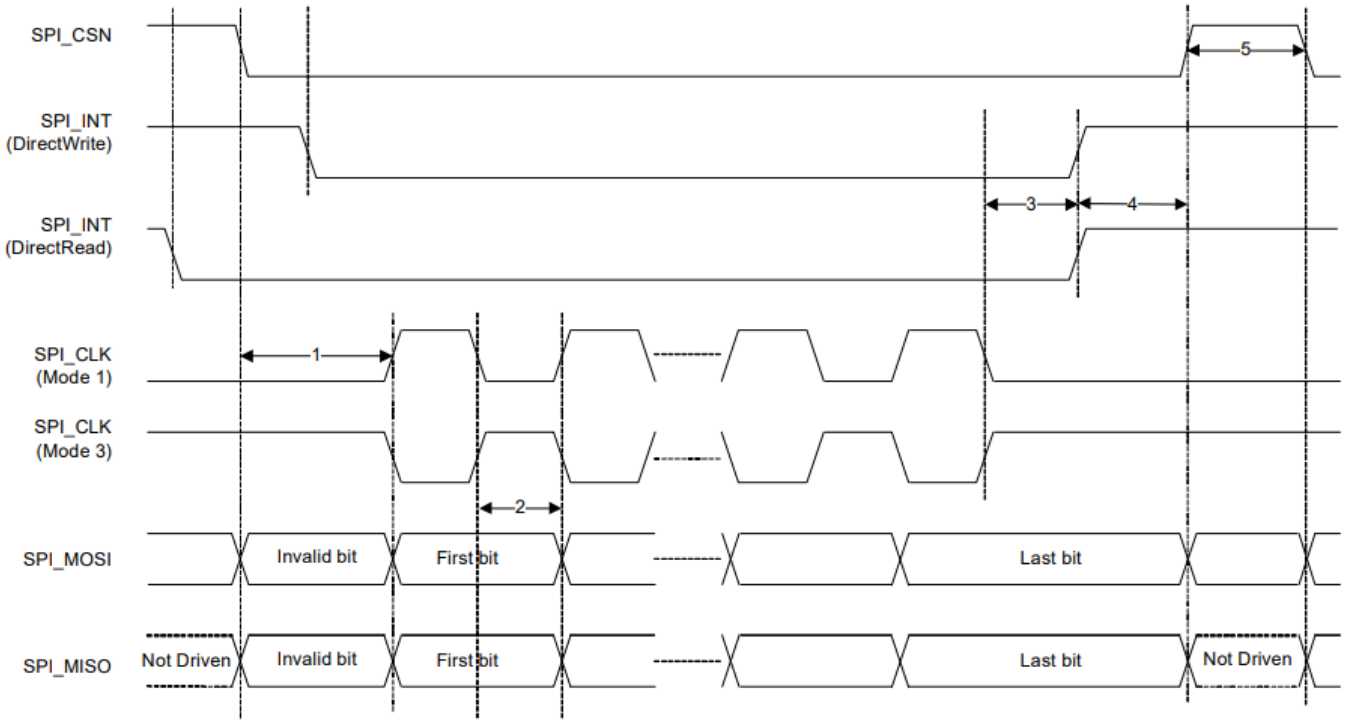
SPI Timing, Mode 0 and 2



SPI Mode 1 and 3

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

SPI Timing, Mode 1 and 3



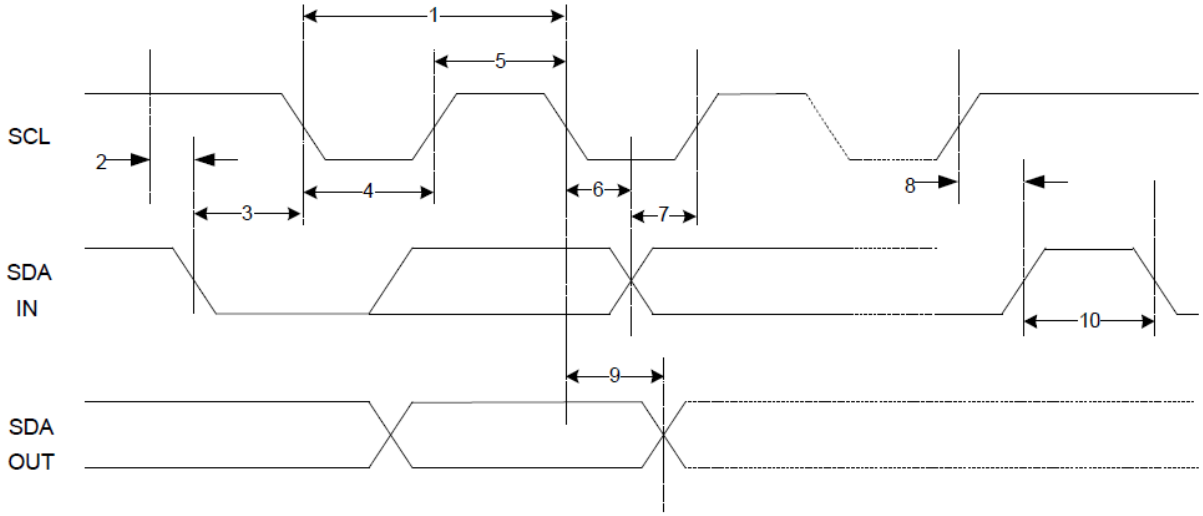
3.4.3 I2C Timing

I²C Compatible Interface Timing Specifications (up to 1 MHz)

Reference	Characteristics	Min.	Max.	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	
4	Clock low time	650	–	
5	Clock high time	280	–	
6	Data input hold time[23]	0	–	
7	Data input setup time	100	–	
8	STOP condition setup time	280	–	
9	Output valid from clock	–	400	
10	Bus free time[24]	650	–	

Notes
23. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
24. Time that the CBUS must be free before a new transaction can start.

I²C Interface Timing Diagram



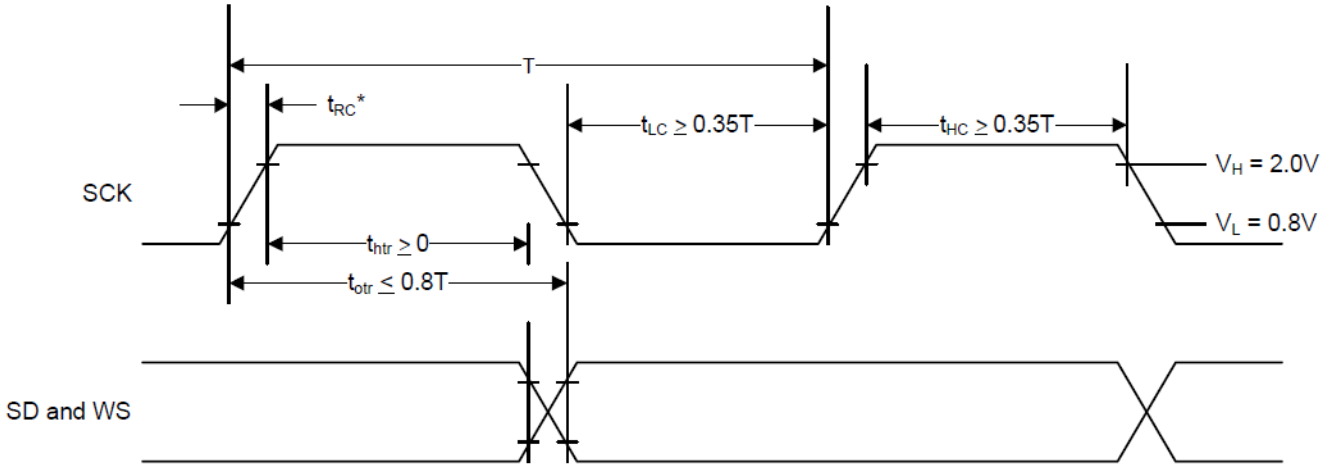
3.4.4 I2S Timing

Timing for I^2S Transmitters and Receivers

	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	[25]
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	[26]
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	[26]
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	[27]
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	[27]
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	[28]
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	[29]
Hold time t_{htr}	0	–	–	–	–	–	–	–	[28]
Receiver									
Setup time t_{sr}	–	–	–	–	$0.2T_{tr}$	–	–	–	[30]
Hold time t_{hr}	–	–	–	–	$0.2T_{tr}$	–	–	–	[30]

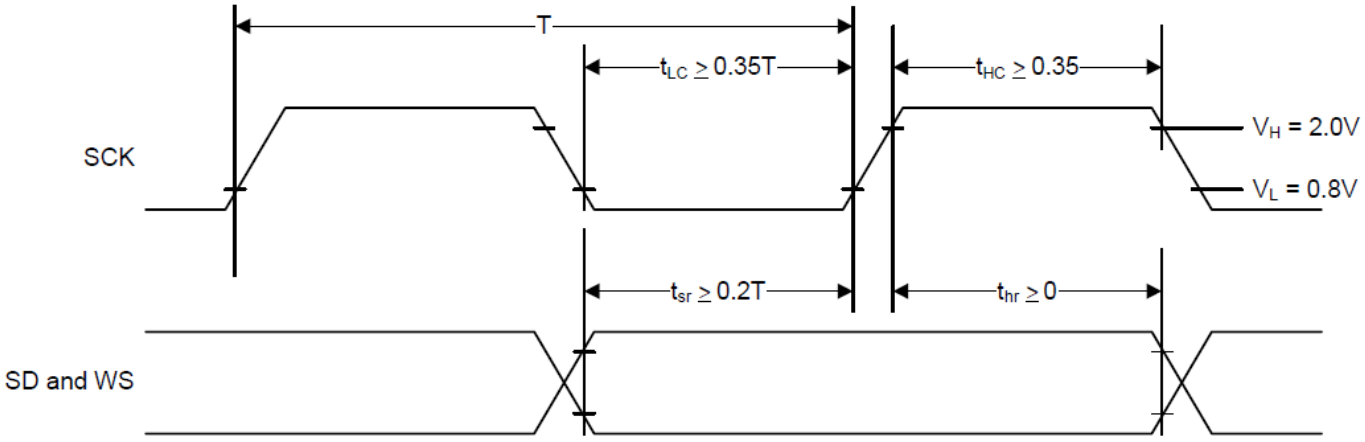
Note :
1. The system clock period T must be greater than Ttr and Tr because both the transmitter and receiver have to be able to handle the data transfer rate.
2. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, tHC and tLC are specified with respect to T.
3. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35Tr, any clock that meets the requirements can be used.
4. Because the delay (tdtr) and the maximum transmitter speed (defined by Ttr) are related, a fast transmitter driven by a slow clock edge can result in tdtr not exceeding tRC which means thtr becomes zero or negative. Therefore, the transmitter has to guarantee that thtr ≥ zero, so long as the clock rise-time tRC is not more than tRCmax, where tRCmax is not less than 0.15Ttr.
5. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
6. The data setup and hold time must not be less than the specified receiver setup and hold time.

I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

3.5 Power Consumption

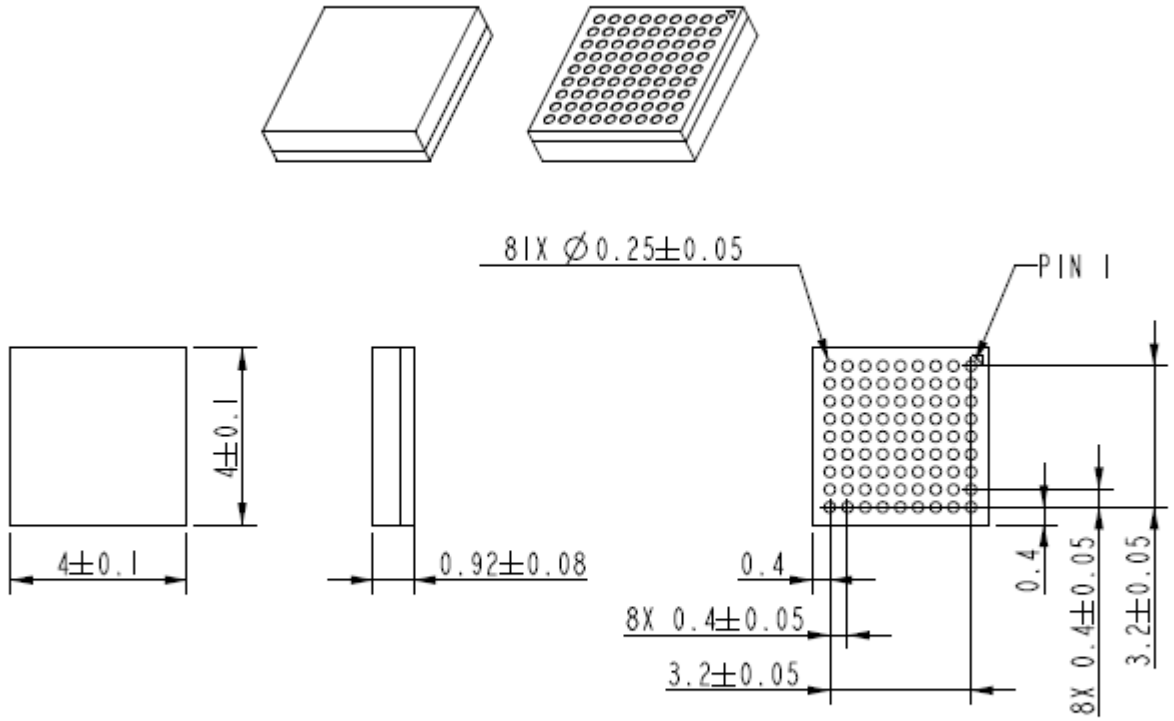
3.5.1 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	VDD3p3 = V	
				Max.	Avg.
1	Sleep	n/a	n/a	TBD	TBD
2	Transmit	DH5 / 3-DH5	n/a	TBD	TBD
3	Receive	DH5 / 3-DH5	n/a	TBD	TBD

No.	Mode	Packet Type	RF Power (dBm)	VDDIO = V	
				Max.	Avg.
1	Sleep	n/a	n/a	TBD	TBD
2	Transmit	DH5 / 3-DH5	n/a	TBD	TBD
3	Receive	DH5 / 3-DH5	n/a	TBD	TBD

4. Mechanical Information

4.1 Mechanical Drawing



5. Packaging Information