AW-HM662

IEEE 802.11ah Wireless LAN Module (US)

Datasheet

Rev. A

DF

(For STD)

Features

General

- Supports 902 ~ 928MHz frequency band
- Supports single-stream 150kbps ~ 15Mbps data rate
- Supports AP and STA mode

Host interface

- UART and HSPI support for host interface

Standards Supported

- IEEE Std 802.11ah standard
- Security: OPEN, WPA2-PSK(AES), WPA3-OWE, WPA3-SAE

MAC Features

- S1G Beacon, NDP Control frame, TIM compression, unified scaling factor for max Idle period/listen interval/WNM-sleep interval, STA Type, S1G baseline functions (DCF, HCF, multi-rate support, A-MPDU), and S1G BSS operation
- Network efficiency enhancements: NDP PS-Poll/PS-Poll Ack/Probe Req./Probe Resp., RAW avoidance, TSBTT, and differentiated EDCA Parameter
- Power saving: Non-TIM operation, dynamic AID assignment and TWT
- BSS scalability (up to 8192 STAs): Multicast AID, and authentication control
- Low-cost STA/AP: EL operation, Flow Control
- Supports transmission of Standby Radio frame

Peripheral Interfaces

- I2C, SPI and UART
- A Wi-Fi dedicated HSPI for data transfer to Host

Peripheral Interfaces

- Full IEEE 802.11ah compatibility with enhanced performance
- Single-stream up to 15Mbps data rate
- Supports 1/2/4 MHz channel with optional SGI
- Supports S1G_1M, Short/Long format
- Modulation: OFDM with BPSK, QPSK, 16QAM, 64QAM

Revision History

Document NO: R2-2662-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2025/02/12	DCN032266	● Initial version	Daniel Lee	N.C. Chen

AzureWave Technologies, Inc.

Table of Contents

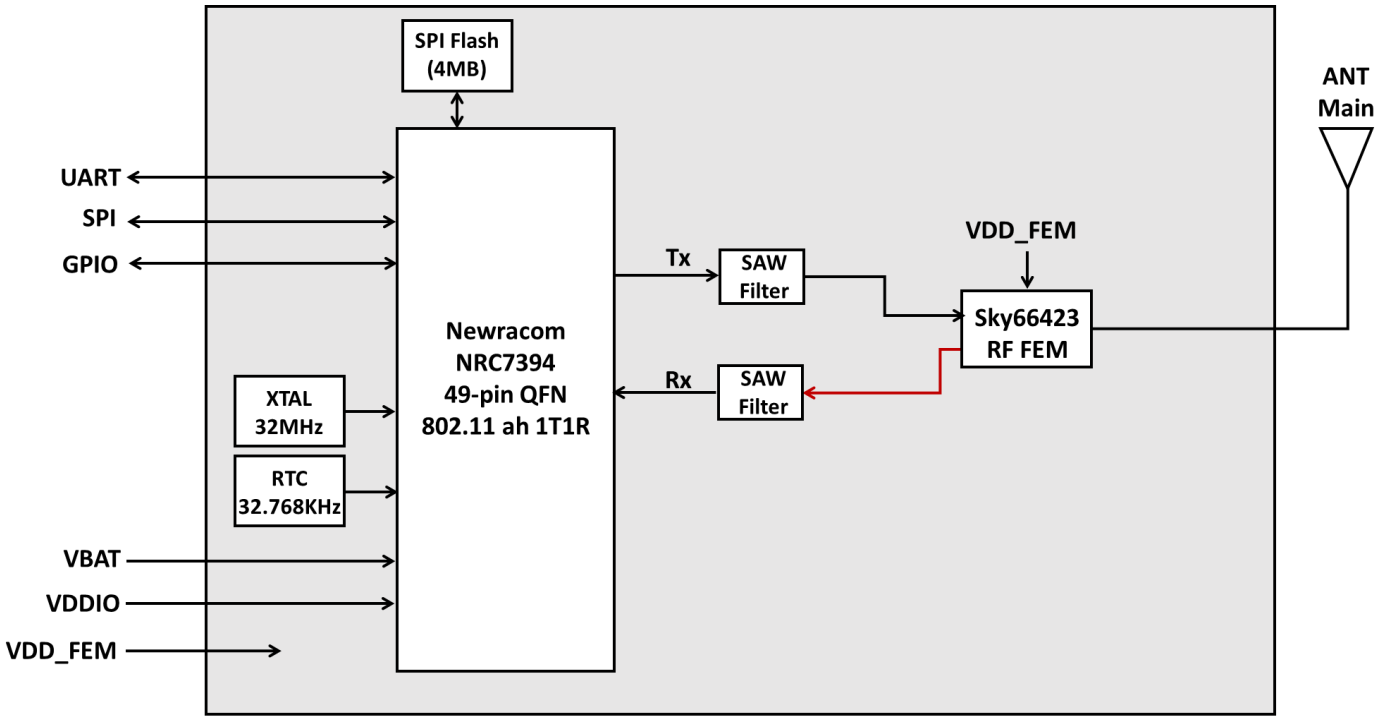
1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.11ah WIFI solder down module --- **AW-HM662**. The **AW-HM662** is the smallest IEEE 802.11ah Wi-Fi module that operates in the Sub 1GHz license-exempt band, offering longer ranger and higher data rate for internet of things (IoT) applications. The **AW-HM662** supports 1/2/4 MHz channel bandwidth which yields 150 Kbps to 15 Mbps PHY rate that can handle low-rate sensors to high-rate surveillance camera applications. The self-contained Wi-Fi networking with huge range of data throughput offers the ideal solution to add Wi-Fi connectivity to IoT products with low power consumption requirements.

The **AW-HM662** integrated Newracom NRC7394 which is a complete radio front-end that is optimized for Sub 1 GHz band. It has a fully integrated PA and fractional-N synthesizer. An embedded Cortex-M3 ARM® processor in the NRC7394 offers enough processing power to accommodate Wi-Fi subsystem as well as user application in a single Wi-Fi SoC. NRC7394 also includes two host interfaces, HSPI and UART, and rich peripherals such as general SPI, I2C, UART, PWM, auxiliary ADC, and GPIOs. The low-leakage retention memory inside NRC7394 can be used to store code and data necessary for fast wake-up from deep-sleep mode.

1.2 Block Diagram



AW-NRC7394 with RF FEM Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11ah Wireless LAN Module
Major Chipset	Newracom NRC7394 (49-pin QFN)
Host Interface	SPI
Dimension	18mm x 24mm x 2.29mm (Tolerance remarked in mechanical drawing)
Form Factor	LGA module, 74 pins
Antenna	● For LGA, “1T1R, external” ANT Main：TX/RX
Weight	1.8g

1.3.2 WLAN

Features	Description
WLAN Standard	IEEE 802.11ah
Frequency Range	US/CA: Unit MHz 1MHz Bandwidth: 902.5, 903.5, 904.5, 905.5, 906.5, 907.5, 908.5, 909.5, 910.5, 911.5, 912.5, 913.5, 914.5, 915.5, 916.5, 917.5, 918.5, 919.5, 920.5, 921.5, 922.5, 923.5, 924.5, 925.5, 926.5, 927.5 2MHz Bandwidth: 903, 905, 907, 909, 911, 913, 915, 917, 919, 921, 923, 925, 927 4MHz Bandwidth: 906, 910, 914, 918, 922, 926
Modulation	OFDM, BPSK, QPSK, 16-QAM, 64-QAM
Channel Bandwidth	1/2/4 MHz

<table>
<tr><td>Output Power
(Board Level Limit)*</td><td>US/CA
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>MCS0 (1/2/4 MHz)
@EVM≦-5dB</td><td>19.5</td><td>21</td><td>22.5</td><td>dBm</td></tr>
<tr><td>MCS7 (1/2/4 MHz)
@EVM≦-27dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Receiver Sensitivity</td><td>US/CA
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>MCS0 (1 MHz)</td><td>TBD</td><td>-99</td><td>-96</td><td>dBm</td></tr>
<tr><td>MCS0 (2 MHz)</td><td>TBD</td><td>-97</td><td>-94</td><td>dBm</td></tr>
<tr><td>MCS0 (4 MHz)</td><td>TBD</td><td>-94</td><td>-91</td><td>dBm</td></tr>
<tr><td>MCS7 (1 MHz)</td><td>TBD</td><td>-82</td><td>-79</td><td>dBm</td></tr>
<tr><td>MCS7 (2 MHz)</td><td>TBD</td><td>-79</td><td>-76</td><td>dBm</td></tr>
<tr><td>MCS7 (4 MHz)</td><td>TBD</td><td>-76</td><td>-73</td><td>dBm</td></tr>
</table></td></tr>
<tr><td>Data Rate</td><td>■ 1 MHz Bandwidth: up to 3Mbps
■ 2 MHz Bandwidth: up to 6.5Mbps
■ 4 MHz Bandwidth: up to 13.5Mbps</td></tr>
<tr><td>Security</td><td>■ OPEN, WPA2-PSK(AES), WPA3-OWE, WPA3-SAE
standard</td></tr>
</table>

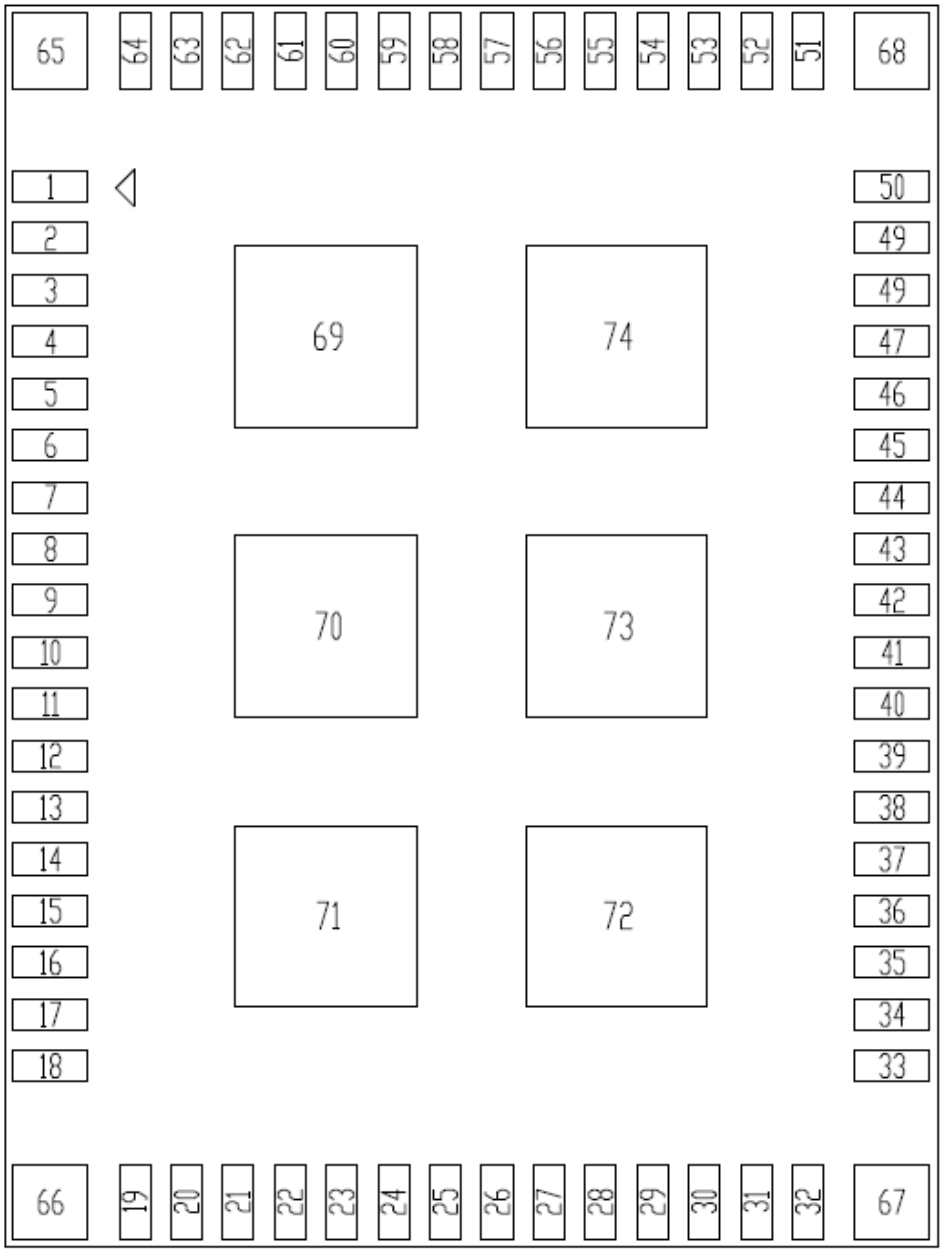
*** If you have any certification questions about output power please contact FAE directly.**
*** Output power and receiver sensitivity is based on VBAT with +/- 5% of typical value.**

1.3.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT: 3.3V VDD_FEM: 4.0V VDDIO: 3.3V
Operating Temperature	-40℃~85 ℃
Operating Humidity	less than 85%R.H
Storage Temperature	-40℃~85 ℃
Storage Humidity	less than 60%R.H
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

2. Pin Definition

2.1 Pin Map



AW-HM662 Pin Map (Top View)

2.2 Pin Table

Pin No.	Definition	Basic Description	Voltage	Type
1	GND	GROUND		GND
2	GND	GROUND		GND
3	GND	GROUND		GND
4	GND	GROUND		GND
5	VDD_FEM	Front End Module power input	4.0V	Power
6	VBAT	3.3V power supply	3.3V	Power
7	GND	GROUND		GND
8	GND	GROUND		GND
9	NC	No Connection		-
10	NC	No Connection		-
11	MODE	0: Host Mode / MFG Mode 1: Standalone Mode		I
12	NC	No Connection		-
13	NC	No Connection		-
14	GND	GROUND		GND
15	HSPI_CSn	Host SPI – Chip Select (active low)		I
16	HSPI_CLK	Host SPI – Clock		I
17	HSPI_MISO	Host SPI – Master in Slave out		O
18	HSPI_MOSI	Host SPI – Master out Slave in		I
19	HSIP_EIRQ	Host SPI – Interrupt		O
20	GND	GROUND		GND
21	GND	GROUND		GND
22	GP12 / UART1_TXD	UART Channel1 Tx		O
23	GP13 / UART1_RXD	UART Channel1 Rx		I
24	GP20 / UART1_RTS	UART Channel1 RTS		O
25	GP14 / UART1_CTS	UART Channel 1 CTS		I

26	NC	No Connection		-
27	NC	No Connection		-
28	GP8 / UART0_TXD	UART Channel0 Tx		O
29	GP9 / UART0_RXD	UART Channel0 Rx		I
30	NC	No Connection		-
31	NC	No Connection		-
32	I2C_SDA	I2C_SDA		I/O
33	NC	No Connection		-
34	NC	No Connection		-
35	I2C_SCL	I2C_SCL		I/O
36	NC	No Connection		-
37	NC	No Connection		-
38	NC	No Connection		-
39	NC	No Connection		-
40	RESET	Reset (active high)		I
41	GND	GROUND		GND
42	GP14 / JTAG_TRSTn	JTAG Reset		I
43	GP10 / JTAG_TMS	JTAG Mode Selection		I
44	GP11 / JTAG_TCK	JTAG Clock		I
45	GP13 / JTAG_TDI	JTAG Data Input		I
46	GP12 / JTAG_TDO	JTAG Data Output		O
47	GND	GROUND		GND
48	GND	GROUND		GND
49	RF_ANT	RF IN/OUT		I/O
50	GND	GROUND		GND
51	VDDIO	I/O supply Input		Power
52	GND	GROUND		GND
53	GND	GROUND		GND

54	NC	No Connection		-
55	GP18 / AUXADCIN1	AUXADC Input 2		I
56	GP17 / AUXADCIN0	AUXADC Input 1		I
57	GND	GROUND		GND
58	GP15 / CTX	RF Tx/Rx Switch Selection		I
59	GP16 / CSD	RF FEM Power Down Control		I
60	GND	GROUND		GND
61	GND	GROUND		GND
62	GND	GROUND		GND
63	GND	GROUND		GND
64	GND	GROUND		GND
65	GND	GROUND		GND
66	GND	GROUND		GND
67	GND	GROUND		GND
68	GND	GROUND		GND
69	GND	GROUND		GND
70	GND	GROUND		GND
71	GND	GROUND		GND
72	GND	GROUND		GND
73	GND	GROUND		GND
74	GND	GROUND		GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_FEM	Front End Module power input	-0.5	-	5.25	V
VBAT	3.3V power supply	-0.5		3.8	
VDDIO	I/O supply Input	-0.5		3.8	
T_{stg}	Storage temperature	-40	-	85	℃

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_FEM	Front End Module power input	3.8	4.0	4.2	V
VBAT	3.3V power supply	3.135	3.3	3.465	V
VDDIO	3.3V I/O supply Input	3.0	3.3	VBAT	V
VDDIO	1.8V I/O supply Input	1.68	1.8	1.92	V

3.3 Digital IO Pin DC Characteristics

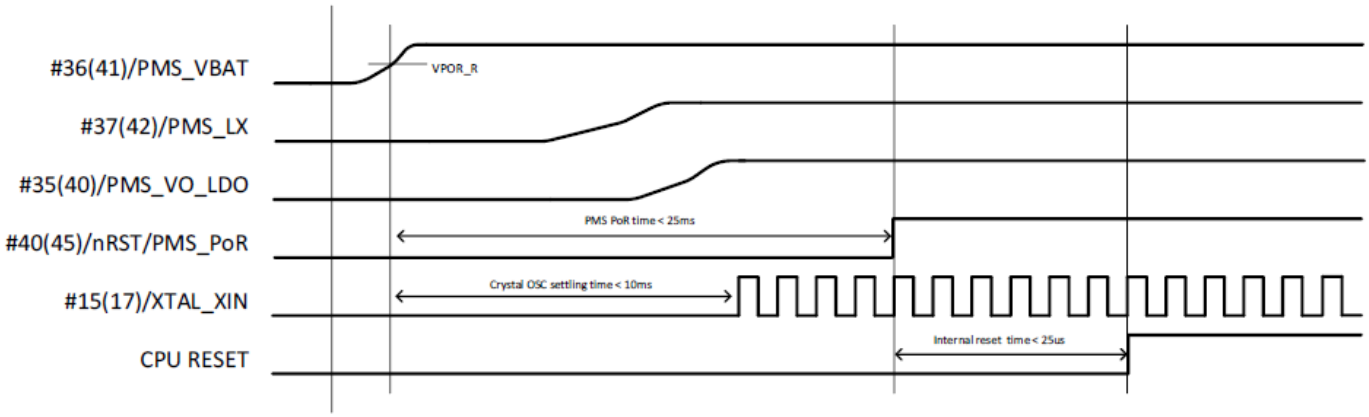
VDDIO = 3.3V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	2	-	3.6	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{OH}	Output high voltage	2.4	-		V
V_{OL}	Output low voltage		-	0.4	V

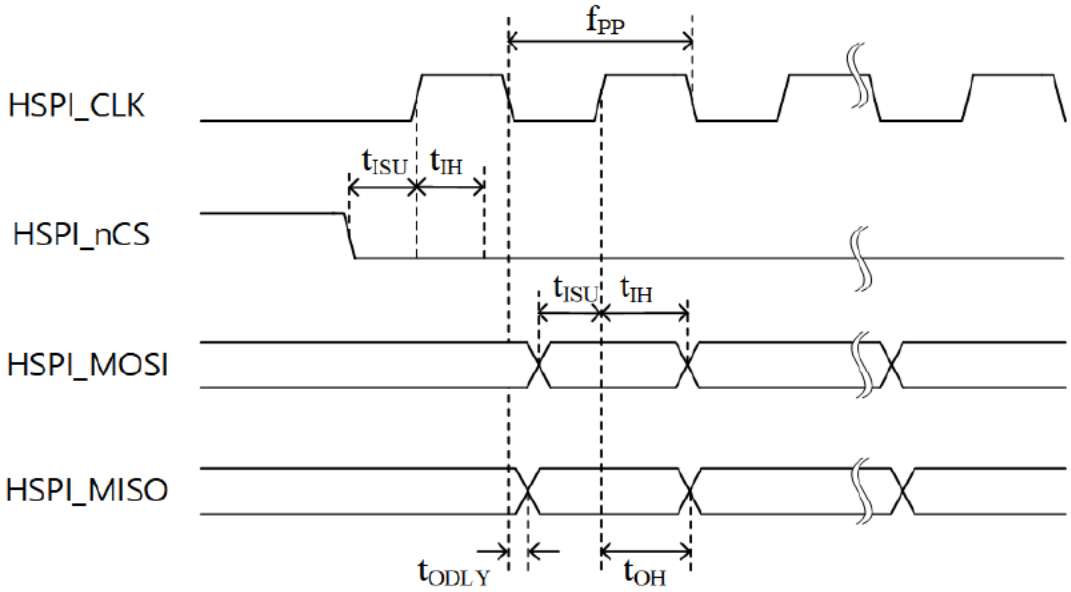
3.4 Timing Sequence

3.4.1 Power on sequence

The figure below shows the module power on sequence. The start of the POR circuit in the PMS block and BUCK oscillator are triggered by VBAT when the level exceeds a predefined voltage level. The main 32 MHz crystal oscillator starts to run when the internal power supply is stable. The PMS_PoR (active low) is de-asserted after a pre-defined settling time for stable crystal oscillation to ensure reliable SoC operation. PMS_PoR is open-drain circuit with internal pull-up resistor and connected with external RSTn pin. When the PMS_PoR releases RSTn pin to HIGH, the power-on sequence is completed and the SoC can control the entire system after the internal 25usec reset time.

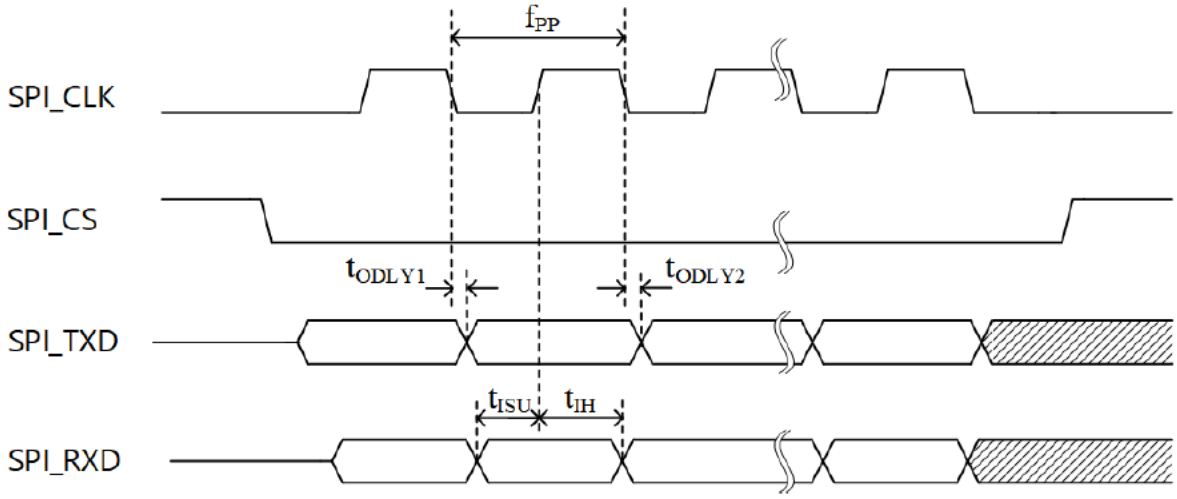


3.4.2 HSPI Timing



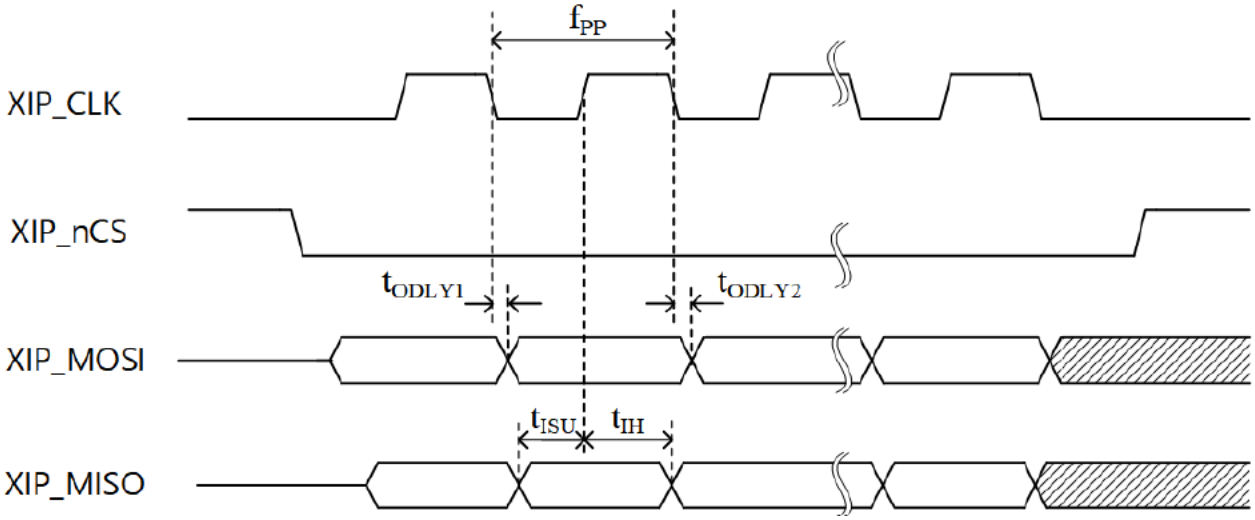
Symbol	Parameter	Min	Typ	Max	Unit
f_{PP}	Frequency	-	-	20	MHz
t_{ODLY}	Output delay time	2.7	-	20.2	ns
t_{OH}	Output hold time	25	-	-	ns
t_{ISU}	Input setup time	-	-	21.6	ns
t_{IH}	Input hold time	5.8	-	-	ns

3.4.3 SPI Timing



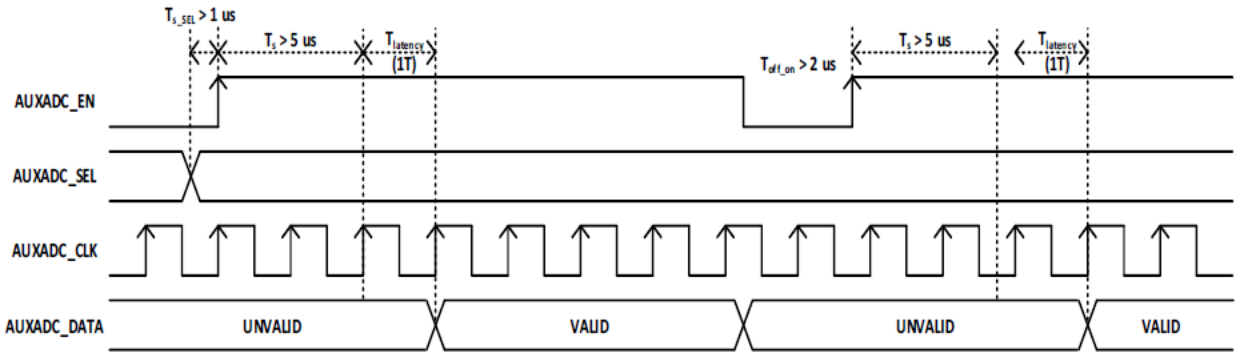
Symbol	Parameter		Min	Typ	Max	Unit
f_{PP}	Frequency	master	-	-	16	MHz
		slave	-	-	2	MHz
t_{ODLY1}	Output delay time1		0	-	23	ns
t_{ODLY2}	Output delay time2		0	-	23	ns
t_{ISU}	Input setup time		18	-	-	ns
t_{IH}	Input hold time		20	-	-	ns

3.4.4 XIP(eXecute In Place) Timing



Symbol	Parameter	Min	Typ	Max	Unit
f_{PP}	Frequency	-	-	32	MHz
t_{ODLY1}	Output delay time1	0	-	15	ns
t_{ODLY2}	Output delay time2	0	-	15	ns
t_{ISU}	Input setup time	-	-	5.1	ns
t_{IH}	Input hold time	7.7	-	-	ns

3.4.5 AUXADC Timing



Symbol	Parameter	Min	Typ	Max	Unit
Input Range	Input signal range	0.1		0.9	V
Output Range	Output Code Range (After s/w compensation)	100		900	10-bit
FS	Sampling Clock	-	2	-	MHz
Latency	Conversion latency (1 cycle = T)	-	1	-	cycle
N	Resolution	-	10	-	Bit
RIN	Input impedance	-	4	-	Mohms
Ts	Settling time after enable	5			us
Ts_sel	Setup time of AUXADC_SEL	1			us
Toff_on	Reset time	2			us
I_active	Current consumption (1.1 V)	-	-	150	uA
I_down	Power-down current (1.1 V)	-	-	2	uA

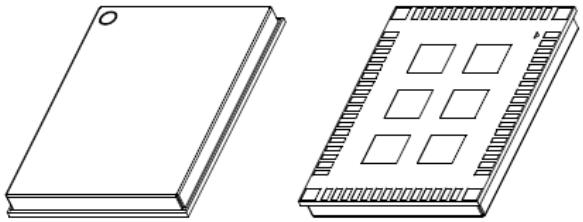
3.5 Power Consumption

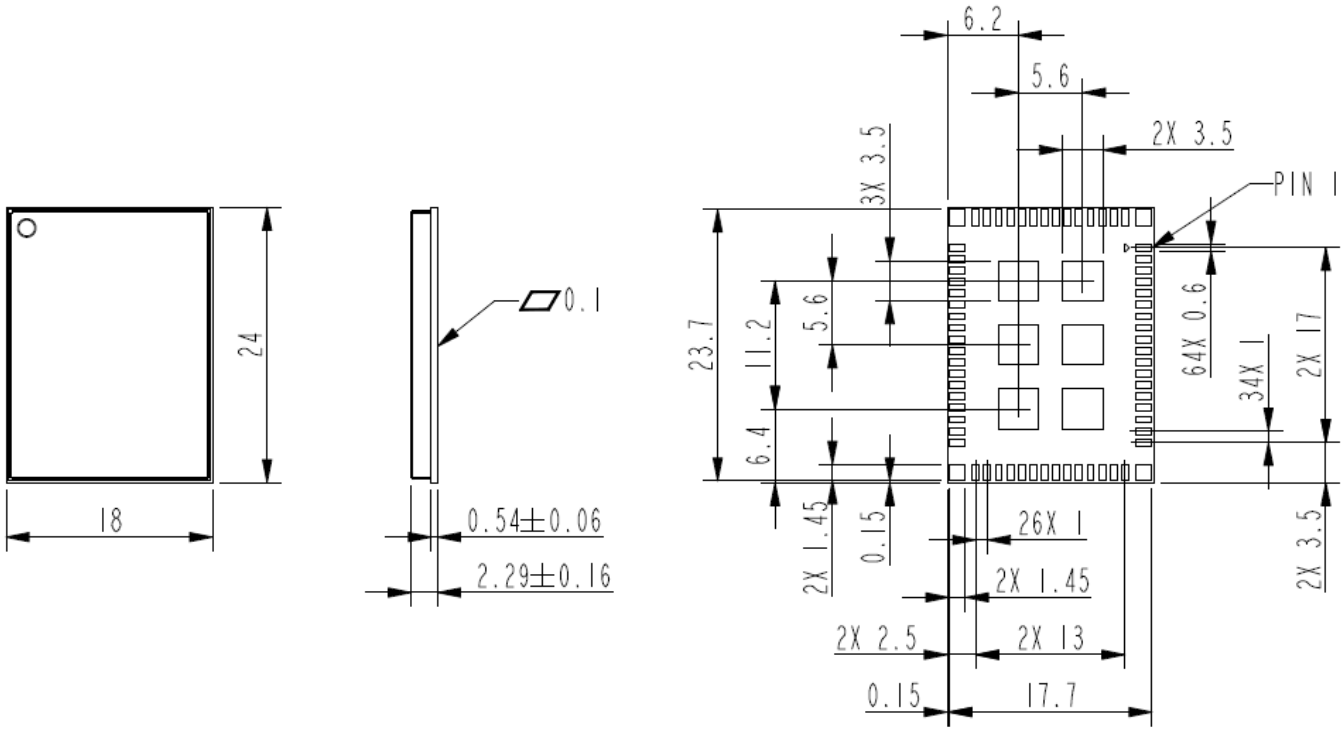
3.5.1 Current Consumption Results

MODE	DUT Status	VDDIO 3.3V (mA)	VBAT 3.3V (mA)	VDD_FEM 3.3V (mA)
802.11ah (1/2/4MHz BW)	**Tx@13dBm**	TBD	TBD	TBD
	Tx@16dBm	TBD	TBD	TBD
	Tx@21dBm	TBD	TBD	TBD
	Continuous Rx @ -85 dBm	TBD	TBD	TBD
	Deep Sleep mode	TBD	TBD	TBD

4. Mechanical Information

4.1 Mechanical Drawing





5. Package information