

AW-HM581

IEEE 802.11ah Wireless LAN Module

Datasheet

Rev. C

DF

(For STD)

Features

General

- Support 902 ~ 928MHz frequency band
- Support single-stream data rate up to 32.5Mbps @8MHz or 15 Mbps @4MHz channel
- Support channel width options of 1/2/4/8 MHz
- Support Modulation and Coding Scheme (MCS) levels MCS 0-7 and MCS 10
- Modulation: BPSK & QPSK, 16-QAM & 64 - QAM
- Support for 1 MHz and 2 MHz duplicate modes

Host interface

- SDIO 2.0 (slave) Default Speed (DS) at 25MHz
- SDIO 2.0 (slave) High Speed (HS) at 50MHz
- Support for both 1-bit and 4-bit data mode
- Support for SPI mode operation

Standards Supported

- IEEE Std 802.11ah-2016 compliant

Security Features

- AES encryption engine
- Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
- WPA3 including protected management

frames (PMF)

- Opportunistic Wireless Encryption (OWE)

Peripheral Interfaces

- SDIO/SPI, I2C and UART
- Support for STA and AP roles



AzureWave Technologies, Inc.

Revision History

Document NO: R2-2581-DST-01

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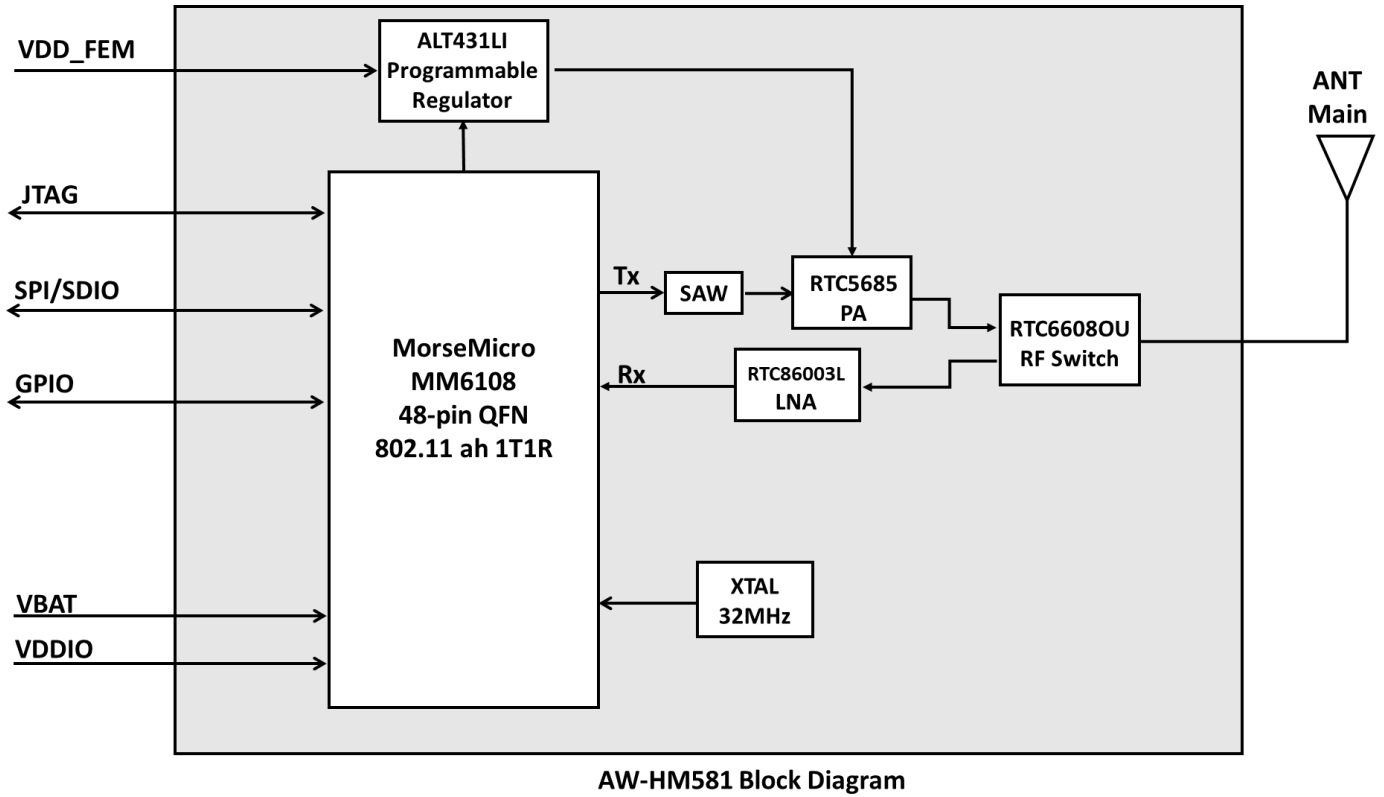
1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.11ah WIFI LGA module --- **AW-HM581**. The **AW-HM581** is an IEEE 802.11ah Wi-Fi module designed in compliance with the IEEE 802.11ah standard, supporting data rates up to 32.5 Mbps that operates in the Sub 1GHz license-exempt band, offering longer range and higher data rate for internet of things (IoT) applications. The **AW-HM581** enables streamlined data transfer interoperability with existing Wi-Fi networks while meeting up to 1Km long range data transfer with low power consumption requirements.

The **AW-HM581** integrated IEEE 802.11ah Sub-1G 8MHz Single-chip MAC/PHY/Radio SoC Morse Micro MM6108, ultra-long-reach PA, high linearity LNA, T/R switch, 32 MHz crystal and it has been designed for a simplified Wi-Fi HaLow connection to an external host for applications in which a customer wants to merely replace their prior RF technology with a Wi-Fi HaLow connection while leveraging the latest WPA3 security protocol. **AW-HM581** supports SDIO 2.0 compliant slave interface and SPI mode operation, and many peripherals such as general I2C, UART and GPIOs. In addition, its MAC supports for STA and AP roles.

1.2 Block Diagram



1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11ah Wireless LAN Module
Major Chipset	Morse Micro MM6108 (48-pin QFN)
Host Interface	SDIO/SPI
Dimension	13mm x 13mm x 2.1mm (Tolerance remarked in mechanical drawing)
Form Factor	LGA module, 44 pins
Antenna	<ul style="list-style-type: none"> For Stamp Module, "1T1R, external" ANT Main : TX/RX
Weight	0.7g

1.3.2 WLAN

Features	Description				
WLAN Standard	IEEE 802.11ah				
WLAN VID/PID	TBD				
WLAN SVID/SPID	TBD				
Frequency Rage	US (902.5 – 926.5 MHz)				
Modulation	OFDM, BPSK, QPSK, 16-QAM, 64-QAM				
Channel Bandwidth	1/2/4/8 MHz				
Output Power (Board Level Limit)*		Min	Typ	Max	Unit
	MCS0 (1/2/4/8 MHz) @EVM≤-5dB		TBD		dBm
	MCS7 (1/2/4/8 MHz) @EVM≤-27dB		TBD		dBm

Receiver Sensitivity		Min	Typ	Max	Unit
	MCS0 (1 MHz)		TBD		dBm
	MCS0 (2 MHz)		TBD		dBm
	MCS0 (4 MHz)		TBD		dBm
	MCS0 (8 MHz)		TBD		dBm
	MCS7 (1 MHz)		TBD		dBm
	MCS7 (2 MHz)		TBD		dBm
	MCS7 (4 MHz)		TBD		dBm
	MCS7 (8 MHz)		TBD		dBm
Data Rate	<ul style="list-style-type: none"> 1 MHz Bandwidth: up to 3.333Mbps 2 MHz Bandwidth: up to 7.222Mbps 4 MHz Bandwidth: up to 15Mbps 8 MHz Bandwidth: up to 32.5Mbps 				
Security	<ul style="list-style-type: none"> AES encryption engine Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512) WPA3 including protected management frames (PMF) Opportunistic Wireless Encryption (OWE) 				

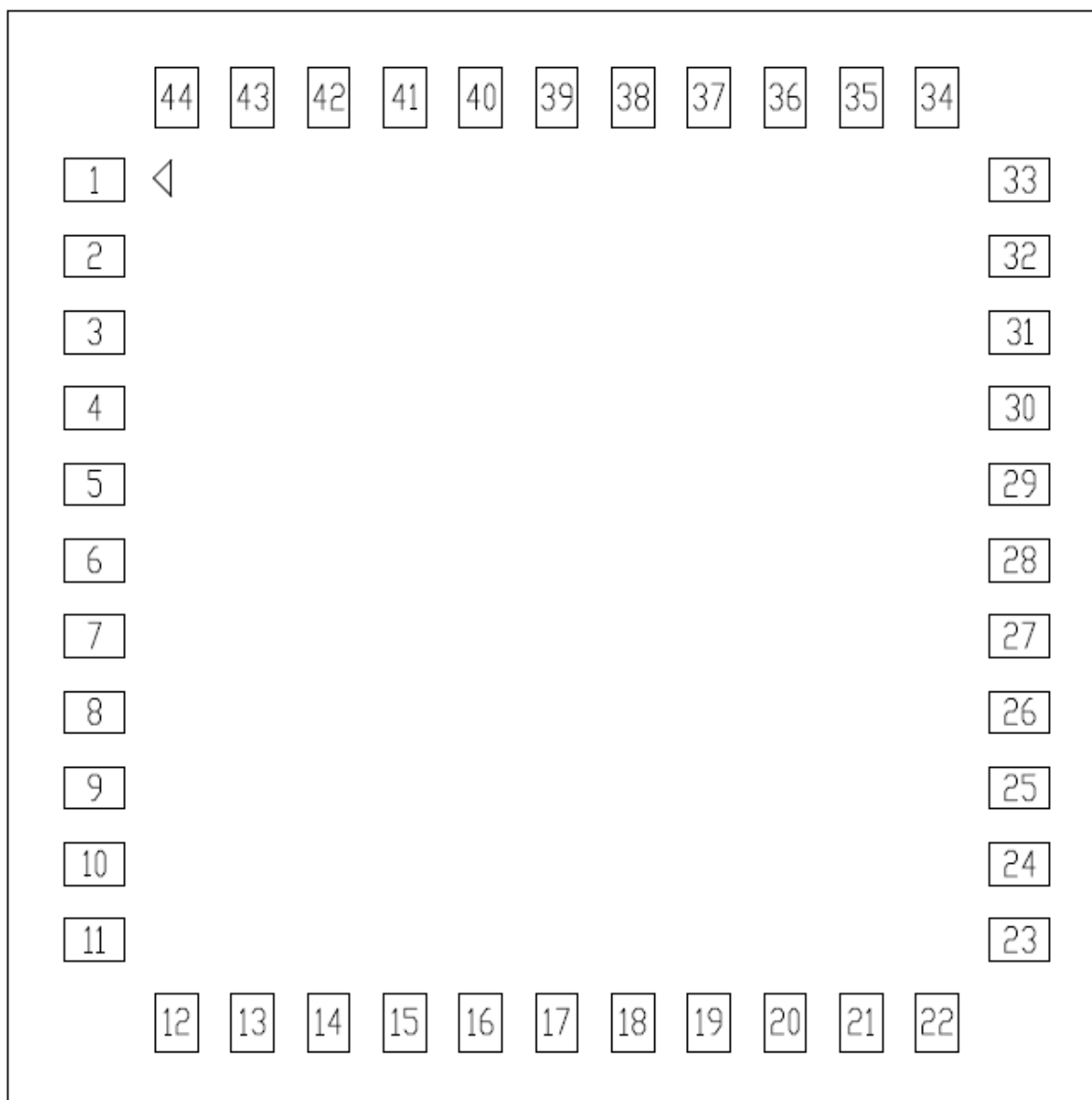
*** If you have any certification questions about output power please contact FAE directly.**

1.3.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT: 3.3V VDDIO: 3.3V
Operating Temperature	-40°C ~ 85 °C
Operating Humidity	less than 85%R.H
Storage Temperature	-40°C ~ 90 °C
Storage Humidity	less than 60%R.H
ESD Protection	
Human Body Model	TBD
Changed Device Model	TBD

2. Pin Definition

2.1 Pin Map



AW-HM581 Pin Map (Top View)

2.2 Pin Table

Pin No.	Definition	Basic Description	Voltage	Type
1	GND	GROUND		GND
2	ANT	RF IN/OUT		I/O
3	GND	GROUND		GND
4	NC	No Connection		
5	NC	No Connection		
6	MM_WAKE	WAKE from sleep		I
7	NC	No Connection		
8	NC	No Connection		
9	VBAT	3.3V power supply	3.3V	Power
10	GND	GROUND		GND
11	GND	GROUND		GND
12	MM_RESET_N	Reset (active low)		I/O
13	NC	No Connection		
14	MM_SD_D2	SDIO Data pin 2		I/O
15	MM_SD_D3	SDIO Data pin 3		I/O
16	MM_SD_CMD	SDIO Command pin		I/O
17	MM_SD_CLK	SDIO Clock pin (input)		I
18	MM_SD_D0	SDIO Data pin 0		I/O
19	MM_SD_D1	SDIO Data pin 1		I/O
20	GND	GROUND		GND
21	NC	No Connection		
22	VDDIO	I/O supply Input	3.3V	Power
23	NC	No Connection		

24	NC	No Connection		I
25	MM_GPIO6	General purpose I/O		I/O
26	MM_GPIO5	General purpose I/O		I/O
27	MM_GPIO4	General purpose I/O		I/O
28	MM_GPIO3	General purpose I/O		I/O
29	MM_GPIO2	General purpose I/O		I/O
30	MM_GPIO1	General purpose I/O		I/O
31	GND	GROUND		GND
32	MM_GPIO7	General purpose I/O		I/O
33	GND	GROUND		GND
34	MM_GPIO11	General purpose I/O		I/O
35	MM_GPIO10	General purpose I/O		I/O
36	GND	GROUND		GND
37	MM_GPIO9	General purpose I/O		I/O
38	MM_GPIO8	General purpose I/O		I/O
39	MM_JTAG_TDO	JTAG data output		O
40	MM_GPIO0	General purpose I/O		I/O
41	MM_JTAG_TMS	JTAG mode selection		I
42	MM_JTAG_TDI	JTAG data input		I
43	MM_JTAG_TRST	JTAG reset		I
44	MM_JTAG_TCK	JTAG clock		I

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.3V power supply	-0.5	-	4.3	V
VDDIO	I/O supply Input	-0.5	-	4.3	V
T _{stg}	Storage temperature	-40	-	90	°C

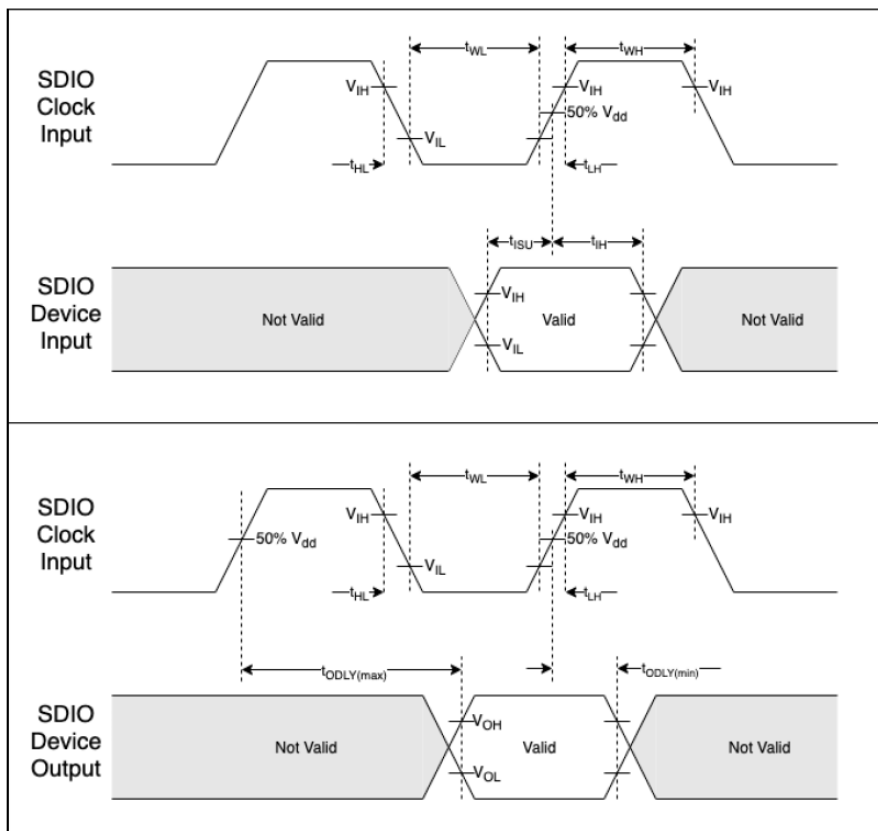
3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.3V power supply	3.0	3.3	3.6	V
VDDIO	3.3V I/O supply Input	3.0	3.3	3.6	V
T _{AMBIENT}	Ambient temperature	-40	25	85	°C

3.3 Timing Sequence

3.3.1 SDIO Bus Timing

The SDIO clock rate supports up to 50MHz. The device always operates in SD high speed mode.



Parameter	Min	Max
Clock parameters		
Clock frequency	0MHz	50MHz
Clock low time (t_{WL})	7ns	
Clock high time(t_{WH})	7ns	
Clock rise time (t_{LH})		3ns
Clock fall time (t_{HL})		3ns
Inputs on CMD, DAT lines to device from host		
Input setup time (t_{ISU})	6ns	
Input hold time (t_{IH})	2ns	
Outputs on CMD, DAT lines from device to host		
Output delay ($t_{ODLY(max)}$)		14ns
Output hold time ($t_{ODLY(min)}$)	2.5ns	
Total system capacitance for each line		40pF

3.3.2 SPI Bus

The SPI clock rate supports up to 50MHz. The SPI bus timing is identical to the SDIO bus timing, where MOSI and MISO are considered input and output timing, respectively, in the SDIO timing specification.

The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per SDIO high-speed mode. It may be configured to behave like CPHA=0 (drive output on negative edge, sample on positive edge) after being initialized.

3.3.3 UART Bus

Two universal asynchronous receiver/transmitter (UARTs) are available and provide a means for serial communication to off-chip devices. The UART cores are as-provided by the SiFive IP repository. The UART peripheral does not support hardware flow control or other modem control signals, or synchronous serial data transfers.

We will clock the UARTs with a maximum clock speed of 30MHz (TBD), meaning maximum baud of the UART will be around 30Mbaud or 30Mbits/s if a divisor of 0 is specified.

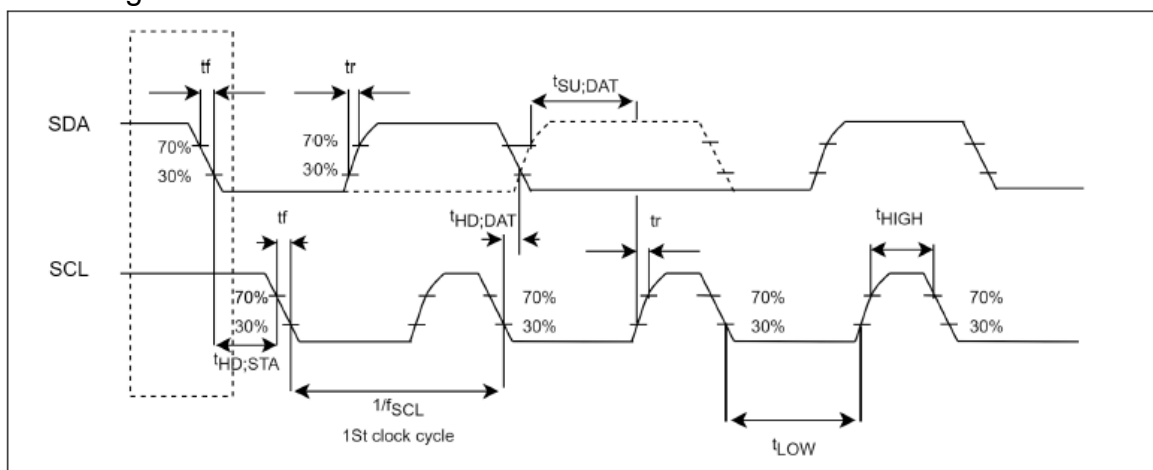
Pin	Name	Default Function	I/O Function
32	MM_GPIO7	GPIO	UART1 Tx
25	MM_GPIO6	GPIO	UART1 Rx
28	MM_GPIO3	GPIO	UART0 Tx
29	MM_GPIO2	GPIO	UART0 Rx

3.3.4 I2C Bus Timing

An I2C master interface is available. It consists of two lines, SDA and SCL, which are bidirectional, connected to a positive supply voltage via a current-source or pull-up resistor.

Pin	Name	Default Function	I/O Function
27	MM_GPIO4	GPIO	I2C SDA
26	MM_GPIO5	GPIO	I2C SCL

Definition of timing for F/S-mode devices on the I2C-bus. All values referred to



$V_{IH(min)}(0.3V_{DD})$ and $V_{IL(max)}(0.7V_{DD})$ levels.

Parameter	Standard-mode		Fast-mode	
	Min	Max	Min	Max
Clock frequency(f_{SCL})	0	100kHz	0	400kHz
Fall time of both SDA and SCL (t_f)	-	300ns	20x ($V_{DD}/5.5V$)	300ns
Rise time of both SDA and SCL signals(t_r)	-	1000ns	20ns	300ns
Data hold time ($t_{HD;DAT}$)	5.0us	-	-	-
Data set-up time ($t_{SU;DAT}$)	250ns	-	100ns	-
LOW period of the SCL clock	4.7us	-	1.3us	-
HIGH period of the SCL clock	4.0us	-	0.6us	-
Hold time- START,first clock is generated after this($t_{HD;STA}$)	4us	-	0.6us	-

3.4 Power Consumption

3.4.1 Transmit Power Consumption

Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V, VDDIO = 3.3V	
				VBAT (mA)	
				Max.	Avg.
915	MCS0	1	Tx @ 23 dBm	TBD	TBD
		2		TBD	TBD
		4		TBD	TBD
		8		TBD	TBD
	MCS7	1	Tx @ 17 dBm	TBD	TBD
		2		TBD	TBD
		4		TBD	TBD
		8		TBD	TBD

* The power consumption is based on AzureWave test environment, these data for reference only.

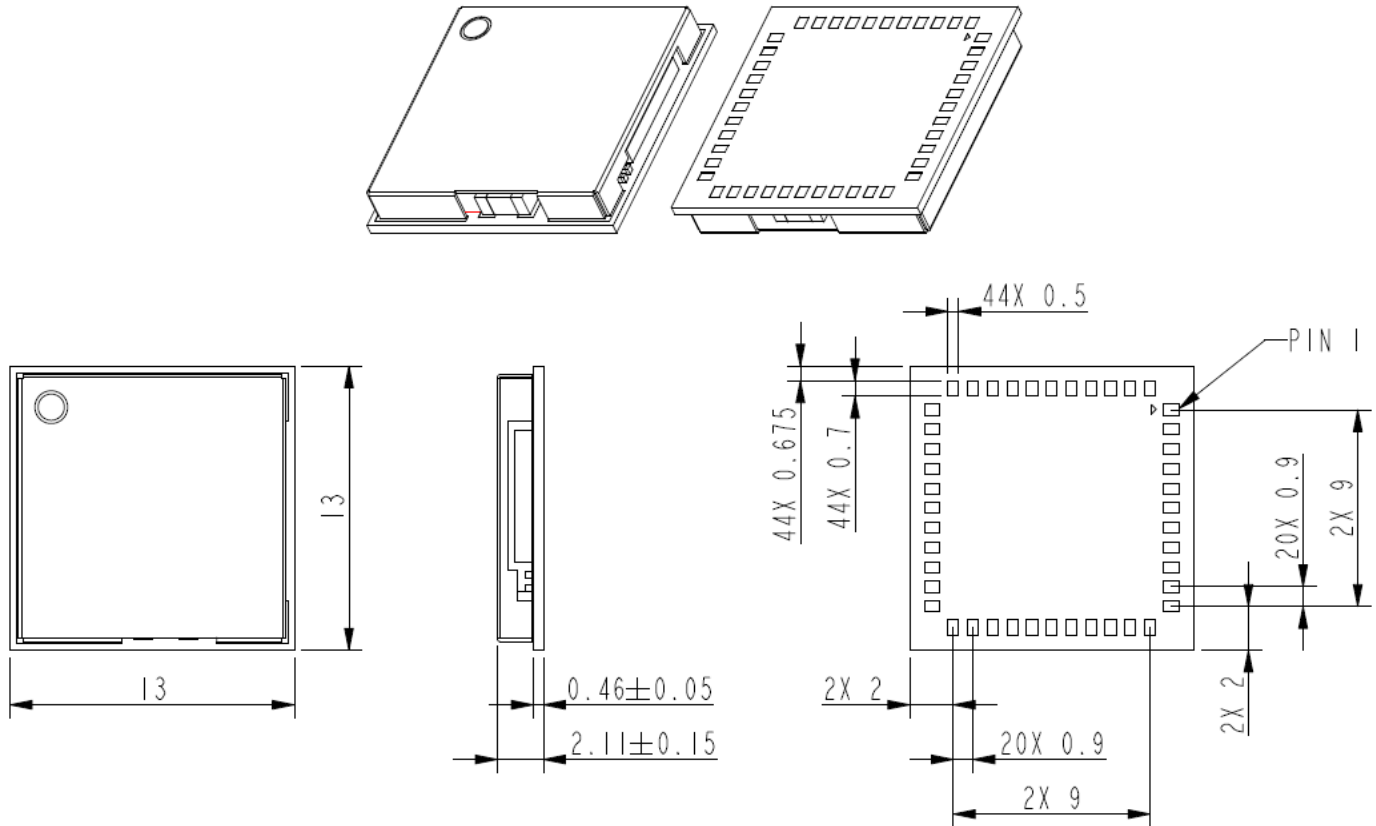
3.4.2 Receive Power Consumption

Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V, VDDIO = 3.3V	
				VBAT (mA)	
				Max.	Avg.
915	MCS0	1	Continuous Rx @ -95 dBm	TBD	TBD
		2	Continuous Rx @ -92 dBm	TBD	TBD
		4	Continuous Rx @ -89 dBm	TBD	TBD
		8	Continuous Rx @ -86 dBm	TBD	TBD
	MCS7	1	Continuous Rx @ -77 dBm	TBD	TBD
		2	Continuous Rx @ -74 dBm	TBD	TBD
		4	Continuous Rx @ -71 dBm	TBD	TBD
		8	Continuous Rx @ -68 dBm	TBD	TBD

* The power consumption is based on AzureWave test environment, these data for reference only.

4. Mechanical Information

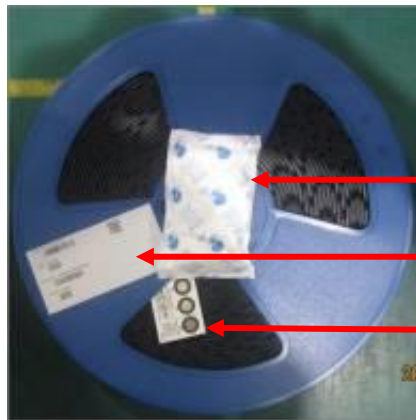
4.1 Mechanical Drawing



TOLERANCE UNLESS OTHERWISE SPECIFIED: $\pm 0.1\text{mm}$

5. Package information

1. One reel can pack 1000pcs
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel



One desiccant

One production label

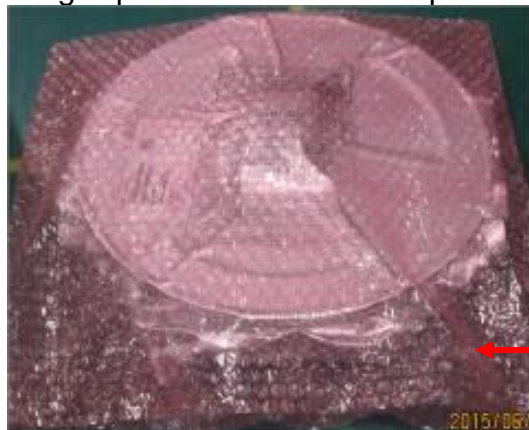
One humidity indicator card

3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



One production label

4. A bag is put into the anti-static pink bubble wrap



One anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box



One production label

6. **5 inner boxes** could be put into one carton

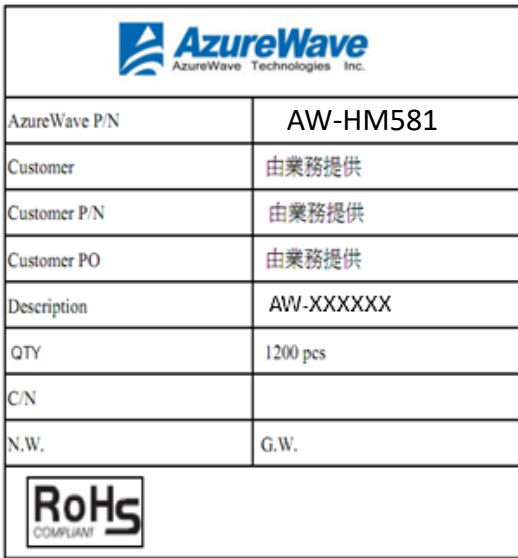



7. Sealing the carton by AzureWave tape



8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton



Example of carton label	
Example of box label	



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Example of production label	
Example of balance label	