

AW-HM482

IEEE 802.11ah Wireless LAN Module

Datasheet

Rev. E

03H

(For STD)

Features

General

- Supports 902 ~ 928MHz frequency band
- Supports single-stream 150kbps ~ 15Mbps data rate
- Supports AP and STA mode

Host interface

- UART and SPI support for host interface

Standards Supported

- IEEE Std 802.11ah-2016 compliant
- Security: OPEN, WPA2-PSK(AES), WPA3-OWE, WPA3-SAE

MAC Features

- S1G Beacon, NDP Control frame, TIM Compression, Unified scaling factor for max Idle period/listen interval/WNM-sleep interval, STA Type, S1G baseline functions (DCF, HCF, multi-rate support, A-MPDU), and S1G BSS operation
- Network efficiency enhancements: PV1 frames, NDP PS-Poll/PS-Poll Ack/Probe Req./Probe Resp., RAW avoidance, TSBTT, and Differentiated EDCA Parameter

- Power saving: Non-TIM operation, dynamic AID assignment, TWT, and Rescheduling STA's doze/awake cycle
- Wider coverage: Relay
- BSS scalability (up to 1024 STAs): Multicast AID, and Authentication control
- Low-cost STA/AP: EL operation, Flow Control

Peripheral Interfaces

- I2C, SPI and UART
- A Wi-Fi dedicated HSPI for data transfer to Host

Peripheral Interfaces

- Full IEEE 802.11ah compatibility with Enhanced performance
- Supports 1/2/4 MHz channel with optional SGI
- Supports S1G_1M, Short/Long format
- Modulation: OFDM with BPSK, QPSK, 16QAM, 64QAM

Revision History

Document NO: R2-2482-DST-01

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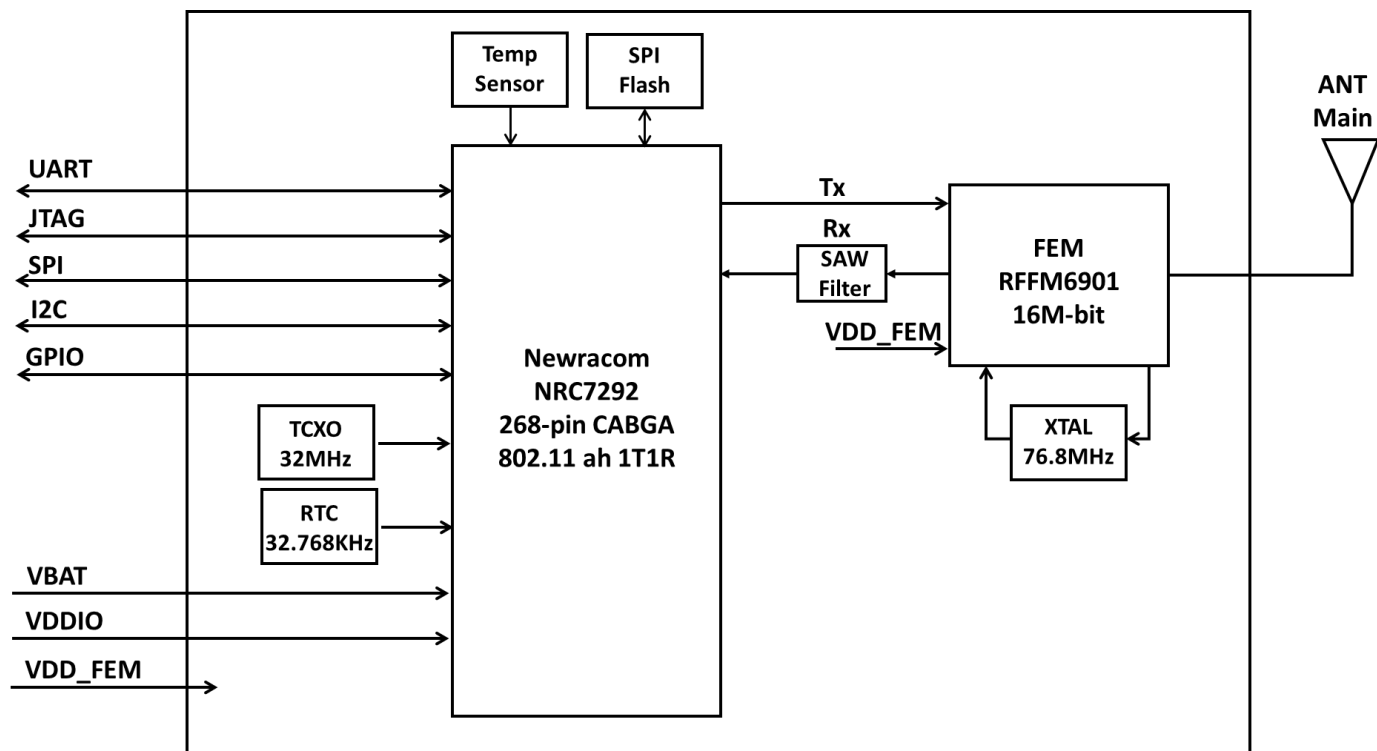
1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the pioneer of the IEEE 802.11ah WIFI solder down module --- **AW-HM482**. The **AW-HM482** is the smallest IEEE 802.11ah Wi-Fi module that operates in the Sub 1GHz license-exempt band, offering longer range and higher data rate for internet of things (IoT) applications. The **AW-HM482** enables streamlined data transfer interoperability with existing Wi-Fi networks while meeting up to 1Km long range data transfer with low power consumption requirements.

The **AW-HM482** integrated Newracom NRC7292 and external RF front end module (FEM) which can increase transmission power up to 20dBm. Two embedded ARM processors, Cortex-M0 and Cortex-M3, in the NRC7292 offers rich processing power to accommodate Wi-Fi subsystem as well as user application in a single Wi-Fi SoC. NRC7292 also includes two host interfaces, HSPI and UART, and many peripherals such as general SPI, I2C, UART, PWM, auxiliary ADC and GPIOs. In addition, it provides a memory large enough for both AP (access point) and STA (station) operation. The low-leakage retention memory can be used to store code and data necessary for fast wake-up from deep-sleep mode.

1.2 Block Diagram



AW-HM482 Block Diagram

1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	IEEE 802.11ah Wireless LAN Module
Major Chipset	Newracom NRC7292 (268-pin CABGA)
Host Interface	SPI
Dimension	18mm x 24mm x 2.55mm (Tolerance remarked in mechanical drawing)
Form Factor	LGA module, 74 pins
Antenna	For LGA, "1T1R, external" ANT Main : TX/RX
Weight	2.2g

1.3.2 WLAN

Features	Description					
WLAN Standard	IEEE 802.11ah					
Frequency Rage	(US/CA): Unit MHz 1MHz Bandwidth: 902.5, 903.5, 904.5, 905.5, 906.5, 907.5, 908.5, 909.5, 910.5, 911.5, 912.5, 913.5, 914.5, 915.5, 916.5, 917.5, 918.5, 919.5, 920.5, 921.5, 922.5, 923.5, 924.5, 925.5, 926.5, 927.5 2MHz Bandwidth: 903, 905, 907, 909, 911, 913, 915, 917, 919, 921, 923, 925, 927 4MHz Bandwidth: 906, 910, 914, 918, 922, 926					
Modulation	OFDM, BPSK, QPSK, 16-QAM, 64-QAM					
Channel Bandwidth	1/2/4 MHz					
Output Power (Board Level Limit)*		Min	Typ	Max	Unit	
	MCS0 (1/2/4 MHz) @EVM ≤ -5dB	18.5	20	21.5	dBm	
	MCS7 (1/2/4 MHz) @EVM ≤ -27dB	16.5	18	19.5	dBm	

Receiver Sensitivity		Min	Typ	Max	Unit
	MCS0 (1 MHz)		-106	-95	dBm
	MCS0 (2 MHz)		-99	-92	dBm
	MCS0 (4 MHz)		-99	-89	dBm
	MCS7 (1 MHz)		-88	-77	dBm
	MCS7 (2 MHz)		-84	-74	dBm
	MCS7 (4 MHz)		-81	-71	dBm
	MCS10 (1 MHz)		-108	-98	dBm
Data Rate	■ 1 MHz Bandwidth: up to 3Mbps				
	■ 2 MHz Bandwidth: up to 6.5Mbps				
	■ 4 MHz Bandwidth: up to 13.5Mbps				
Security	■ OPEN, WPA2-PSK(AES), WPA3-OWE, WPA3-SAE standard				

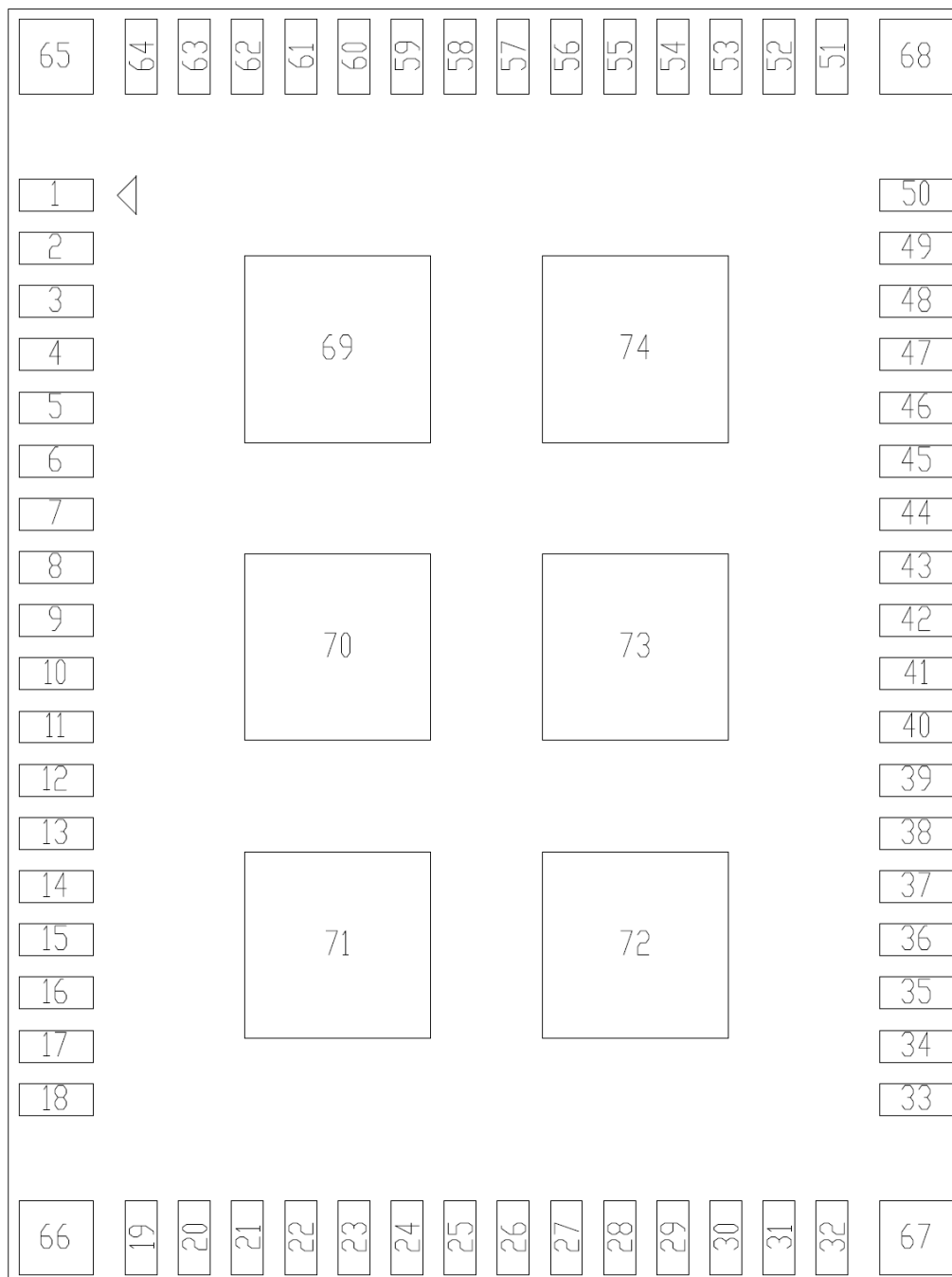
*** If you have any certification questions about output power please contact FAE directly.**

1.3.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	VBAT: 3.3V VDD_FEM: 4.0V VDDIO: 3.3V
Operating Temperature	-40°C~85 °C
Operating Humidity	less than 85%R.H
Storage Temperature	-40°C~85 °C
Storage Humidity	less than 60%R.H
ESD Protection	
Human Body Model	±2KV per ANSI/ESDA/JEDEC JS-001-2017
Changed Device Model	±500V per ESDA/JEDEC JS-002-2018

2. Pin Definition

2.1 Pin Map



AW-HM482 Pin Map (Top View)

2.2 Pin Table

Pin No.	Definition	Basic Description	Voltage	Type
1	GND	GROUND		GND
2	GND	GROUND		GND
3	GND	GROUND		GND
4	GND	GROUND		GND
5	VDD_FEM	Front End Module power input	4.0V	Power
6	VBAT	3.3V power supply	3.3V	Power
7	GND	GROUND		GND
8	GND	GROUND		GND
9	MODE_00	SW Define (When ROM BOOT) 11: Internal SRAM BOOT		I
10	MODE_01			I
11	MODE_02	0: ROM BOOT 1: XIP BOOT		I
12	MODE_03	0: Cortex-M0 Master 1: Cortex-M3 Master		I
13	MODE_04	0: Two CPU 1: One CPU		I
14	GND	GROUND		GND
15	HSPI_CS _n	Host SPI – Chip Select (active low)		I
16	HSPI_CLK	Host SPI – Clock		I
17	HSPI_MISO	Host SPI – Master in Slave out		O
18	HSPI_MOSI	Host SPI – Master out Slave in		I
19	HSIP_EIRQ	Host SPI – Interrupt		O
20	GND	GROUND		GND
21	GND	GROUND		GND

22	GP_00_UART2_TX	UART Channel2 Tx		I/O
23	GP_01_UART2_RX	UART Channel2 Rx		I/O
24	GP_02_UART2_RTS	UART Channel2 RTS		I/O
25	GP_03_UART2_CTS	UART Channel2 CTS		I/O
26	GP_04_UART0_TX	UART Channel0 Tx		I/O
27	GP_05_UART0_RX	UART Channel0 Rx		I/O
28	GP_06_UART3_TX	UART Channel3 Tx		I/O
29	GP_07_UART3_RX	UART Channel3 Rx		I/O
30	GP_08_UART1_RX	UART Channel1 Rx		I/O
31	GP_11_UART1_TX	UART Channel1 Tx		I/O
32	GP_17_I2C_SDA	I2C_SDA		I/O
33	GP_10_GPIO	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)		I/O
34	GP_09_GPIO	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)		I/O
35	GP_16_I2C_SCL	I2C_SCL		I/O
36	GP_15_SSP0_CLK	SPI0_Clock		O
37	PD_14_SSP0_CS	SPI0_Chip Enable(active low)		O
38	PD_13_SSP0_MOSI	SPI0_Master out slave in		O
39	PD_12_SSP0_MISO	SPI0_Master in Slave out		I
40	RESET	Reset (active high)		I
41	GND	GROUND		GND
42	JTAG_TRSTN	JTAG reset		I
43	JTAG_TMS	JTAG mode selection		I
44	JTAG_TCK	JTAG clock		I
45	JTAG_TDI	JTAG data input		O
46	JTAG_TDO	JTAG data output		I

47	GND	GROUND		GND
48	GND	GROUND		GND
49	RF_ANT	RF IN/OUT		I/O
50	GND	GROUND		GND
51	VDDIO	I/O supply Input		Power
52	GND	GROUND		GND
53	GND	GROUND		GND
54	AUXADCIN3	AUXADC input 3		I
55	AUXADCIN2	AUXADC input 2		I
56	AUXADCIN1	AUXADC input 1		I
57	GND	GROUND		GND
58	NC	No Connection		
59	NC	No Connection		
60	GND	GROUND		GND
61	GND	GROUND		GND
62	GND	GROUND		GND
63	GND	GROUND		GND
64	GND	GROUND		GND
65	GND	GROUND		GND
66	GND	GROUND		GND
67	GND	GROUND		GND
68	GND	GROUND		GND
69	GND	GROUND		GND
70	GND	GROUND		GND
71	GND	GROUND		GND

72	GND	GROUND		GND
73	GND	GROUND		GND
74	GND	GROUND		GND

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_FEM	Front End Module power input	-0.5	-	5.25	V
VBAT	3.3V power supply	-0.5		3.8	
VDDIO	I/O supply Input	-0.5		3.8	
T _{stg}	Storage temperature	-40	-	85	°C

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_FEM	Front End Module power input	3.8	4.0	4.2	V
VBAT	3.3V power supply	2.8	3.3	3.6	V
VDDIO	3.3V I/O supply Input	3.0	3.3	VBAT	V
VDDIO	1.8V I/O supply Input	1.62	1.8	1.98	V

3.3 Digital IO Pin DC Characteristics

VDDIO = 3.3V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V _{IH}	Input high voltage	2	-	3.6	V
V _{IL}	Input low voltage	-0.3	-	0.8	V
V _{OH}	Output high voltage	2.4	-		V
V _{OL}	Output low voltage		-	0.4	V

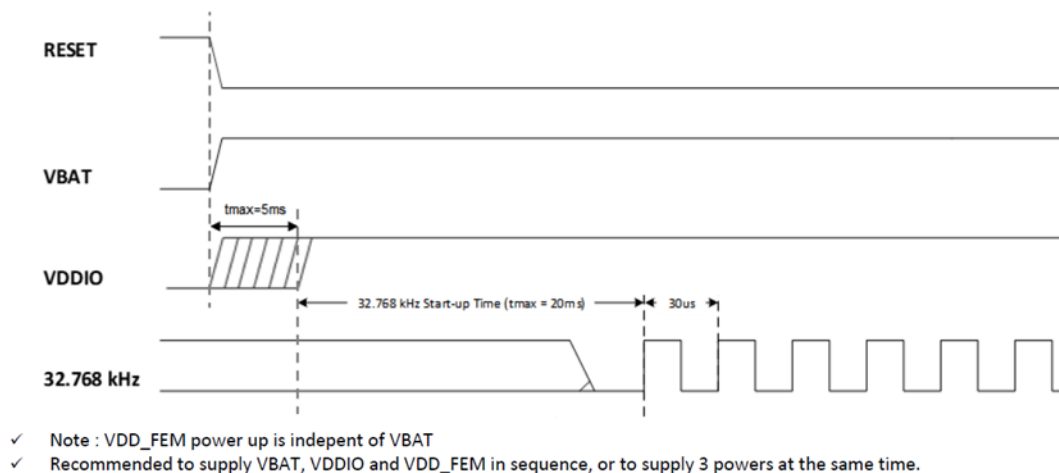
VDDIO = 1.8V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V _{IH}	Input high voltage	1.17	-	3.6	V
V _{IL}	Input low voltage	-0.3	-	0.63	V
V _{OH}	Output high voltage	1.35	-		V
V _{OL}	Output low voltage		-	0.45	V

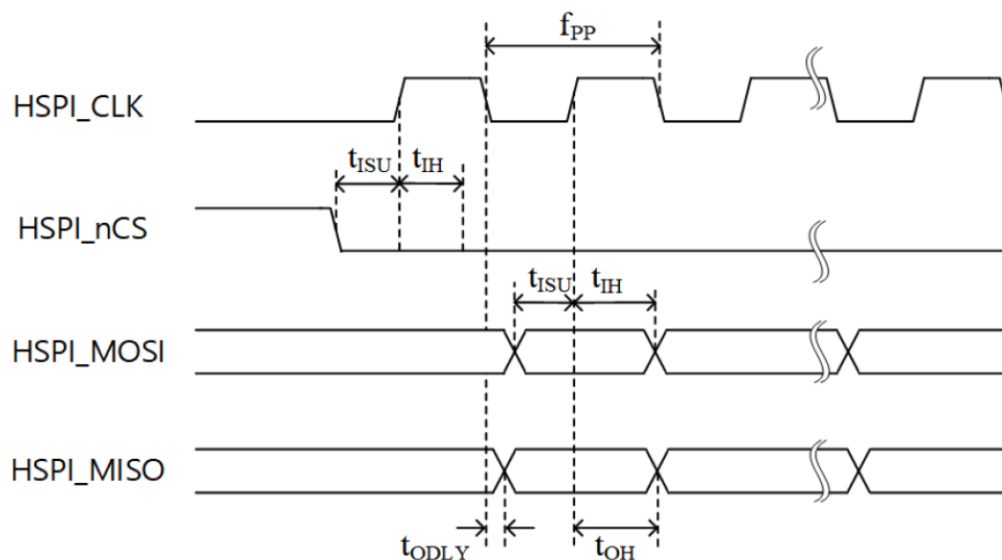
3.4 Timing Sequence

3.4.1 Power on sequence

The figure below shows the module power on sequence.

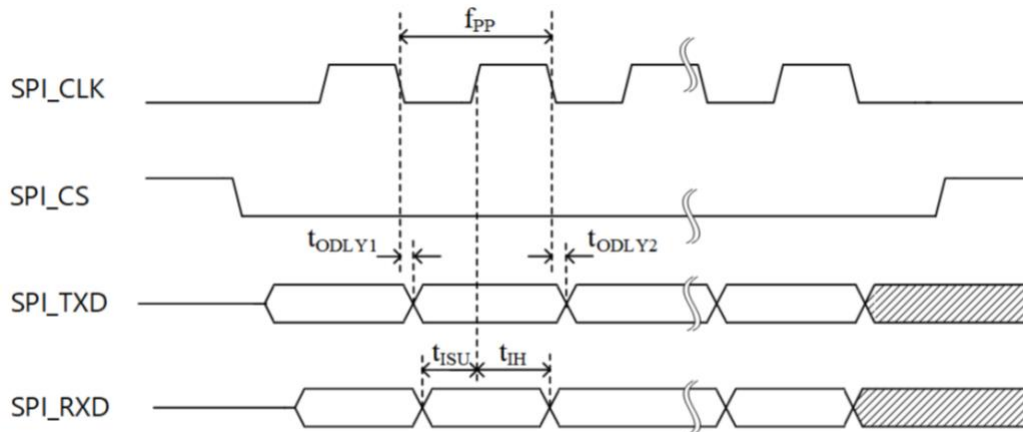


3.4.2 HSPI Timing



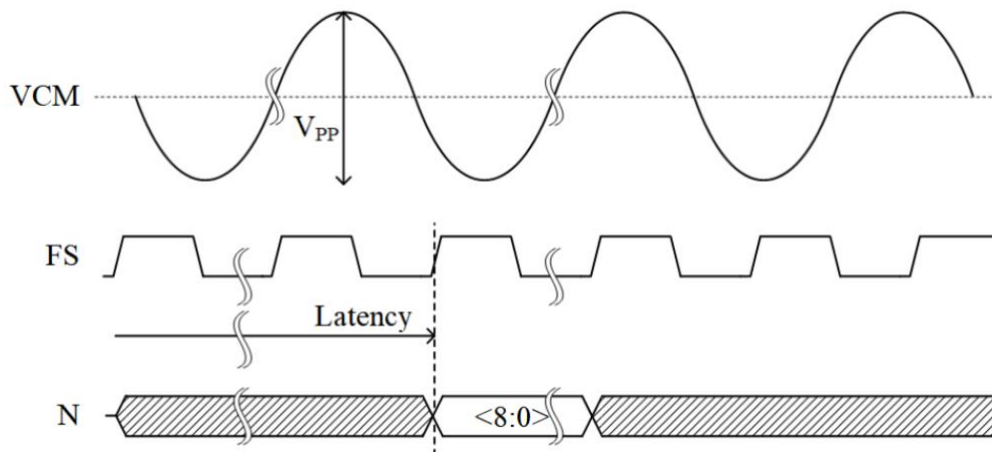
Symbol	Parameter	Min	Typ	Max	Unit
f_{PP}	Frequency	-	-	25	MHz
t_{ODLY}	Output delay time	6	-	-	ns
t_{OH}	Output hold time	2	-	-	ns
t_{ISU}	Input setup time	14	-	-	ns
t_{IH}	Input hold time	2.5	-	-	ns

3.4.3 SPI Timing



Symbol	Parameter	Min	Typ	Max	Unit
f_{PP}	Frequency				
	master	-	-	24	MHz
	slave	-	-	4	MHz
t_{ODLY1}	Output delay time1	0	-	10	ns
t_{ODLY2}	Output delay time2	0	-	10	ns
t_{ISU}	Input setup time	18	-	-	ns
t_{IH}	Input hold time	20	-	-	ns

3.4.4 AUXADC Timing



Symbol	Parameter	Min	Typ	Max	Unit
VCM	Input common-mode voltage	0.25	0.28	0.31	V
V_{PP}	Input Swing	-	0.5	-	V _{pp}
FS	Sampling Clock	-	32	-	MHz
Latency	Conversion latency (1 cycle = 31.25 ns)	-	11	-	cycle
N	Resolution	-	9	-	Bit
RIN	Input impedance	-	1	-	Mohms
I _{active}	Current consumption (1.2V supply)	-	-	300	uA
I _{down}	Power-down current (1.2V supply)	-	-	1	uA

3.5 Power Consumption

3.5.1 Transmit Power Consumption

Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V, VDD_FEM = 4.0V			
				VBAT (mA)		VDD_FEM (mA)	
				Max.	Avg.	Max.	Avg.
915	MCS0	1	Tx @ 22 dBm	36	33	260	228
		2		36	33	260	227
		4		37	34	260	230
	MCS7	1	Tx @ 19 dBm	38	35	200	182
		2		38	35	200	177
		4		38	35	200	168
	MCS10	1	Tx @ 22 dBm	36	33	260	232

* The power consumption is based on AzureWave test environment, these data for reference only.

3.5.2 Receive Power Consumption

Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V, VDD_FEM = 4.0V			
				VBAT (mA)		VDD_FEM (mA)	
				Max.	Avg.	Max.	Avg.
915	MCS0	1	Continuous Rx @ -80 dBm	36	33	8	7
		2	Continuous Rx @ -80 dBm	36	33	8	7
		4	Continuous Rx @ -80 dBm	36	34	8	7
	MCS7	1	Continuous Rx @ -80 dBm	36	33	8	7
		2	Continuous Rx @ -80 dBm	36	33	8	7
		4	Continuous Rx @ -80 dBm	36	34	8	7
	MCS10	1	Continuous Rx @ -80 dBm	36	33	8	7

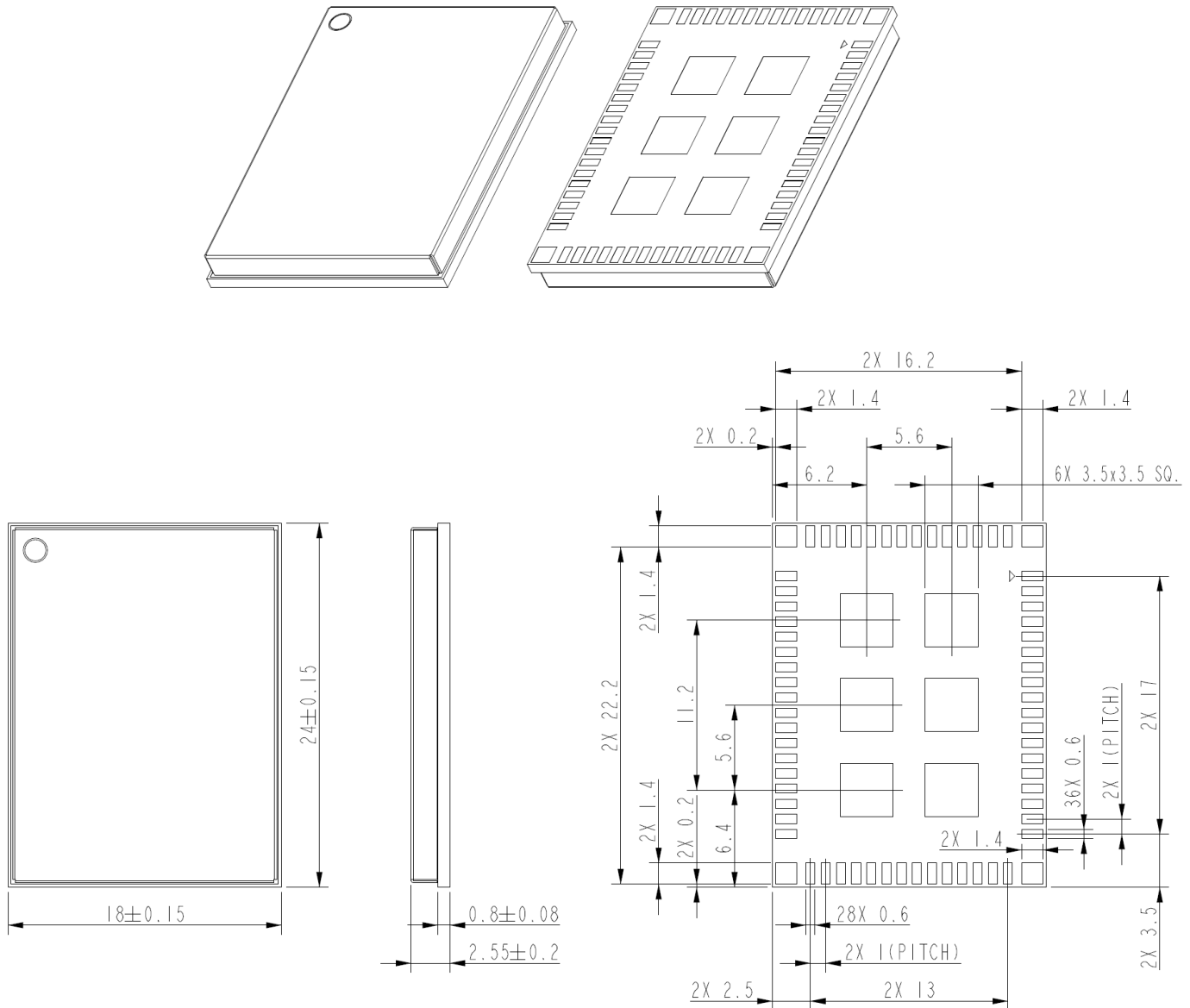
* The power consumption is based on AzureWave test environment, these data for reference only.

3.5.3 Deep Sleep Mode Power Consumption

DUT Condition	VBAT = 3.3V, VDD_FEM = 4.0V	
	VBAT (uA)	VDD_FEM (uA)
Deep Sleep Mode	30	0.5

4. Mechanical Information

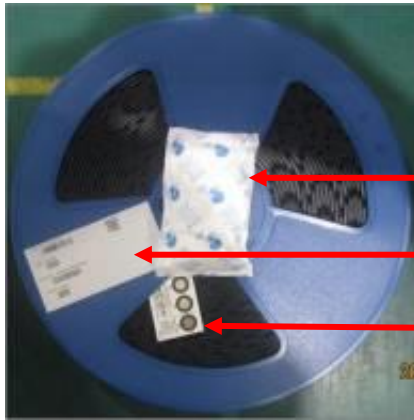
4.1 Mechanical Drawing



TOLERANCES UNLESS OTHERWISE SPECIFIED: ± 0.1 mm

5. Package information

1. One reel can pack 700pcs
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel

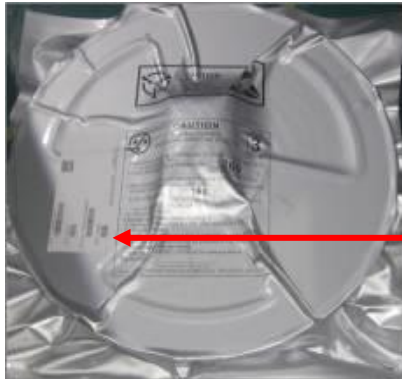


One desiccant

One production label

One humidity indicator card

3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag



One production label

4. A bag is put into the anti-static pink bubble wrap



One anti-static pink bubble wrap

5. A bubble wrap is put into the inner box and then one label is pasted on the inner box



One production label

6. **3 inner boxes** could be put into one carton



Production

7. Sealing the carton by AzureWave tape



8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton



Example of carton label	
Example of box label	



AzureWave

AzureWave Technologies, Inc.

Example of production label	
Example of balance label	